

## CT43X DESIGN RECOMMENDATION

By Allegro MicroSystems

### DESCRIPTION

The objective of this document is to help design engineers implement and use Allegro's new XtremeSense™ tunnel magnetoresistance (TMR) technology based CT430 and CT431 integrated contact current sensors in their designs. This application note provides circuit and printed circuit board (PCB) layout recommendations, as well as other recommendations and tips.

### SUMMARY

The following topics are discussed in this document:

- Package and Pinout
- Schematic Recommendations
- Layout Recommendations
- Isolation
- Filtering
- Thermal Considerations
- Stray Magnetic Field Reduction
- Reflow Conditions

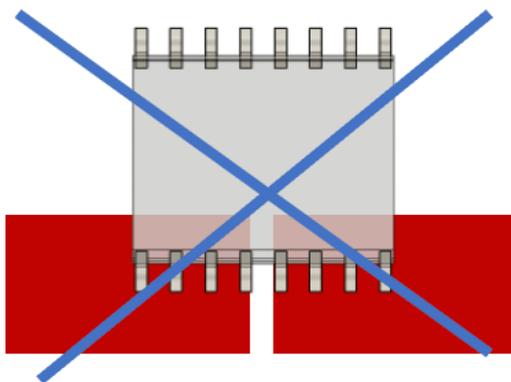


Figure 1: Overview of CT43x in SOICW-16 Package on a PCB with a Current Trace

### INTRODUCTION

The CT43x family is a coreless current sensor featuring a 1 MHz bandwidth, 5 kV isolation, stray-field magnetic rejection, and total error of less than 1% full-scale (FS) over the full  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  operational temperature range.

For the full performance details of the CT43x, refer to Allegro application note AN131.

### NONRATIOMETRIC VOLTAGE OUTPUT

The CT43x is designed to produce the same offset and sensitivity as long as the supply voltage is within the operating range. While ratiometry can mitigate some errors when the supply voltage is variable, it cannot be relied upon to provide the high-accuracy figures the CT43x achieves, primarily due to ratiometric scaling mismatch. The CT43x with its nonratiometric design offers high offset/sensitivity precision, supply-voltage noise immunity, and design flexibility.

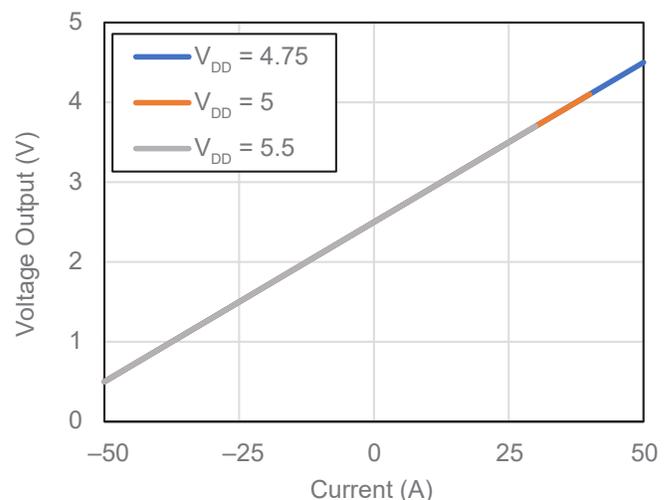
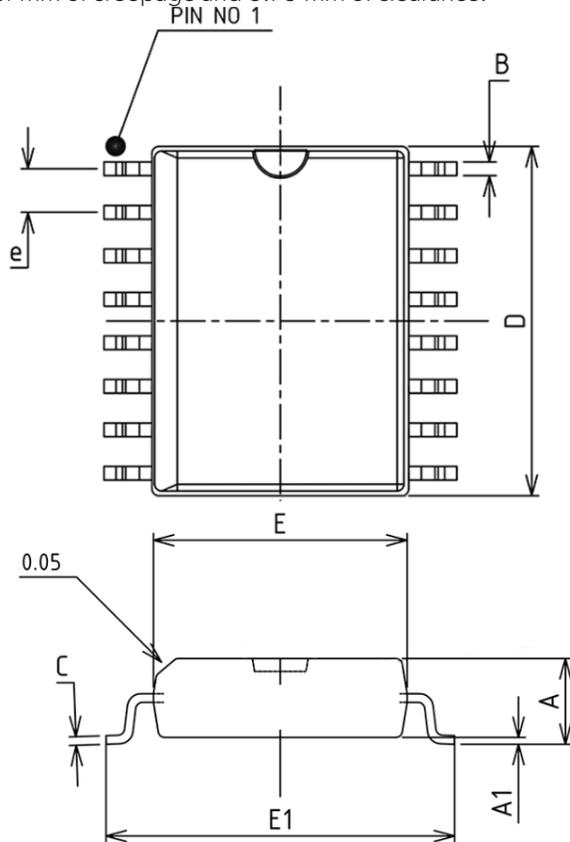


Figure 2: CT43x Output Voltage Gain and Offset Do Not Vary with a Varying Voltage Supply on the VCC Pin

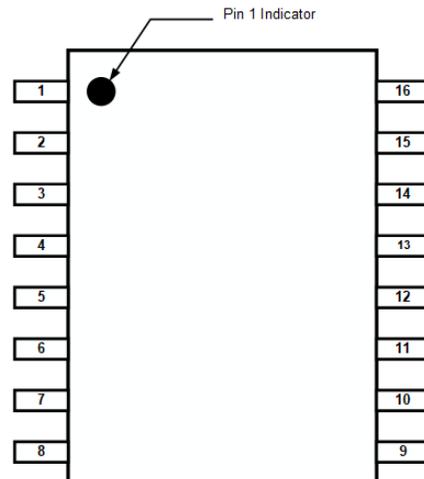
## SOICW-16 Package

The CT43x is packaged in an industry-standard SOICW-16, with a custom internal leadframe. This package offers 9.21 mm of creepage and 8.79 mm of clearance.



Symbol	Dimension (mm)
A	2.54
A1	0.2
B	0.4
C	0.254
D	10.2
E	7.5
E1	10.31
e	1.27

## Pinout



Pin #	Name	Function
1 – 4	IP+	Input current
5 – 8	IP-	Output current
9	VREF	Reference voltage output
10	GND	Ground
11	FLT	Fault detection output
12	FILTER	Helps set a low-pass filter
13	OUT	Voltage output
14	N/C	Do not connect
15	VCC	Supply Voltage
16	N/C	Do not connect

## SCHEMATIC RECOMMENDATIONS

### Decoupling Capacitor

A 1  $\mu\text{F}$  capacitor located as close as practical to the VDD pin is highly recommended. Decoupling capacitors avoid UVLO in case of a sudden  $V_{\text{DD}}$  drop and provides a relatively cleaner voltage supply free of voltage ripples.

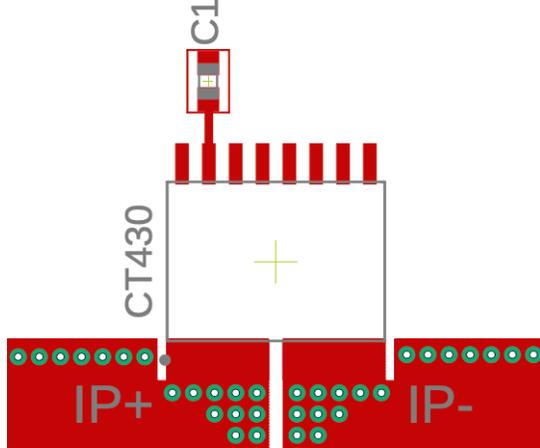


Figure 3: CT43x Footprint with Decoupling Capacitor C1

### Single-Ended ADC

The CT43x features a nonratiometric voltage output ( $V_{\text{OUT}}$ ). The OUT pin can be directly connected to a single-ended analog-to-digital converter (ADC) input with a precise internal or external reference voltage, which is typically available in microcontroller unit (MCU) integrated ADCs.

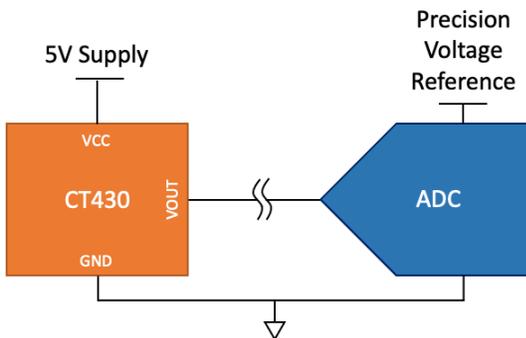


Figure 4: CT43x Connected to Single-Ended ADC

### Differential ADC

In noisy environments, such as power systems with fast-switching transistors, the VREF pin of the CT43x can be used along with the OUT pin to generate a differential voltage that can be used with a differential input ADC. The main benefit of measuring  $V_{\text{REF}} - V_{\text{OUT}}$  is to mitigate the  $dV/dt$  transients and supply noise that appears on the voltage supply and signal traces.

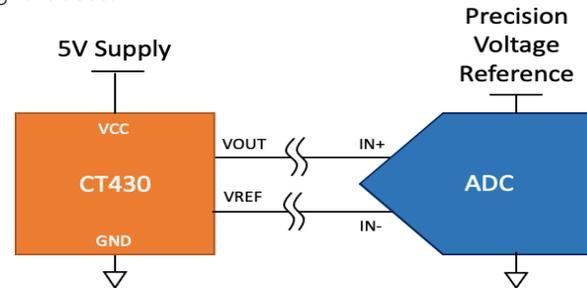


Figure 5: CT43x Connected to Differential ADC Input

Contrary to Hall-effect-based sensors, VREF is not needed to minimize offset temperature drift on the CT43x.

### Reference Voltage (VREF) Pin

The CT43x VREF pin is intended to be used as a voltage reference only. Hence, it does not sink/source more than 5 mA. For this reason, a series resistor of 10  $\text{k}\Omega$  is highly recommended to guarantee the precision of the voltage output.

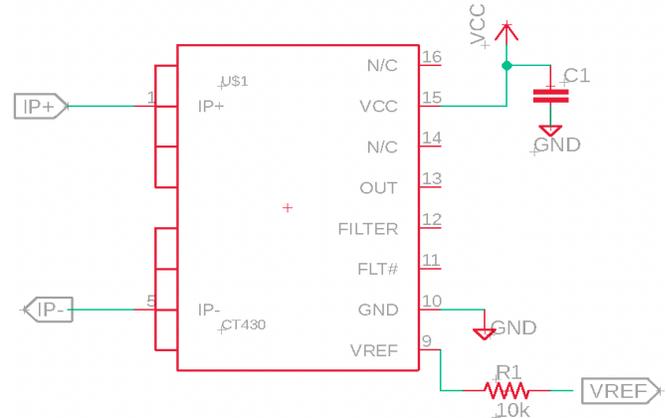


Figure 6: CT43x with 10  $\text{k}\Omega$  R1 Resistor Connected in Series to VREF Pin

### Fault Pin

The FAULT pin is an open-drain output that can sink up to 20 mA. When active, the FAULT pin is pulled low by the CT43x; otherwise, it assumes a high-impedance (high-Z) value. Depending on the design requirements, a pull-up resistor can be used.

## PCB LAYOUT RECOMMENDATION

### Footprint

The recommended footprint for the CT43x is detailed in Figure 7.

NOTE: This footprint is able to achieve 8 mm creepage between the pins carrying the primary current (pins 1 through 8) and the signal pins.

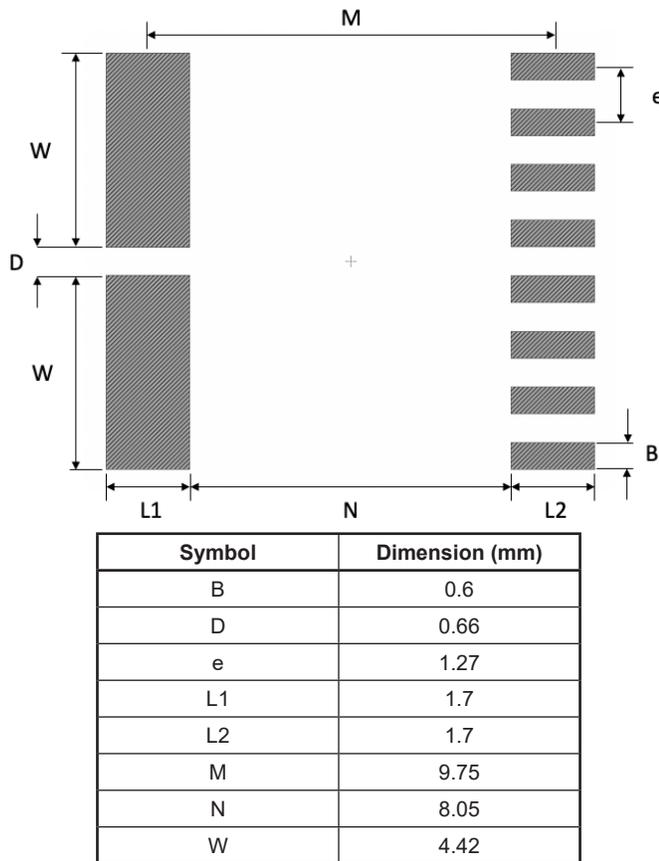


Figure 7: CT43x SOICW-16 Recommended Footprint

### Current-Carrying Trace

The current trace design is very important because it impacts different aspects of the overall performance of the current sensing system.

#### Heating

To minimize heat generation, implementation of the following is recommended:

- Use of at least a 70  $\mu\text{m}$  (2 oz.) copper thickness
- Use of at least a four-layer board
- Addition of thermal-vias close to the primary current pins

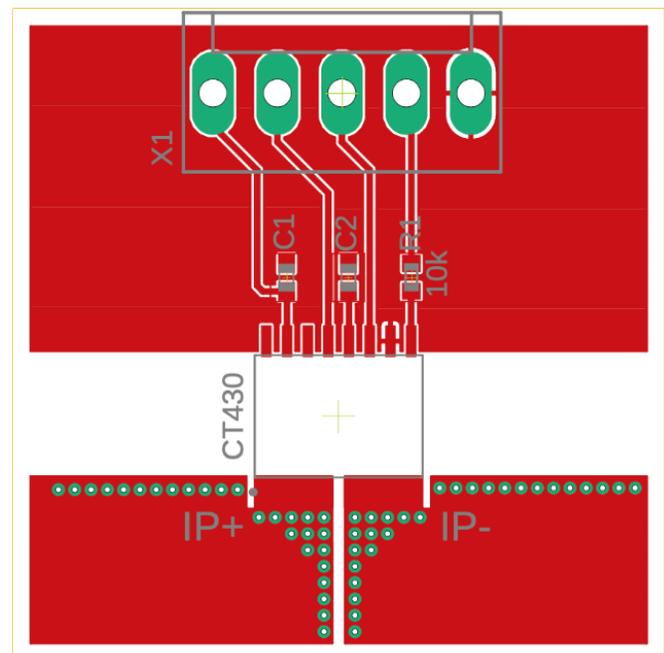


Figure 8: Layout of Current-Carrying Trace and Signal Traces

### Magnetic Coupling

To reduce any magnetic interference generated by the current trace:

- The orientation of the current traces is important. Ideally, the current traces should not come from behind the sensor.
- The current trace should not be extended below the package.

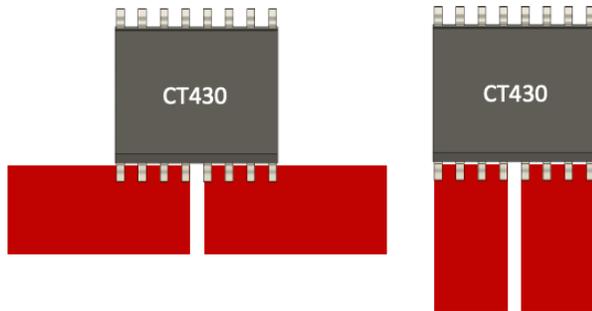


Figure 9: Recommended Layouts of Current-Carrying Trace

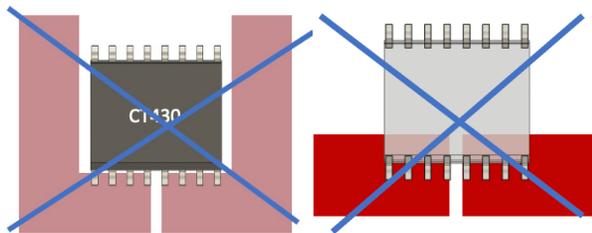


Figure 10: Not Recommended

### Isolation

The distance between the current trace and the signal pins needs to be maximized.

Hence, extending the current trace below the package or behind the sensor leads to shorter distances between the current trace and signal traces, reducing the isolation specification.

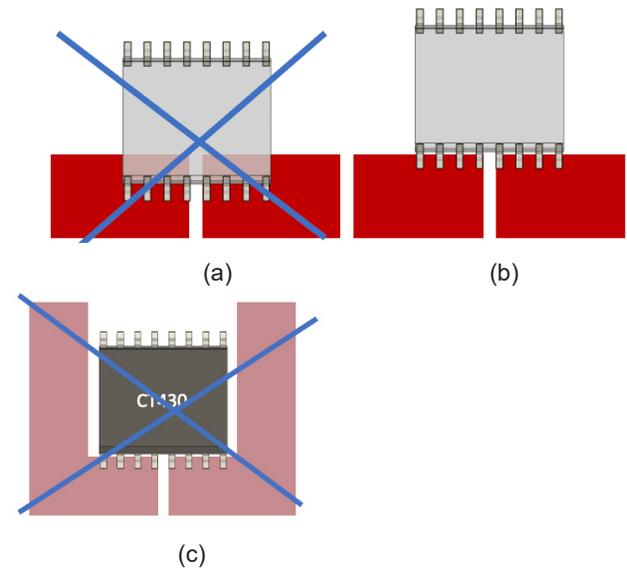


Figure 11: CT43x Recommended (b) and Not Recommended (a) and (c) Layouts for Isolation

### Signal Traces

All signal paths on the PCB should be as wide and short as possible to avoid electrical noise from external capacitive coupling. Signal pins are numbered 9 to 16.

## ISOLATION

The package of the CT43x is compliant with safety standard UL61800-5-1. The clearance and creepage between the primary conductor and the signal paths is more than 8.79 mm and 9.21 mm, respectively.

If the creepage is shorter than the design requirement, it is possible to increase it more than 9 mm by adding a slit in the board, as shown in Figure 12.

In terms of safety, the CT43x is certified to be IEC/UL 62368-1 and UL1577 compliant.

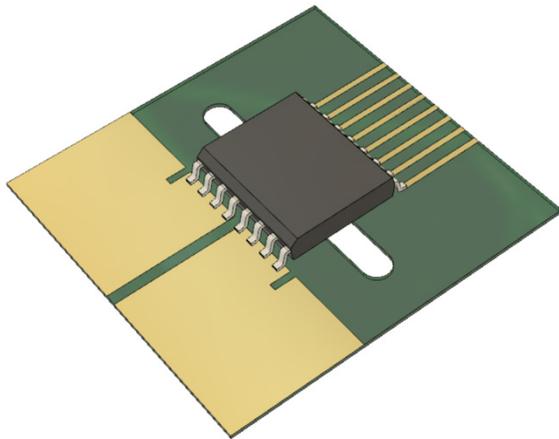


Figure 12: CT43x PCB with Slit to Increase Creepage

## FILTERING

In applications where the full 1 MHz bandwidth of the CT43x is not required by the design constraints, the filter pin allows the user to implement a low-pass filter that reduces bandwidth, which provides benefits in terms of noise and resolution.

A single capacitor is used to implement a low-pass filter thanks to the integrated 15 kΩ resistor already in the chip.

Recommended capacitor values along with the obtained bandwidths are shown in Table 1.

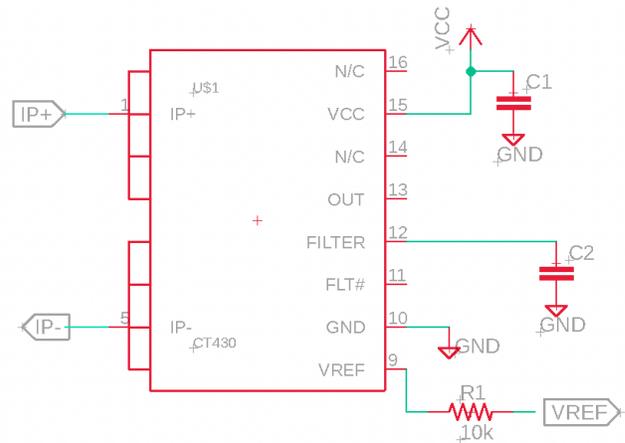


Figure 13: CT43x Using Capacitor C2 to Implement Low-Pass Filter

**Table 1: Recommended Capacitor Values and Obtained Bandwidths**

C (pF)	BW (kHz)	Noise (mA <sub>RMS</sub> )
5	1,000	15
10	500	12
20	250	11
47	100	9

## THERMAL CONSIDERATIONS

The CT43x is capable of supporting up to 50 A<sub>RMS</sub> continuous current at room temperature and even larger current for short bursts.

The junction temperature is the limiting factor and needs to stay below 130°C. The main parameters that contribute to the junction temperature are:

- Ambient temperature
- PCB layout and characteristics
- Primary current

The junction temperature can be estimated by measuring temperature on the red dot shown in Figure 14.

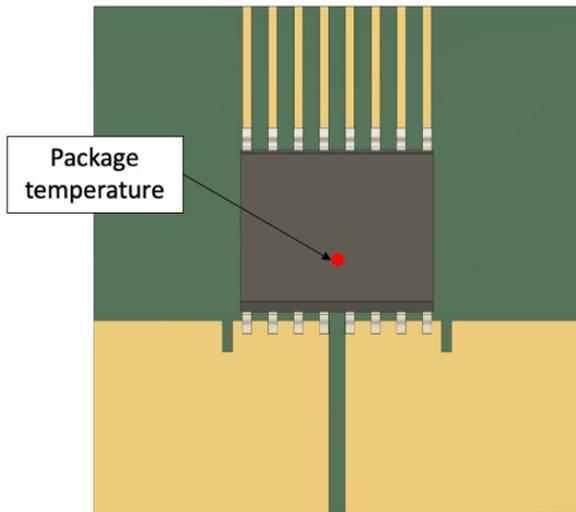


Figure 14: CT43x SOICW-16 with Red Dot Showing Relative Hottest Point on Package

## Reference Measurements

The measurements in this section were performed using the CT430 (CTD430-50DC) evaluation board. The rise of junction temperature  $T_J$  relative to the ambient temperature versus continuous current at different ambient temperatures is shown in Figure 15. The rise in temperature on the package versus time is shown in Figure 16.

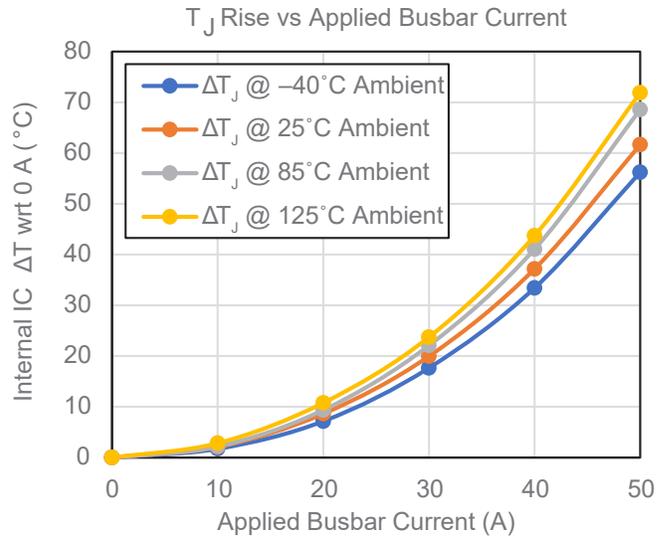


Figure 15: Junction Temperature of CT43x vs. Applied Current through Busbar

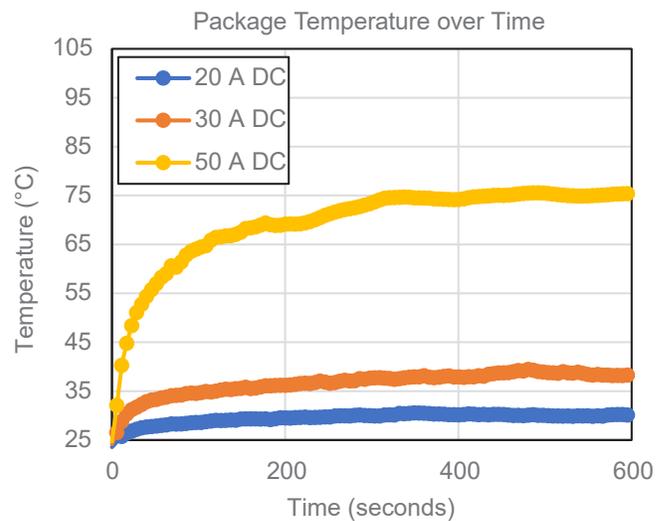


Figure 16: Package Temperature of CT43x over Time

## STRAY MAGNETIC FIELD REDUCTION

The CT43x benefits from two advantages when it comes to common-mode field rejection (CMFR), detailed next.

### Axis of Sensitivity

XtremeSense TMR has a planar axis of sensitivity as opposed to Hall-effect perpendicular orientation of sensitivity. The CT43x is thus better-suited to handle crosstalk magnetic fields generated by adjacent current-carrying conductors. The magnetic field generated by a nearby conductor is mainly perpendicular, as shown in Figure 17.

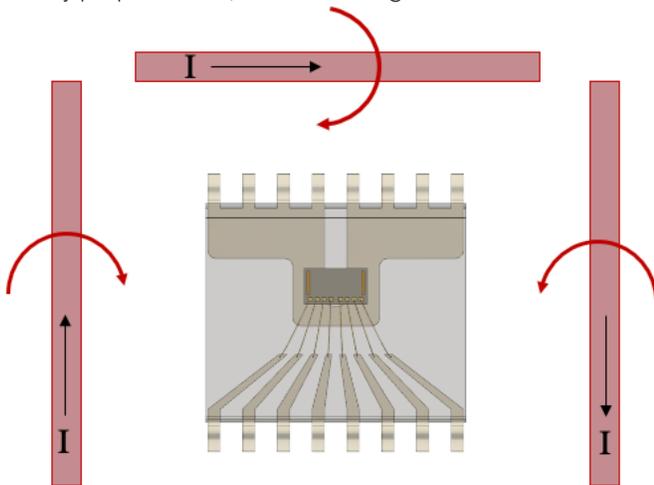


Figure 17: CT43x with Three Adjacent Current-Carrying Conductors (shown in red)

## Differential Sensing

The CT43x uses two full-bridge XtremeSense TMR sensors to achieve differential sensing capability, which allows CMFR.

A detailed analysis of the CT43x CMFR is available in Allegro application note AN131.

The CT43x family is meant to be used in magnetically noisy environments and in designs containing multiple current paths.

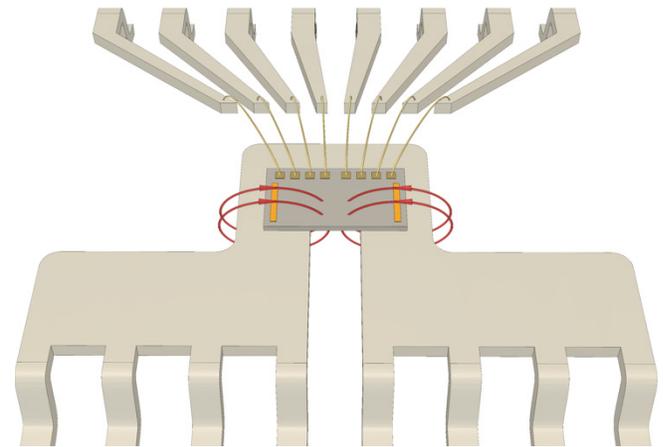


Figure 18: CT43x Leadframe Approximation Showing Internal U-Shape that Allows Differential Sensing Capability

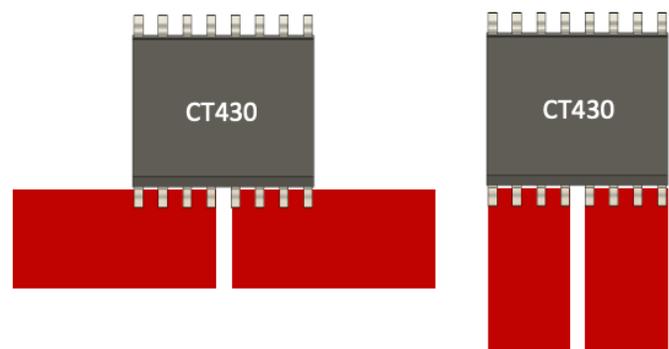


Figure 19: Recommended Layouts of Current-Carrying Trace

## REFLOW CONDITIONS

The recommended reflow temperature profile is outlined in Table 2 and Figure 20. For more details, refer to Allegro application note AN125.

Table 2: Recommended Reflow Temperature Profile

Parameter	1	TC Mean	TC Range
Peak Temperature	261.4°C	261.4°C	0
Rising Temperature Between 150°C and 200°C	87.31 s	87.31 s	0
Total Time Above 217°C	69.88 s	69.88 s	0
Total Time Above 255°C	36.61 s	36.61 s	0

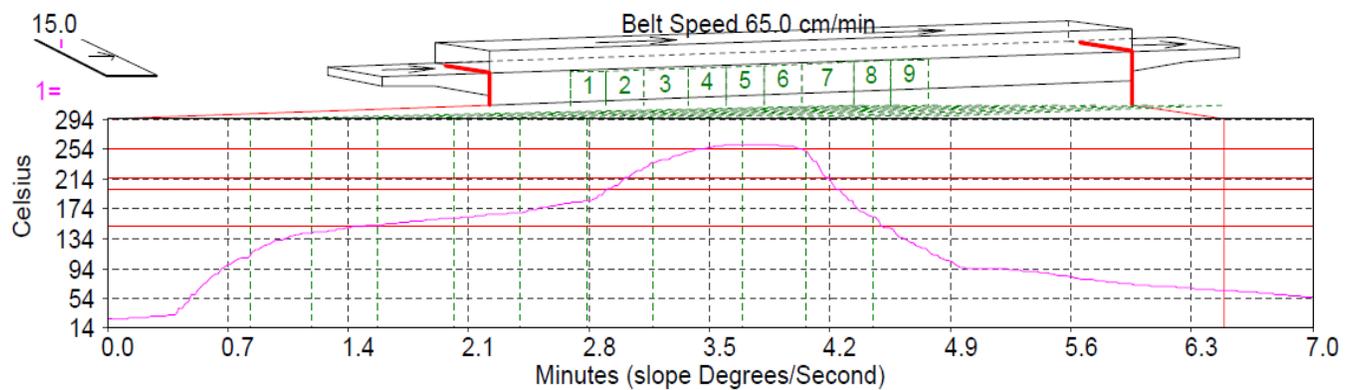


Figure 20: Lead-Free Solder Temperature Profile and Belt Speed for Allegro TMR Products

## OTHER INFORMATION

For additional documentation, visit [www.allegromicro.com](http://www.allegromicro.com).

*Revision History*

Number	Date	Description	Responsibility
1	November 16, 2023	Document rebrand and minor editorial corrections	J. Henry

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