

CT430 POWER MEASUREMENT MODULE

By Allegro MicroSystems

INTRODUCTION

This application note is for a power measurement module based on Allegro MicroSystems' CT43x contact current sensor. It discusses PCB design guidelines and how to interface with an external MCU for reading all components of a power measurement, e.g. RMS values, active and passive power, etc.

The CT43x devices are a family of high-bandwidth and low-noise current sensors that offer accurate measurements for a wide variety of enterprise and industrial applications.

HIGH-LEVEL DESIGN

The power meter is a module that conditions and reads current and voltage analog values, quantizes them using analog-to-digital converters (ADCs), and based on the voltage and current values, calculates instantaneous and RMS values. It provides an SPI interface for the end user to readout the power values from the module using its own microcontroller unit. Figure 1 shows the high-level diagram of this module.

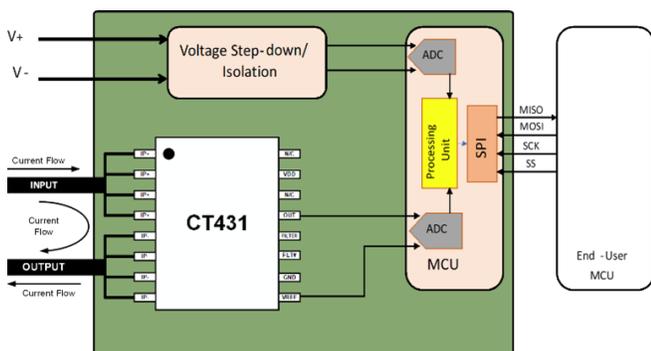


Figure 1: Power module block diagram

MODULE PCB OVERVIEW

Inputs and Outputs

The module's I/O consist of a high current conducting path through the IP+ and IP- pins (shown in Figure 1), voltage monitoring inputs, CT43x signals, and SPI communication pins, as illustrated in Figure 2.

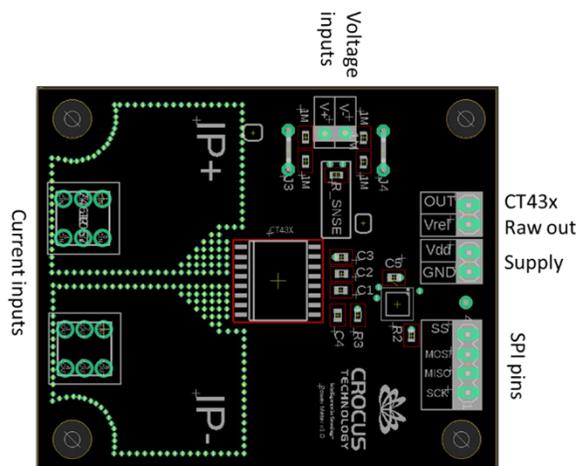


Figure 2: PCB module pinouts

Placing the module in line with the load

As shown in Figure 3, the current conducting path passes from IP+ through the CT43x and out IP- to reach the load. This is considered 'high-side' current sensing. In the high-side configuration, the voltage monitoring input (V+) can be connected directly to the IP+ on PCB.

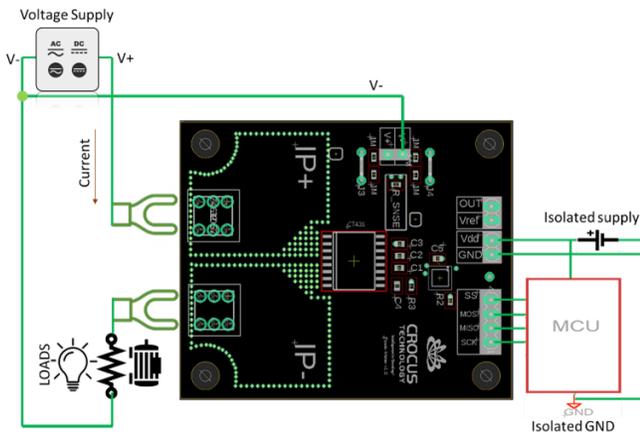


Figure 3: Module circuit connection

Since the module already has a trace between IP+ and V+ then only the negative voltage monitor pin (V-) needs to be connected to the negative or neutral side of the voltage supply. If the module is not placed on the load's high side, then both voltage inputs are required to be connected to the module's V+ and V- pins. In this case, the PCB trace from IP+ to V+ must be cut, as shown in Figure 4.

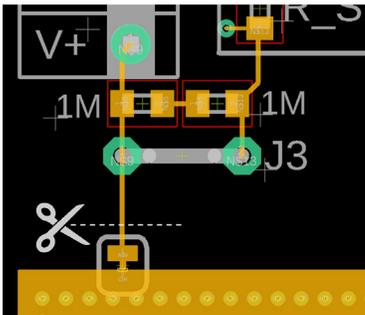


Figure 4: Cutting the path between IP+ and V+

Voltage Sensing

For high voltage measurement, the input voltage needs to be stepped down and isolated before reaching the microcontroller. A step-down IC or a simple resistive circuit can be used for that purpose.

Figure 5 shows the step-down resistive circuit consisting of four 1 MΩ resistors (R_{ISO}) to isolate the V+ and V- high-voltage parts from the digital low-voltage side. If an external step-down circuit is used this resistive network needs to be bypassed and disabled by connecting J3 and J4.

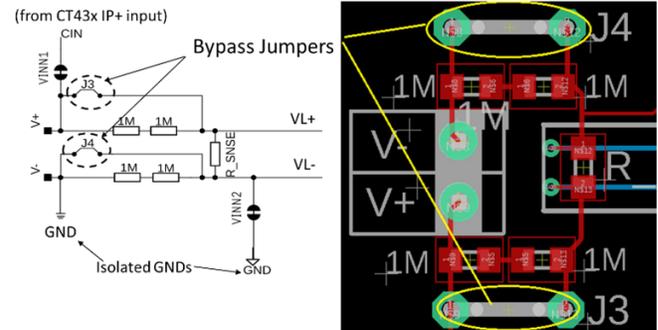


Figure 5: J3 and J4 jumpers to bypass the isolation

Choosing R_{SNSE} for Voltage Measurement

The R_{ISO} isolation network is connected across the R_{SNSE} resistor. The voltage difference on both sides of R_{SNSE} will be measured by the MCU to quantize the supply voltage. The value of R_{SNSE} depends on the maximum voltage between V+ and V- and must be chosen so that 625 mV (max) is measured across R_{SNSE} for $(V+ - V-)$. In this case, for correct measurements the input voltage cannot exceed 0.625 V. The ICs will be damaged if greater than 5.5 V is applied.

The equation for choosing the appropriate value for R_{SNSE} is:

$$R_{SNSE} = R_{ISO} \times \frac{0.625}{(V_{high-max} - 0.625)}$$

For example, to measure 300 V on the high side, and with R_{ISO} of 4 M (4 × 1 MΩ), a value of $R_{SNSE} \sim 8.2$ KΩ is required.

ATTINY426 PROGRAMMING

Microcontroller

Figure 6 shows the module's ATtiny426 MCU and the required pin connections. This includes CT43x OUT and VREF pins, stepped down VL+ and VL- voltage inputs, SPI interface pins (MOSI, MISO, SCK and SS), supply and UPDI programming pin.

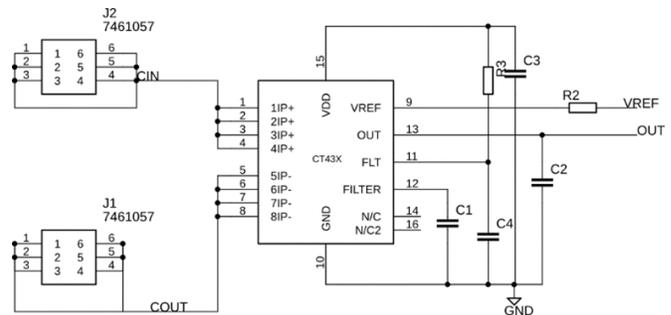


Figure 6: ATtiny426 Connections

Programming the ATtiny

The ATtiny's C++ firmware was developed using the Microchip

Studio IDE environment. The same IDE will both compile and program the MCU.

Microchip's ATMEL-ICE debugger/programmer supports the UPDI pin for programming the ATtiny MCU. To avoid accidental damage, the programmer must be disconnected while working with high voltages.

The debugger requires only three connections to the ATtiny: UPDI, VDD and GND. The debugger does not power-up the ATtiny, the VDD and GND connections provide power feedback to the debugger. Figure 7 shows the three pins required for programming.

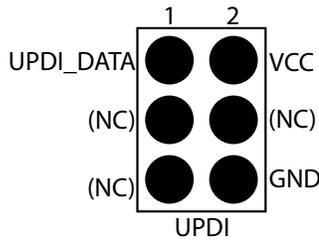


Figure 7: Pins required for programming

Operating Voltage

The PCB module's CT43x can operate with either a 3.3V or 5.0V supply. Fortunately, the ATtiny can operate with either voltage.

CALCULATING POWER VALUES

The ATtiny426 samples the current and voltage signals every 250 μs (Figure 8) and stores the quantized values in registers (Table 1) as instantaneous values. The module monitors the voltage value to detect the zero-crossing moment. Upon its detection, RMS values and power components are calculated.

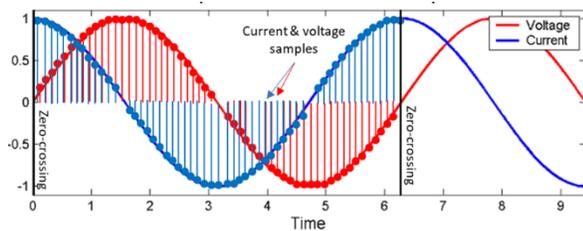


Figure 8: AC Cycle Current and Voltage Sampling

Below are brief descriptions of the calculated values.

Quantized instantaneous values: I_{inst} & V_{inst} :

The instantaneous values are the last quantized current and voltage values from the ADCs.

Calculated RMS values I_{RMS} & V_{RMS} :

The RMS values are based on discrete current and voltage measurements taken every 250 μs during a sinusoidal AC cycle.

Their values are calculated using the following equations:

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} I_n^2}{N}} \quad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{N-1} V_n^2}{N}}$$

In which, I_n and V_n are instantaneous values and N is the number of samples during the sinusoidal AC cycle.

Calculated Apparent Power $P_{apparent}$:

$P_{apparent}$ is calculated using the RMS values:

$$P_{apparent} = I_{RMS} \times V_{RMS}$$

Calculated Active/Reactive Power

P_{active} & $P_{reactive}$:

Calculated active power is based on the instantaneous values:

$$P_{active} = \frac{\sum_{n=0}^{N-1} I_n \times V_n}{N}$$

Consequently, reactive or imaginary power is calculated by:

$$P_{reactive} = \sqrt{P_{apparent}^2 - P_{active}^2}$$

Calculated Power Factor PF:

Power Factor is the ratio between active and apparent power:

$$PowerFactor = \frac{P_{active}}{P_{apparent}}$$

Sign of Power Factor and Reactive Power:

Sign of PF and $P_{reactive}$ determines whether the current sign signal is lagging or leading, the load is capacitive or inductive and whether the power is produced or consumed by the load (Figure 9).

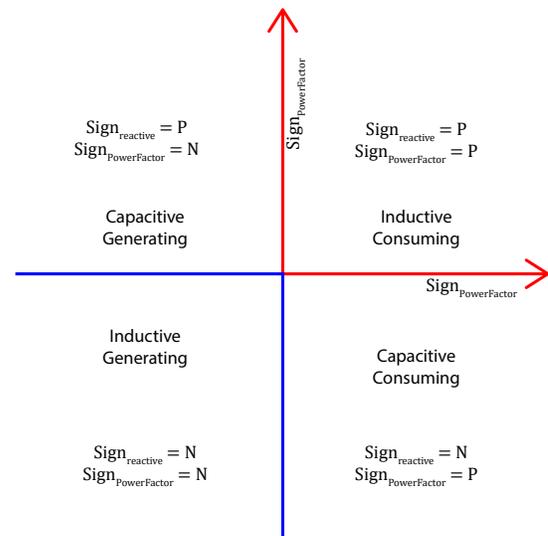


Figure 9: Power Factor and Apparent Power

Table 1: ATtiny Register Address Space

Address	Bit Positions																																					
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0						
0x20	I _{rms}																V _{rms}																					
0x21	P _{reactive}																P _{active}																					
0x22					Sign _{PowerF}	Sign _{reactive}	(Pf) Power Factor																P _{apparent}															
0x25	numpts																																					
0x2A	I _{inst}																V _{inst}																					
0x2C	P _{inst}																																					

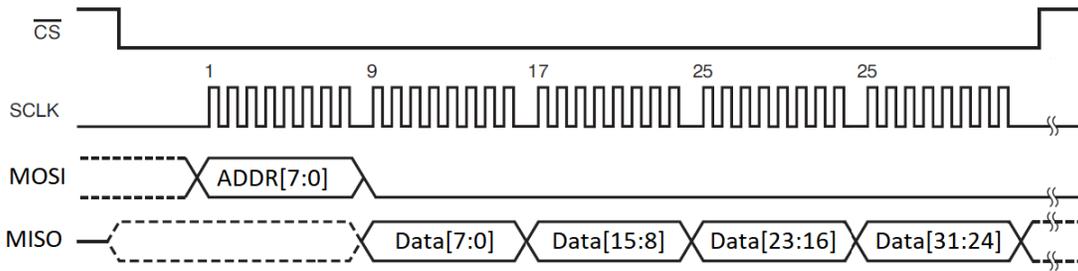


Figure 10: SPI Communication Protocol

REGISTER DEFINITION

SPI interface

The module provides an SPI interface for register value readouts. Every readout is a 32-byte word shifted out after receiving an 8-bit register address (Figure 11). The current data is in response to the previous given address. The response of the current address will be shifted out on the next SPI readout.

The address part can take the values described in Table 1.

0x20: I_{RMS} – V_{RMS}

I_{RMS} and V_{RMS} are 11-bit unsigned integer values. The range and conversion information is provided in Table 2.

Table 2: 0x20: I_{RMS} and V_{RMS}

	Range	Conversion Formula	Unit
I _{RMS}	0–2047	I _{RMS} × 0.03	A
V _{RMS}	0–2047	V _{RMS} × 0.3 × $\frac{R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mV

0x21: P_{reactive} – P_{active}

The active and reactive powers are two 16-bit signed integer values. Table 3 shows the relationship between their value and the real physical values.

Table 3: 0x21: P_{reactive} – P_{active}

	Range	Conversion Formula	Unit
I _{RMS}	–32768 to 32767	P _{active} × 2.3 × $\frac{R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mVAR
V _{RMS}	–32768 to 32767	P _{active} × 2.3 × $\frac{R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mW

0x22: Apparent Power – Power Factor and Signs

Apparent power is a 12-bit unsigned integer value. Table 4 shows the relation between their value and the real physical value.

Power Factor is an 11-bit signed fractional value between. Table 4 shows how to convert the digital value to the fractional value.

Negative or positive sign for reactive power and power factor determines the type of load and phase relation between current and voltage signals (Figure 10).

Table 4: 0x22: $P_{apparent}$ – PF $Sign_{react}$ & $Sign_{pf}$

	Range	Conversion Formula	Unit
$P_{apparent}$	-32768 to 32767	$\frac{P_{reactive} \times 2.3 \times R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mVA
PF	-32768 to 32767	PowerFactor /1024	-
$SIGN_{pf}$	0 to 1	1: Negative, 0: Positive	-
$SIGN_{react}$	0 to 1	1: Negative, 0: Positive	-

0x25: Number of points numpts

Numpts is a 10-bit output that determines the value of N, as described in the previous section. N is the number of current and voltage samples used to perform discrete integration of the RMS and power values. Numpts varies based on the frequency of the signal and is determined by the times of voltage signal zero-crossing.

0x20: Instantaneous current and voltage I_{inst} – V_{inst}

I_{inst} and V_{inst} are 12-bit signed integer values. Table 5 lists the range and conversion formula.

Table 5: 0x20: I_{inst} and V_{inst}

	Range	Conversion Formula	Unit
I_{inst}	-2048 to 2047	$I_{inst} \times 0.3$	A
V_{inst}	-2048 to 2047	$V_{inst} \times 0.3 \times \frac{R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mV

0x2C: P_{inst}

Instantaneous power is a 16-bit signed integer value. Table 6 shows the relationship between the value and the real physical value.

Table 6: 0x2C: P_{inst}

	Range	Conversion Formula	Unit
P_{inst}	-32768 to 32767	$P_{inst} \times 2.3 \times \frac{R_{ISO} \times R_{SNSE}}{R_{SNSE}}$	mW

PCB DESIGN

Two main considerations when designing the PCB layout are thermal dissipation and electrical isolation.

For optimum thermal dissipation, it is recommended to use a PCB copper layer thickness of 4.0 oz and above on both sides and internal layers, if any. Wide current carrying tracks, reinforced with thermal vias are recommended to minimize thermal resistance. Thermal vias create a low thermal resistance path between the PCB copper layers (Figures 11 and 13).

The integrated current carrying lead frame in the CT43x causes

self-heating which can affect overall performance if not managed. Device failure can occur if its junction temperature (T_j) exceeds 155°C. This PCB is designed to have a minimal thermal resistance for dissipating the heat generated within the CT43x current sensor.

An isolated module voltage is required on the digital logic side. The high-voltage GND must be completely isolated from the low-voltage GND. Any potential between these two grounds (caused by low-end power supplies) may result in wrong measurements.

Depending on the maximum sensed voltage, a creepage of a few to 10 mm may be needed between the high-side (current conducting circuitry) and the low side (digital outputs).

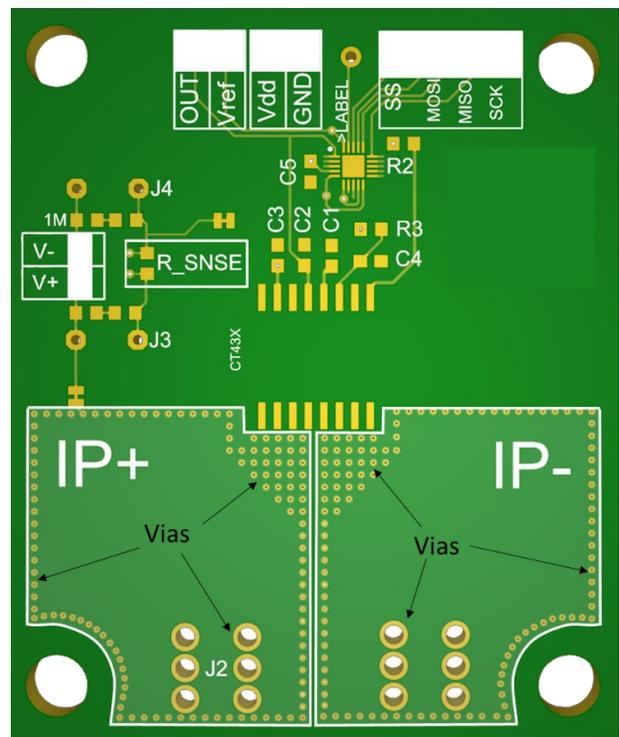


Figure 11: Power meter PCB Thermal Vias

BILL OF MATERIALS (BOM)

The module uses surface mount components to maintain a small profile. This is shown in the PCB module BOM, Table 7.

The recommended decoupling and filtering capacitors are explained in the CT43x datasheet. Only two (2) CT43x differential outputs, OUT and VREF pins, are connected to the ATtiny microcontroller. The step-down resistive circuit consists of four (4) 1.0 MΩ resistors for providing an isolated voltage measurement across the R_{SNSE} resistor. See Figure 12, the Power Meter Module schematic diagram.

CONCLUSION

The power meter module is a usage example for the CT430 TMR current sensor. When the module is placed in line with a load circuit, the on-board ATtiny426 reads both load current and voltage to calculate and store multiple power values. These values are accessible to an external micro via the SPI bus to enable additional calculations and reporting capabilities.

Table 7: PCB Module BOM

Part	Value	Device	Package	Description
1M	1.0 MΩ	R-EU_R0603	R0603	RESISTOR
1M_1	1.0 MΩ	R-EU_R0603	R0603	RESISTOR
1M_3	1.0 MΩ	R-EU_R0603	R0603	RESISTOR
1M_4	1.0 MΩ	R-EU_R0603	R0603	RESISTOR
C1	100 pF	C-EUC0603	C0603	CAPACITOR
C2		C-EUC0603	C0603	CAPACITOR
C3	1.0 μF	C-EUC0603	C0603	CAPACITOR
C4	1.0 nF	C-EUC0603	C0603	CAPACITOR
C5	1.0 μF	C-EUC0603	C0603	CAPACITOR
CT43x		CT430_CT430_SOI6_WIDE	CT430_SO16DW	CT430 Integrated Current Sensor
IC2	ATTINY426-MU	ATTINY426-MU	QFN40P300X300X90-21N	8-bit Microcontrollers - MCU 20 MHz
J1	7461057	7461057	7461057	PCB power element bush terminal
J2	7461057	7461057	7461057	PCB power element bush terminal
J3	J5MM	J5MM	5	Bridge
J4	J5MM	J5MM	5	Bridge
JP1		PINHD-1X2	1X02	PIN HEADER
JP2		PINHD-1X2	1X02	PIN HEADER
R2	10 kΩ	R-EU_R0603	R0603	RESISTOR
R3	100 kΩ	R-EU_R0603	R0603	RESISTOR
R_SNSE	8.2 kΩ	R-EU_R0603	R0603	RESISTOR
SV1		MA04-1	MA04-1	PIN HEADER
UPDI	TESTPOINT_TPS-PAD-036	TESTPOINT_TPS-PAD-036	TESTPOINT_PAD-036	TEST POINT PAD
V+	TESTPOINT_TPS-PAD-036	TESTPOINT_TPS-PAD-036	TESTPOINT_PAD-036	TEST POINT PAD
V-	TESTPOINT_TPS-PAD-036	TESTPOINT_TPS-PAD-036	TESTPOINT_PAD-036	TEST POINT PAD
VINN1	JUMPER-SMT_2_NC_TRACE_SILK	JUMPER-SMT_2_NC_TRACE_SILK	SMT-JUMPER_2_NC_TRACE_SILK	Normally closed trace jumper
VINN2	JUMPER-SMT_2_NC_TRACE_SILK	JUMPER-SMT_2_NC_TRACE_SILK	SMT-JUMPER_2_NC_TRACE_SILK	Normally closed trace jumper

PCB LAYOUT AND VIAS

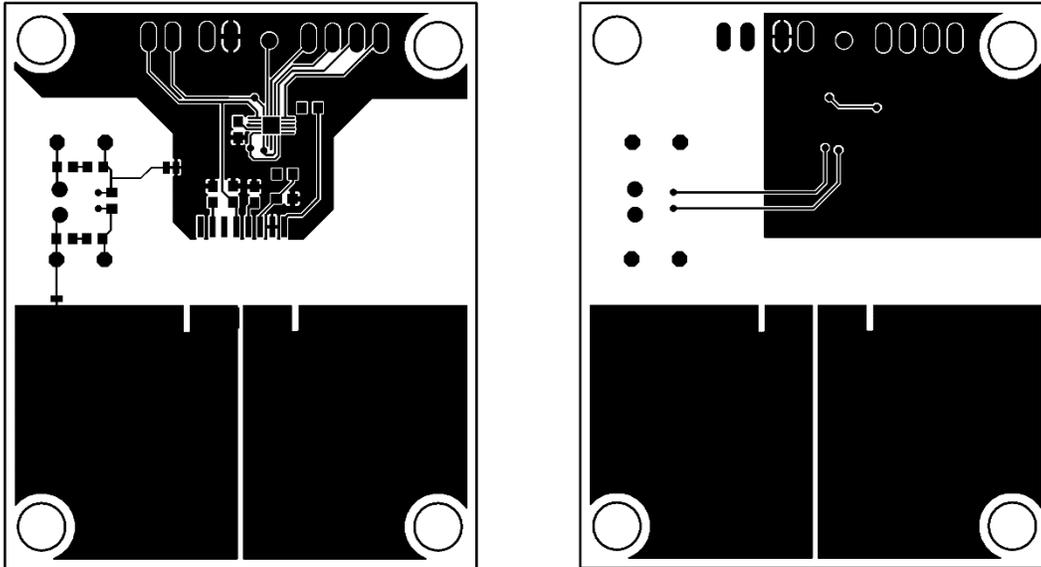


Figure 13: Top and bottom PCB layout

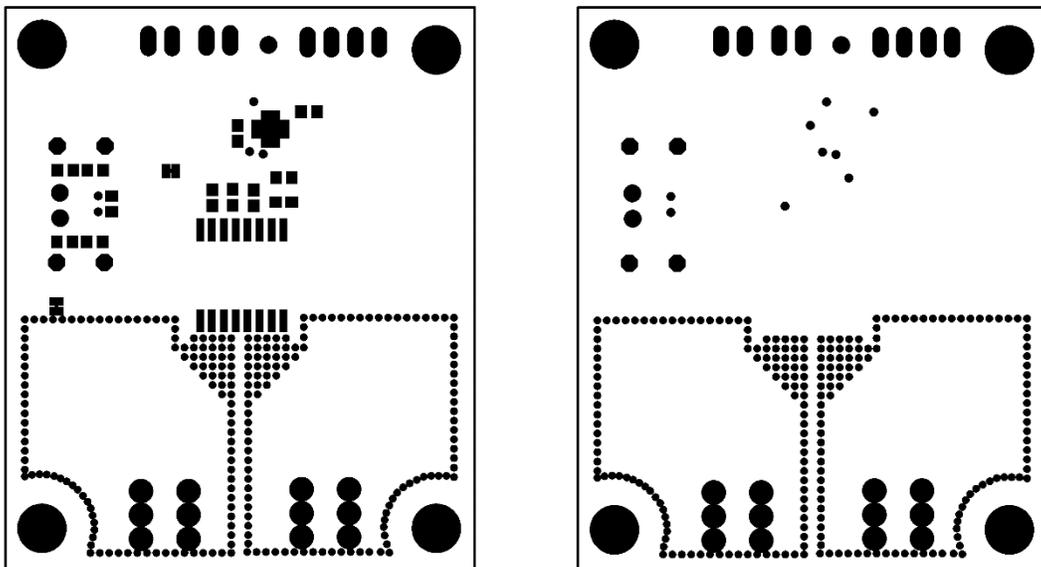


Figure 14: Top and bottom Via placement

Revision History

Number	Date	Description	Responsibility
1	December 18, 2023	Document rebrand and minor editorial updates	Tyler Hendrigan

Copyright 2023, Allegro MicroSystems.

The information contained in this document does not constitute any representation, warranty, assurance, guaranty, or inducement by Allegro to the customer with respect to the subject matter of this document. The information being provided does not guarantee that a process based on this information will be reliable, or that Allegro has explored all of the possible failure modes. It is the customer's responsibility to do sufficient qualification testing of the final product to ensure that it is reliable and meets all design requirements.

Copies of this document are considered uncontrolled documents.