Application Information

Increasing System Safety using the A1365 Programmable Linear Hall-Effect Sensor IC with Self-Test Diagnostic Mode

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Abstract

This application note provides guidelines for implementing the Self-Test Diagnostic mode on the A1365 from Allegro MicroSystems in order to verify system functionality and safety in the application. To learn more about the A1365 from Allegro MicroSystems, refer to the device's datasheet at www.allegromicro.com.

Introduction

The advent of Automotive Safety Levels has spurred an increase in safety requirements, making IC and sensor safety features as important as the target performance specifications in some applications. As safety goals multiply throughout the system design process, customers demand smart sensors that can be used to diagnose abnormalities in a system. The built-in Self-Test mode of the A1365 grants users such insight into their systems.

The Self-Test mode on the A1365 covers the entire signal path, from the analog output (V_{OUT}) and $\overline{FAULT}$ output pins up to the connections to the Hall transducer.

Refer to the block diagram of the A1365 in Figure 1 which highlights the injection point of the on-chip test voltage in green.

The A1365's Self-Test mode allows the user to verify, at any point, connectivity of the analog signal path, drifts in quiescent output voltage, as well as connectivity and functionality of the Over Field Fault signal path. By comparing the voltages and various timings measured during the Self-Test mode, the user can also evaluate the integrity of any external devices, including system ADCs and overcurrent fault control devices. The Self-Test Fault feature simplifies end-of-line verification of overcurrent fault circuitry external to the A1365 without the burden of injecting large full-scale currents.

The Self-Test mode is intended to reveal gross single point failures in the Hall path, but does not test the sensitivity of the Hall transducer itself.

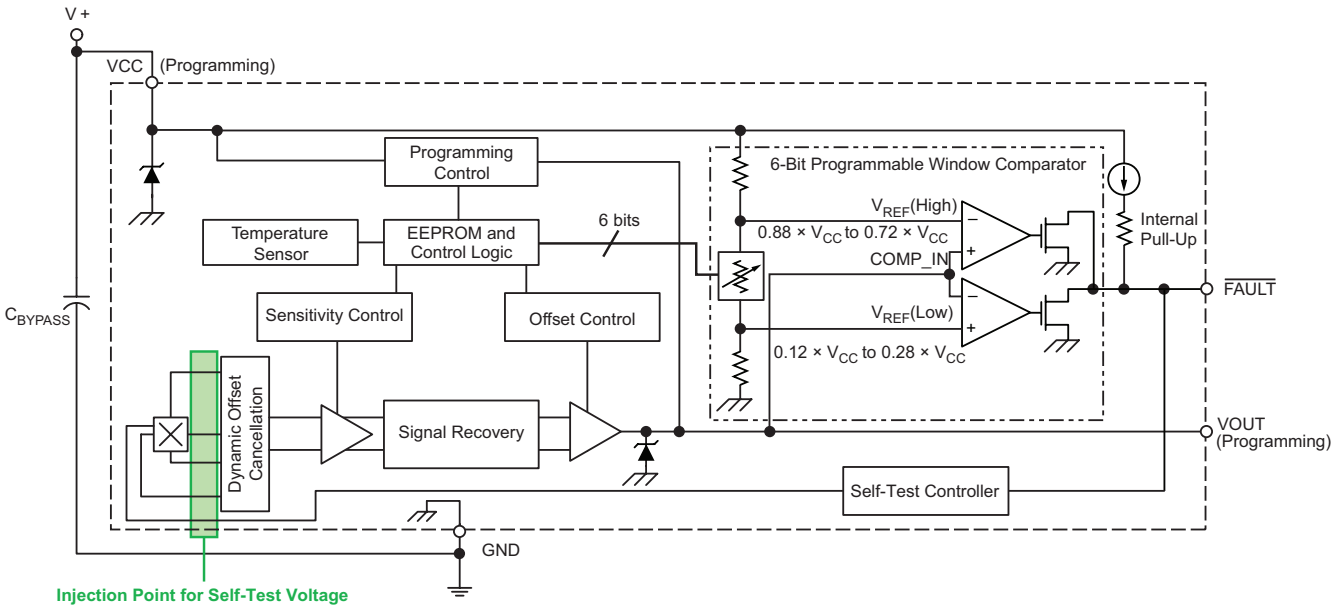

Figure 1: A1365 Functional Block Diagram

Enabling the Self-Test Mode

The Self Test feature is disabled in all sales versions of the A1365 IC. However, the test mode is easy to enable using the Allegro A1365 Samples Programmer and an ASEK evaluation board.

The A1365 Samples Programmer is available on Allegro's software portal at https://registration.allegromicro.com. Contact your sales representative for information on acquiring an ASEK evaluation kit.

To enable the Self-Test mode on the A1365, power-on the device by pressing the "Power On" button [1] on the A1365 Samples Programmer shown in Figure 2. Confirm that the device is operational by verifying V_{CC}, I_{CC}, and Output values are reading as expected using the "Update" button [2].

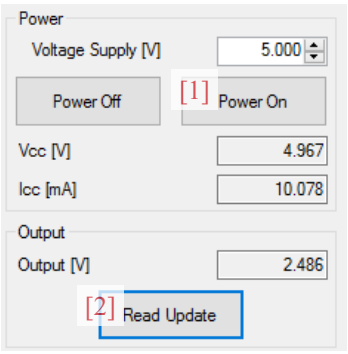

Figure 2: Power Panel from the A1365 Samples Programmer

The "Memory" panel on the programmer displays all available registers on the A1365 device, along with a brief description of each register's function [3]. Refer to Figure 3 for more information.

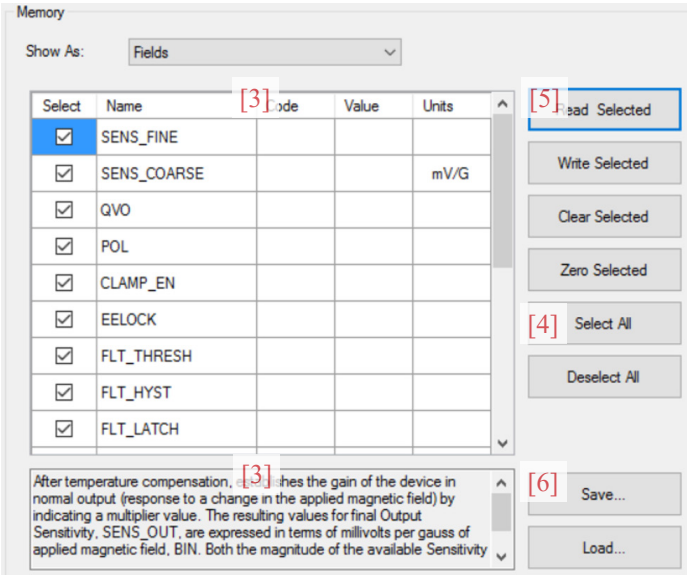

Figure 3: Memory Panel from the A1365 Samples Programmer

Choose the "Select All" button [4], followed by the "Read Selected" button [5], which will read back the memory contents of the device and populate the code and value columns with the returned data. Prior to making any changes to the device's memory, it is best practice to save a local copy of the EEPROM contents to revert back to. Choose the "Save" button [6] to generate either a .csv or .txt file for safekeeping.

To enable the Self-Test mode, refer to Figure 4. Scroll down to the field "ST_DIS" (self-test disable) [7], choose the "Deselect All" button [8], then select only the "ST_DIS" field using the checkbox.

Set the "ST_DIS" code column to "0" by typing "0" into the cell, or choosing the "Zero Selected" button [9] on the GUI. When ready, press the "Write Selected" button [10] to write the new value to EEPROM. It is best practice to read back the same register to verify the change. Choose "Read Selected" [11] to confirm the "ST_DIS" bit has been cleared. The Self-Test mode is now enabled.

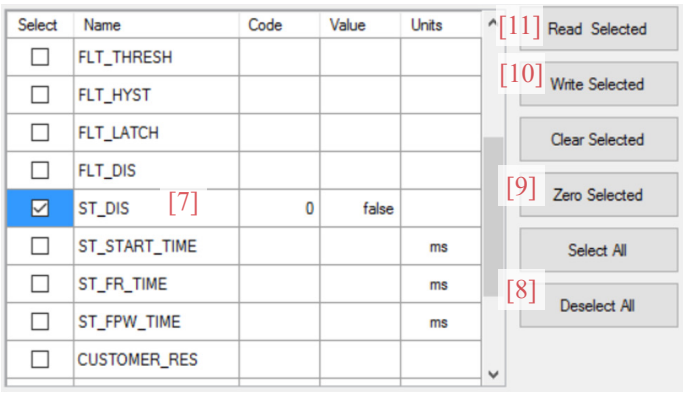

Figure 4: Self-Test Enable from the A1365 Samples Programmer

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Initiating the Self-Test Mode

Once enabled, the Self-Test mode may be initiated by pulling the A1365's $\overline{\text{FAULT}}$ pin low. The device does not enter the Self-Test mode immediately; the $\overline{\text{FAULT}}$ pin must be held low for a time period greater than the "Self-Test Start Time" to enter the Self-Test diagnostic mode. The Self-Test Start Time is programmable and is designated in the programming field "ST_START_TIME". There are sixteen codes which correspond to twelve discrete Start Time values.

The available codes for Self-Test Start Time and their corresponding time delays are listed in Table 1.

Table 1: Self-Test Start Time Codes and Timing

ST_START_TIME Code (decimal)	Self-Test Start Time (ms)
0	0.05
1	0.1
2	0.2
3	0.5
4	1
5	2
6	5
7	10
8	20
9	50
10	100
11-15 [a]	200

[a] Start Time Codes 11 through 15 are equivalent.

Self-Test Start Time is defined from when the $\overline{\text{FAULT}}$ pin voltage ($V_{\overline{\text{FAULT}}}$) falls below the Self-Test Threshold Voltage (V_{STTH}) until the sensor enters the Self-Test Sense mode. The sensor enters Self-Test Sense mode by driving the analog output to Self-Test Low Voltage (V_{STL}). If at any point during Self-Test Start Time the sensor detects a magnetic input exceeding the programmed fault threshold, the Self-Test timer will reset.

The plot in Figure 5 shows the time for V_{OUT} to reach V_{STL} after the $\overline{\text{FAULT}}$ pin is pulled low for all Self-Test Start Time codes on the A1365.

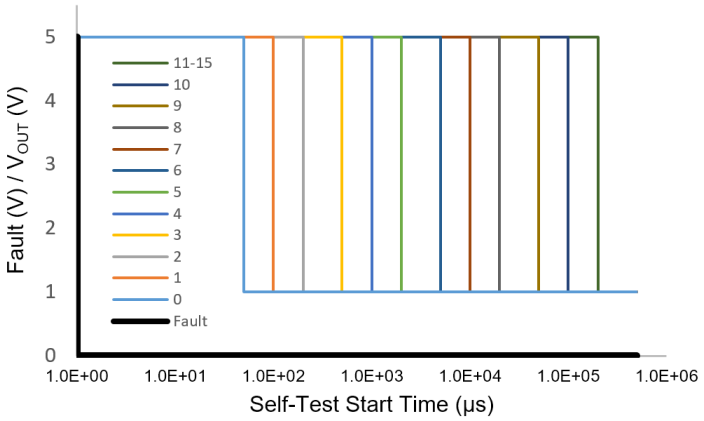

Figure 5: Self-Test Start Time for all Codes

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Self-Test Fault Request Time

Self-Test Fault Request mode allows the user to verify the user-programmed fault thresholds on the A1365. The device will enter Self-Test Fault mode after the $\overline{\text{FAULT}}$ pin is released for a time longer than Self-Test Fault Request Time (ST_FR_TIME). After the pin is released, but prior to Self-Test Fault Request time expires, the output is driven to Self-Test High Voltage (V_{STH}). As the device enters Self-Test Fault Request Mode, the output of the device is driven to saturation ($V_{SAT(HIGH)}$).

The available codes for Self-Test Fault Request Time (ST_FR_TIME) and their corresponding delays are listed in Table 2.

Table 2: Self-Test Fault Request Time Codes and Timing

ST_FR_TIME Code (decimal)	Self-Test Fault Request Time (ms)
0	0.05
1	0.1
2	0.2
3	0.5
4	1
5	2
6	5
7	10

In Self-Test Fault mode, the A1365 will drive V_{OUT} into saturation, both $V_{SAT(H)}$ and $V_{SAT(L)}$. When V_{OUT} crosses the user-programmed fault thresholds (FLT_THRESH), the sensor's $\overline{\text{FAULT}}$ pin will assert to indicate a fault condition. Note that this mode temporarily disables the clamps if the clamps are enabled.

Self-Test Fault Pulse Width Time

The A1365 will drive and hold V_{OUT} to each test voltage for a period defined by Self-Test Fault Pulse Width Time (ST_FPW_TIME). The available codes for Self-Test Fault Pulse Width Time and their corresponding pulse width times are listed in Table 3.

Table 3: Self-Test Fault Request Time Codes and Timing

ST_FPW_TIME Code (decimal)	Self-Test Fault Pulse Width Time (ms)
0	0.05
1	0.1
2	0.2
3	0.5
4	1
5	2
6	5
7	10

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Complete Self-Test Mode Sequence

The entire Self-Test mode sequence is shown in Figure 6. The applied magnetic field during the Self-Test Mode must be zero.

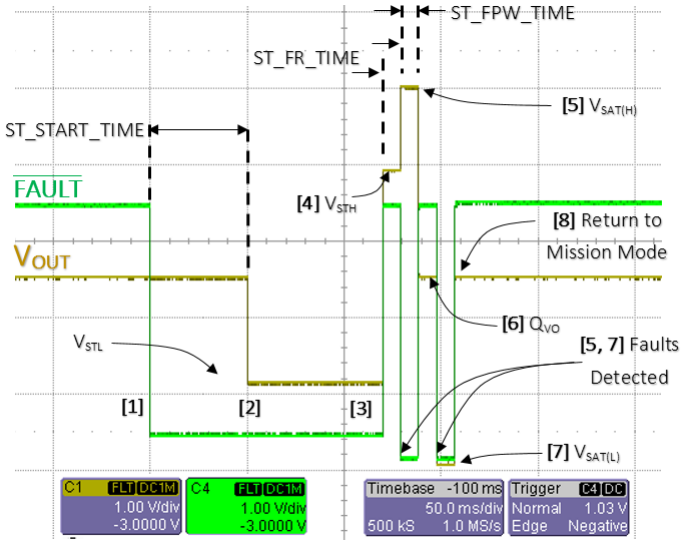

Figure 6: Self-Test Mode Sequence

For the case in Figure 6, ST_START_TIME = 50 ms, ST_FR_TIME = 10 ms, and ST_FPW_TIME = 10 ms. The Self-Test and Magnetic Fault settings are shown in Figure 7.

Select	Name	Code	Value	Units
☑	FLT_THRESH	0	0	
☑	FLT_HYST	0	0	
☑	FLT_LATCH	0	false	
☑	FLT_DIS	0	false	
☑	ST_DIS	0	false	
☑	ST_START_TIME	9	50	ms
☑	ST_FR_TIME	7	10	ms
☑	ST_FPW_TIME	7	10	ms

Figure 7: Self-Test and Fault Settings for the Sequence in Figure 6

The Self-Test sequence is described in the list below. Each step corresponds to a point in time on the plot in Figure 7.

1. The A1365's $\overline{\text{FAULT}}$ pin is pulled low externally to initiate the Self-Test mode. The A1365 would still properly respond to magnetic fields at this time.
2. The device enters Self-Test Sense mode after ST_START_TIME and drives V_{OUT} to V_{STL}.
3. V_{OUT} remains at V_{STL} until the $\overline{\text{FAULT}}$ pin is released.
4. V_{OUT} is driven to V_{STH} for the duration of Self-Test Fault Request Time, ST_FR_TIME.
5. The device enters Self-Test Fault Request mode and V_{OUT} is driven to $V_{SAT(H)}$ for ST_FPW_TIME and the $\overline{\text{FAULT}}$ pin is asserted.
6. V_{OUT} is driven to QVO for ST_FPW_TIME (10 ms) and the $\overline{\text{FAULT}}$ pin resets.
7. V_{OUT} is driven to $V_{SAT(L)}$ for ST_FPW_TIME (10 ms) and the $\overline{\text{FAULT}}$ pin is asserted.
8. The Self-Test Sequence is complete and the device returns back to normal operation (mission mode).

Application Case

The Self-Test mode on the A1365 may be used to verify gross anomalies and single point failures on the A1365 device. This feature may also be used to confirm the integrity and timing of other system devices, including ADCs and fault control circuitry. The application schematic in Figure 8 shows such a system.

The A1365 is installed in the gap of a laminated core and is used to sense magnetic field generated by current flow in a conductor. The analog output, V_{OUT}, is connected to an ADC while the $\overline{\text{FAULT}}$ pin is connected to a general purpose I/O pin on the microcontroller. Assume the I/O-connected $\overline{\text{FAULT}}$ pin signals a system interrupt in the event of an overcurrent condition. This interrupt prompts the microcontroller to put the system in a safe state by disconnecting current flow in the conductor.

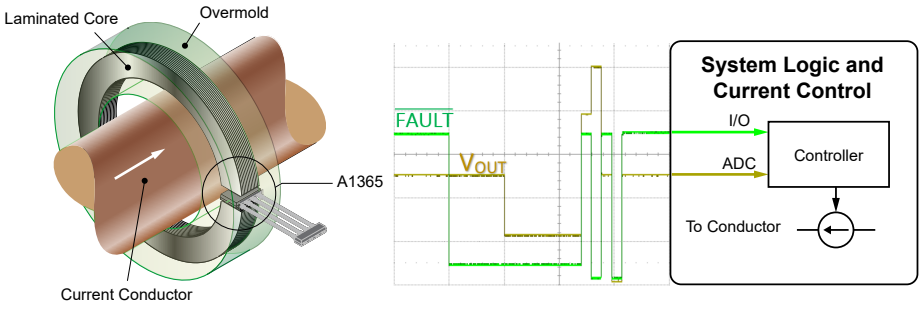

Figure 8: Application Schematic with A1365, ADC, and Overcurrent Fault Control

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Revision History

Number	Date	Description
–	July 5, 2018	Initial release
1	OCtober 7, 2019	Minor editorial updates

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