ESTIMATING MAXIMUM MOSFET SWITCHING FREQUENCY

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Introduction

This application note describes how to calculate the maximum power MOSFET switching frequency in BLDC motor gate drives. While this application note focuses on Allegro three-phase bridge gate drivers with a standard voltage regulator plus bootstrap capacitor architecture, such as the Allegro A4910, A4911, A4913, A4916, and A4918, the concept is generally applicable to other gate driver circuits.

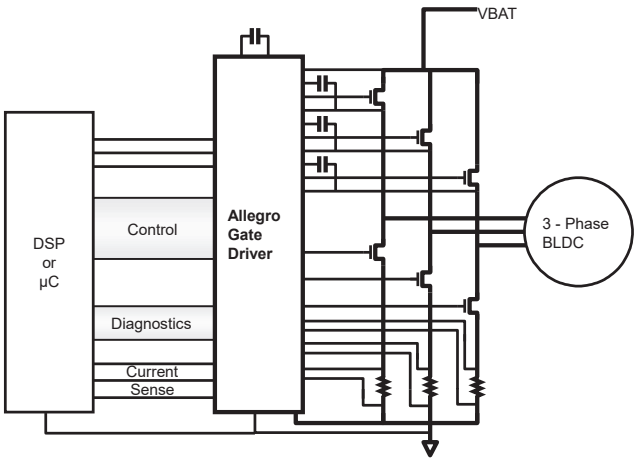

Figure 1: Typical Application

MOSFET Turn-On Voltage Requirement

To hold a MOSFET in the off state, the gate is normally held at a voltage that is close to that of the source ($V_{GS} \ll V_{TH}$).

To turn on a standard N-channel MOSFET, it is necessary to raise the gate voltage to a suitable positive value with respect to the source to generate low $R_{DS(ON)}$. Figure 2 shows a representative plot of $R_{DS(ON)}$ versus V_{GS} for a typical power MOSFET.

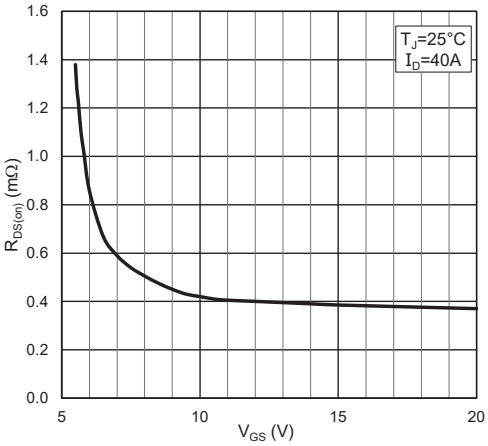

Figure 2: $R_{DS(ON)}$ versus V_{GS}

As can be seen in Figure 2, to achieve low $R_{DS(ON)}$, a V_{GS} of 10 V is typically required, though operation at lower voltages can be supported with only limited increase of $R_{DS(ON)}$.

MOSFET Turn-On/Off Current Requirement

If a power MOSFET gate source voltage is quickly raised from near zero to a sufficient value for MOSFET turn-on, the resultant current waveform is as shown in Figure 3 as "charge current". The current into the MOSFET gate rises very quickly and then decays exponentially as the device input charges up. When the gate source voltage is quickly reduced to close to zero, current flows out of the MOSFET gate in a similar manner as shown as "discharge current" in Figure 3.

When using an Allegro gate driver to turn power MOSFETs on and off, the peak of each current 'spike' can reach 0.5 A or higher. However, the duration of each spike is typically no more than a few hundred nanoseconds.

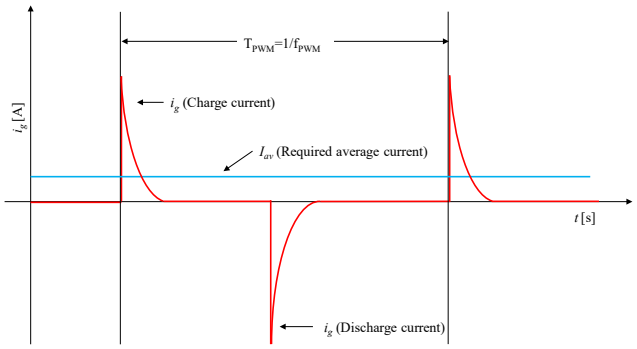

Figure 3: Example gate charge switching current waveform.

The charge represented by the area under each spike is equivalent to the total gate charge, Q_g, of the MOSFET being driven. A representative gate charge versus gate-source voltage characteristic of a MOSFET is shown in Figure 4 below.

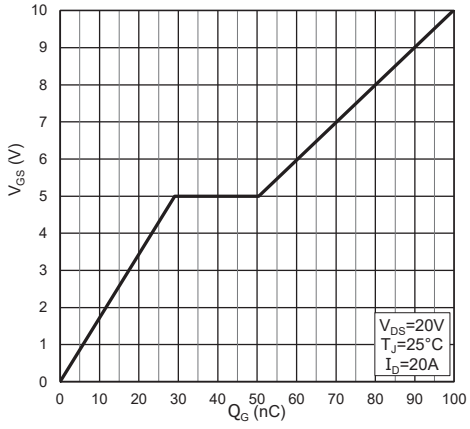

Figure 4: Typical gate charge of MOSFET.

It is possible to calculate the average current that must be provided to continuously switch a MOSFET on and off at a particular frequency. This is effectively the time average of all the positive-going charge current pulses in Figure 3. If the switching frequency is $f_{PWM} = 1 / t_{PWM}$ and the MOSFET gate charge is Q_g, then the average charge current, I_{av} is equal to

Equation 1: $$I_{av} = f_{PWM} \times Q_g$$

If switching multiple MOSFETs, N, per PWM cycle, the average current requirement scales by the number of MOSFETs given.

Equation 2: $$I_{av} = N \times Q_g \times f_{PWM}$$

For example, if the following parameter values representative of driving a three-phase BLDC motor are assumed for illustration: N = 6, Q_g = 123 nC, f_{PWM} = 10 kHz, then the resultant average current from Equation 2 is:

$$I_{av} = 6 \times 123 \text{ nC} \times 20 \text{ kHz} = 14.8 \text{ mA}$$

As can be seen from this result, the average current (tens of mA) is typically small compared to the peak gate driver current delivered on each switching cycle (possibly 0.5 A or higher). This arises because the duration of each switching pulse is short compared to the duration of the period between switching cycles.

Note that the average discharge current is equal in magnitude to the average charge current. This is effectively the time average of all the negative-going charge current pulses in Figure 3.

MOSFET Switching Speed Control

In some applications, it may be necessary to limit the rate of change of the voltage at the motor phase connections to help comply with EMC requirements at the expense of increased MOSFET dissipation.

The conventional method of achieving this is to add an external resistor between the gate drive output and the gate terminal of each MOSFET. This reduces the peak switching current as shown in Figure 3 to increase the time required to deliver/remove gate charge to/from the MOSFETs and slow switching as required.

In addition to operating in this conventional switch mode, many of Allegro's gate drivers can be configured via their serial interface to control gate drive current without an external resistor between the gate drive output and the corresponding MOSFET gate terminal. For further information, consult Allegro gate driver product datasheets. Note that the average current required to support switching is the same regardless of whether external resistors or the internal gate drive control mechanism is used.

Gate Driver Output Current Capability

When using an Allegro gate driver to switch a three-phase bridge comprising six N-channel MOSFETs, the MOSFET gate current is supplied by the VREG output as generated by the gate driver regulator.

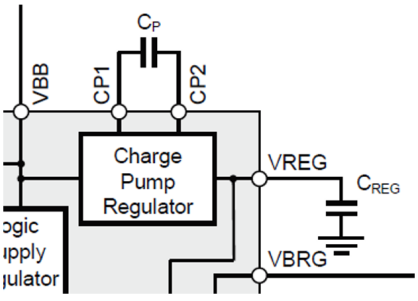

Figure 5: Charge pump regulator

VREG supplies current for the low-side gate-drive circuits and

the charging current for the bootstrap capacitors. When a low-side MOSFET is turned on, the gate drive circuit will provide the high transient current to the gate that is necessary to turn the MOSFET on quickly. This current, which can be several hundred milliamperes, cannot be provided directly by the limited output of the VREG regulator but must be supplied by an external capacitor, C_{REG}, connected between the VREG terminal and GND.

The turn-on current for the high-side MOSFET is similar in value but is mainly supplied by the bootstrap capacitor. However, the bootstrap capacitor must then be recharged from C_{REG} through the VREG terminal. Unfortunately, the bootstrap recharge can occur a very short time after the low-side turn-on occurs. This means that the value of C_{REG} between VREG and GND should be high enough to minimize the transient voltage drop on VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge.

For block commutation control (trapezoidal drive) where only one high side and one low side are switching during each PWM period, a minimum value of $20 \times C_{BOOT}$ is reasonable. For sinusoidal control schemes, a minimum value of $40 \times C_{BOOT}$ is recommended. As the maximum working voltage of C_{REG} will never exceed V_{REG}, the capacitor voltage rating can be as low as 15 V. However, it is recommended that a capacitor rated to at least twice the maximum working voltage should be used to reduce any impact operating voltage may have on capacitance value. For best performance, C_{REG} should be ceramic rather than electrolytic. C_{REG} should be mounted as close to the VREG terminal as possible.

For the gate driver, the continuous current that this charge pump is able to produce is detailed in the Electrical Characteristics section of the relevant product datasheet.

Example 1

It is sometimes the case that system designers are required to determine if a particular gate driver IC can support the switching of a three-phase bridge comprising MOSFETs of a particular type at a specified PWM frequency. This can be translated into determining if the VREG regulator of the gate driver in question (see Gate Driver Output Current Capability section) can provide sufficient continuous current to supply the average current requirement for bridge switching (see MOSFET Turn-On/Off Current Requirement section) while maintaining a sufficient value of V_{REG} at the system minimum V_{BB}.

For example, assume that the system minimum V_{BB} is 6 V, the maximum required PWM frequency is 20 kHz, the selected bridge MOSFETs each have a total gate capacitance, Q_g, of 200 nC(max) at V_{GS} = 10 V, and that sinusoidal drive is being used (N = 6). The average current that must be provided by the regulator can be determined directly from Equation 2:

$$I_{av} = N \times Q_g \times f_{PWM}$$
$$I_{av} = 6 \times 200\ nC \times 20\ kHz$$
$$= 24\ mA$$

By inspection of Figure 6, it can be seen that the regulator will maintain a minimum V_{REG} of 7.9 V with a V_{BB} supply voltage down to 6 V while supporting a load current I_{VREG} of up to 50 mA. If a minimum V_{REG} of 7.9 V is acceptable [1], then the gate driver in question will support switching of the proposed MOSFETs at the specified frequency.

In practice, this calculation can be considered conservative for two reasons. First, the limit value of V_{REG} read from Figure 6 assumes a load current, I_{VREG} of 50 mA. As the estimated current requirement from Equation 2 is actually 24 mA, the minimum V_{REG} will be higher than the stated value of 7.9 V. Second, as the value of V_{REG} may be less than 10 V, the actual gate charge required to turn on the selected MOSFET type may be less than the specified figure of 200 nC. This would lead to a value of average current of less than 24 mA from Equation 2.

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VREG Output Voltage, VRG = 1	V_{REG}	V_{BB} > 9 V, I_{VREG} = 0 to 50 mA	9	11	11.7	V
		7.5 V < V_{BB} ≤ 9 V, I_{VREG} = 0 to 50 mA	9	11	11.7	V
		6 V < V_{BB} ≤ 7.5 V, I_{VREG} = 0 to 50 mA	7.9	11	11.7	V
		4.5 V < V_{BB} ≤ 6 V, I_{VREG} < 15 mA	7.5	8	11.7	V

Figure 6: Example VREG Output Voltage Specification (A4918)

Example 2

It is sometimes the case that system designers are required to estimate the maximum possible three-phase bridge switching frequency when running from a particular minimum supply voltage.

For example, assume that the system minimum V_{BB} is 9 V, the regulator has the VREG output capability shown in the datasheet extract in Figure 6, the selected bridge MOSFETs each have a Q_g of 200 nC(max) at V_{GS} = 10 V, and that sinusoidal drive is being used (N = 6). By inspection of Figure 6, it can be seen that the regulator will maintain a minimum V_{REG} of 9 V [1] with a load current of up to 50 mA. By rearranging Equation 2, maximum switching frequency can then be

[1] Note that voltage drops due to bootstrap diode and gate driver output stage drops should be accounted for when determining the acceptability of minimum V_{REG}.

estimated as:

$$f_{PWM(max)} = I_{av} / (N \times Q_g)$$
$$= 50 \text{ mA} / (6 \times 200 \text{ nC})$$
$$= 41 \text{ kHz}$$

In practice, this calculation can be considered conservative as the MOSFET Q_g is specified at V_{GS} = 10 V, whereas the regulator is only guaranteed to maintain V_{REG} at 9 V. Consequently in the limiting case the gate charge delivered to turn on each MOSFET will actually be 9/10 × 200 nC = 180 nC and the estimated maximum switching frequency will be 46 kHz.

Summary

The relationship between gate driver voltage regulator capability and MOSFET switching has been outlined. This may be used to determine if a particular gate driver IC can switch a given MOSFET type at a required PWM frequency (Example 1). Alternatively, it may be used to determine the maximum achievable PWM frequency for a given gate driver supply voltage and MOSFET type (Example 2).

Revision History

Number	Date	Description	Responsibility
–	November 19, 2020	Initial release	S. Ehara, A. Wood, A. Foletto

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