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AMT49100 AND AMT49101: HOW TO ENABLE/DISABLE THE BUCK REGULATOR

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INTRODUCTION

This application note describes how to switch between buck-enabled and buck-disabled operation on any variant of the AMT49100 or AMT49101 gate driver family.

In buck-enabled mode, an external diode and inductor, D and L respectively, must be connected as shown in Figure 1. A single unregulated supply of 10 to 80 V is applied to VBB, and the buck converter produces a regulated output voltage on the VREG terminal. VBB is typically connected to VBRG via a reverse voltage blocking diode as indicated.

In buck-disabled mode, VBB and VREG are both connected to an externally regulated 12 V (nominal) supply [1] and the external diode and inductor, D and L, need not be fitted, as shown in Figure 2. In this case, the VREG terminal acts as an input to the device rather than an output. The voltage at the VBAT terminal may vary over its full range of 4.5 to 80 V in this configuration.

HOW TO ENABLE/DISABLE THE BUCK REGULATOR

When a device is configured to power-up in buck-enabled mode, the BRE bit in serial register 7 (System) is set to 1 as part of the automatic initialization sequence. If a device is configured to power up in buck disabled mode, the BRE bit is set to 0 as part of the automatic initialization sequence.

It is possible to reconfigure any device for buck-enabled or buck-disabled operation. This is achieved by writing the required state to the BRE bit in register 7 (BRE = 0 for buck disabled, BRE = 1 for buck enabled) and then carrying out a non-volatile memory (NVM) write operation to save it to the device non-volatile storage. The new buck configuration is not applied immediately but only after device power is cycled off and then on again. The power supply applied to the VBRG terminal must comply with the timing and voltage limits, t_{PRS} and V_{PP}, specified in the product datasheet to allow an NVM write to take place.

Device damage does not occur if attempting to run in buck-disabled mode (Figure 2) with external D and L fitted or attempting to run in buck-enabled mode (Figure 1) with external D and L not fitted.

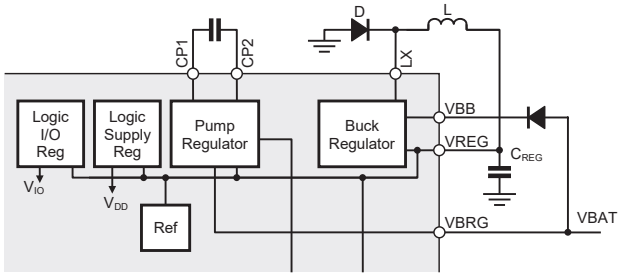

Figure 1: Buck enabled

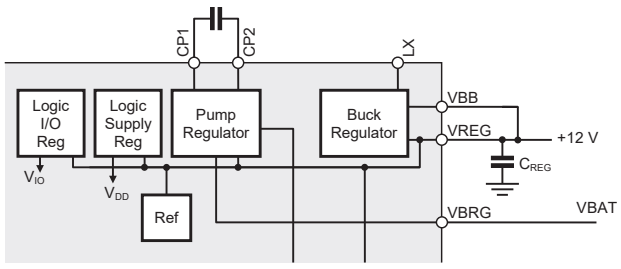

Figure 2: Buck disabled

The following sections describe the procedures necessary to switch between buck modes.

[1] Consult datasheet electrical characteristics table for voltage limits.

CHANGE FROM DISABLED TO ENABLED

The device is in buck-disabled (externally regulated supply) mode with the architecture shown in Figure 2. To enable the buck regulator, follow the instructions below:

1. Power-on AMT49100 by applying VBB, VREG, and VBRG.
2. Ensure VBRG voltage is more than V_{PP} as specified in the product datasheet electrical characteristics table.
3. Wait for Programming Supply Setup Time, t_{PRS}.
4. Change the value of BRE from 0 to 1 by writing to register 7 (See Table 1).
5. Change the value of SAV[1:0] from [01] to [10] in a single write to register 16 (See Table 1).
6. Wait until the save sequence is complete (this takes typically 400 ms).
7. Read register 16 to confirm that the NVM write has been successful (SAV[1:0] is set to 01 after a successful write and 00 after an unsuccessful write).
8. Power-off AMT49100 by removing the externally supplied VBB, VREG, and VBRG.
9. Change the architecture to that shown in Figure 1.
10. Power-on AMT49100 by applying VBB and VBRG.
11. Read register 7 to confirm BRE = 1 and check to see that the voltage on VREG is within the regulator active datasheet limits.
12. At this point, the device is programmed to buck-enabled mode.

CHANGE FROM ENABLED TO DISABLED

The device is in buck-enabled mode with the architecture shown in Figure 1. To disable the buck regulator, follow the instructions below:

1. Power-on AMT49100 by applying VBB and VBRG.
2. Ensure VBRG voltage is more than V_{PP} as specified in the product datasheet electrical characteristics table.
3. Wait for Programming Supply Setup Time, t_{PRS}.
4. Change the value of BRE from 1 to 0 by writing to register 7 (See Table1).
5. Change the value of SAV[1:0] from [01] to [10] in a single write to register 16 (See Table 1).
6. Wait until the save sequence is complete (this takes typically 400 ms).
7. Read register 16 to confirm that the NVM write has been successful (SAV[1:0] is set to 01 after a successful write and 00 after an unsuccessful write).
8. Power-off AMT49100 by removing the externally supplied VBB and VBRG.
9. Change the architecture to that shown in Figure 2.
10. Power-on AMT49100 by applying VBB, VREG, and VBRG.
11. Read register 7 to confirm BRE = 0.
12. At this point, the device is programmed to buck-disabled (externally regulated supply) mode.

Table 1: Serial Register Reference

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
7: System	0	0	1	1	1	WR	VIO	VCL	BRE	CPM1	CPM0	DSR		DG1	DG0	P
							0	0	0/1†	0	0	0	0	0	0	
16: NVM Write	1	0	0	0	0	WR	SAV1	SAV0								P
							0	0	0	0	0	0	0	0	0	

*Power-on reset value shown below each input register bit.

† Factory-set power-on-reset value of BRE is selected by part number:
AMT49100KJPTR-A-3, AMT49100KJPTR-A-5: BRE = 1, Buck Enabled.
AMT49100KJPTR-B-3, AMT49100KJPTR-B-5: BRE = 0, Buck Disabled.

Revision History

Number	Date	Description	Responsibility
–	November 9, 2020	Initial release	S. Ehara, A. Wood
1	October 31, 2024	Minor editorial updates	R. Couture

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