KEY CONSIDERATIONS IN DESIGN OF SENSORLESS THREE-PHASE BLDC MOTOR DRIVER FOR AUTOMOTIVE FUEL PUMPS

By Vashist Bist and Shashank Wekhande, Systems Engineers
Allegro MicroSystems

INTRODUCTION

An automotive fuel pump is the part of a fuel delivery system that pumps fuel, at a specified pressure and flow rate, to the engine through additional components, such as filters. The predominantly used brushed DC motors suffer from sparking, noise, electromagnetic interference (EMI), and low efficiency, which result from brushes and commutators. Newer designs eliminate problems related to brushes—such as wear and tear, noise, EMI, and sparking—using brushless DC (BLDC) motors in the fuel pump assembly.

BLDC motors are highly efficient, offer a higher torque/inertia ratio, and are capable of integrating a closed-loop speed control to improve fuel consumption and reduce CO_2 emission. Moreover, incorporation of an integrated controller enables diagnostics for health monitoring of the motor module, and sensorless algorithms in the BLDC motor module can eliminate noise on the Hall position sensors.

A fuel-pump subsystem in which the integrated fuel module provides the required fuel flow to the engine unit is shown in Figure 1. The engine performance is monitored by the electronic control unit (ECU) and, based on the speed/load demand, the ECU provides signals to the fuel module controller. This fuel module controller provides pulse-width-modulated (PWM) signals to the integrated fuel module, which includes the motor driver and the fuel pump. [1] The fuel controller module also monitors the status of the integrated fuel module via various diagnostics features.

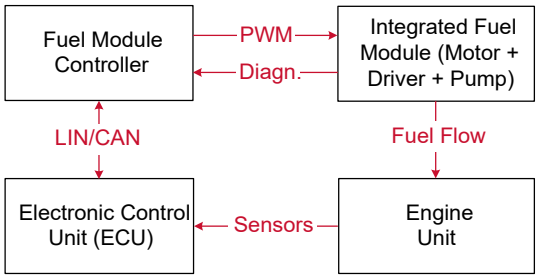

Figure 1: Fuel Pump Subsystem

The startup performance of the BLDC motor is a very important criterion to quickly deliver the fuel in a kick-start system. The Allegro A89303 is such a three-phase motor driver that uses a sensorless algorithm that results in startup to full speed in 50 ms, making kick-starters easier for users to operate. [2]–[4]

The A89303 is a highly integrated sensorless BLDC (trapezoidal) motor driver that in-houses a low on-state resistance ($R_{DS(on)}$) MOSFET power stage, integrated charge pump, inter-integrated circuit (I2C) communication block set, in-built protection schemes, and many advanced features to improve the overall efficacy of the motor drive.

This application note provides details the A89303 device in an automotive fuel pump application. Detailed information about the sensorless control in A89303, advantages of the device, speed control techniques, parameter configuration including efficacy and thermal calculation, EMI consideration, and layout guidelines are presented.

[1] D. Collins, P. Anderson, S. Beyer and D. Moreno, "Brushless Motors for In-Tank Fuel Pumps," SAE Technical Paper, no. 2012-01-0426, 2012.
[2] A89303: Sensorless BLDC Pump Driver with Ultra-Fast Start-Up for Fuel Delivery Systems, Allegro Microsystems datasheet, Rev. 1, March 2021; see https://www.allegromicro.com/en/products/motor-drivers/bldc-drivers/a89303.
[3] A89303 Application Note, Allegro Microsystems Application Information.
[4] A89303 Programming GUI, Allegro Microsystems Programming Application, ver. 0.21.

SENSORLESS CONTROL OF BLDC MOTOR

The A89303 is equipped with sensorless trapezoidal control of the BLDC motor. The key differences between the sensored and sensorless control is:

- In sensored BLDC motor control, Hall-effect position sensors are used to sense the rotor position at 60 degrees of resolution. This data is used to achieve electronic commutation of the BLDC motor.
- In sensorless control, position data is extracted via the back-electromagnetic force (emf) of the BLDC motor, which is achieved by sensing the voltage of the nonexcitation phase.

The three phases of a BLDC motor are illustrated in Figure 2, which shows phase voltage (blue), back-emf (black), phase current (red), and six 60-degree sectors (S1 – S6) in a complete electrical cycle. As shown in this figure, for every half cycle (180 degrees), each phase conducts for the first 120 degrees, then is off for the remaining 60 degrees. During the 60-degree window of offtime, the polarity of the back-emf changes, and the phase becomes nonconducting; a trapezoidal back-emf waveform can be observed on the phase node, the zero-crossing of which is used to determine the actual commutation instances, which are then phase-shifted 30 degrees from the zero-crossing point of the back-emf.

The back-emf in a BLDC motor is directly proportional to the speed of the rotor. If the motor is not rotating, the back-emf is zero. This means that, when the rotor is not moving, phase voltage cannot be used to detect rotor position. Motor startup requires an initial open-loop starting pulses of increasing frequency. Once back-emf is detected, the motor algorithm can shift to the sensorless mode.

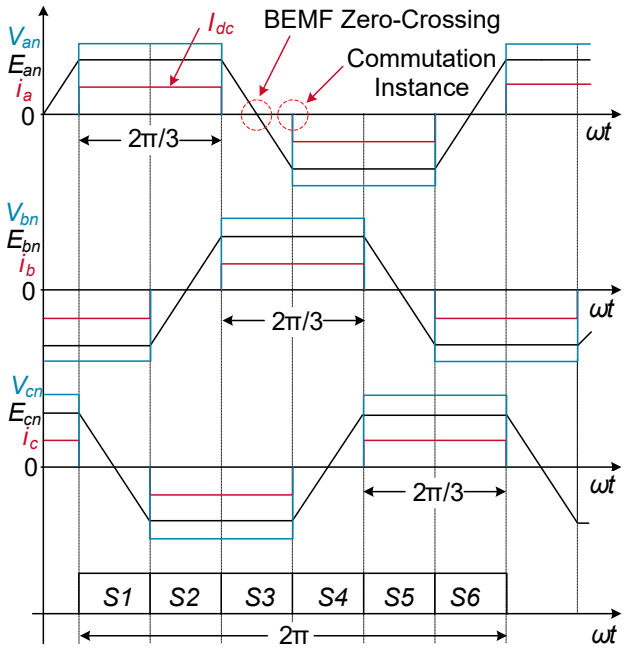

Figure 2: Trapezoidal BLDC Motor Control Waveforms

Application of the open-loop pulses needed for the startup operation requires initial position data to generate the pulse pattern from the known state. Therefore, the position of the rotor must be:

- Aligned to a known position, for instance, by exciting a known phase combination; or
- Estimated using, for instance, an advanced algorithm such as the initial position detection (IPD) algorithm.

The starting sequence of the BLDC motor is shown in Figure 3, which includes the following steps in the sensorless control of a BLDC motor:

1. When the motor-on signal is commanded by the driver, the motor is aligned either to the known position using an alignment algorithm, or the initial position is estimated by the IPD algorithm based on the user configuration. The driver waits for the alignment/IPD algorithm based on the user configuration and signals to the sequencing control unit.
2. Once the alignment/IPD is complete, the sequencing control commands the open-loop start operation. Open-loop pulses of increasing frequency are sent to the BLDC motor, which then starts to rotate in the set direction.
3. The back-emf estimation block begins to detect the back-emf signal. if the detected back-emf signal exceeds the inner threshold value, a command is sent to the sequencing control unit, at which point sensorless control can begin.
4. As soon as the open-loop start operation is complete, control is shifted to the sensorless control mode. The phase measurement and the back-emf estimation block set provide the rotor position data to the sequencing control unit, which generates the necessary sequence for the electronic commutation.

The overall startup waveforms of the BLDC motor are shown in Figure 4. As shown in this figure, the waveforms can be classified into four states—align, startup, open-loop starting, and sensorless closed-loop control.

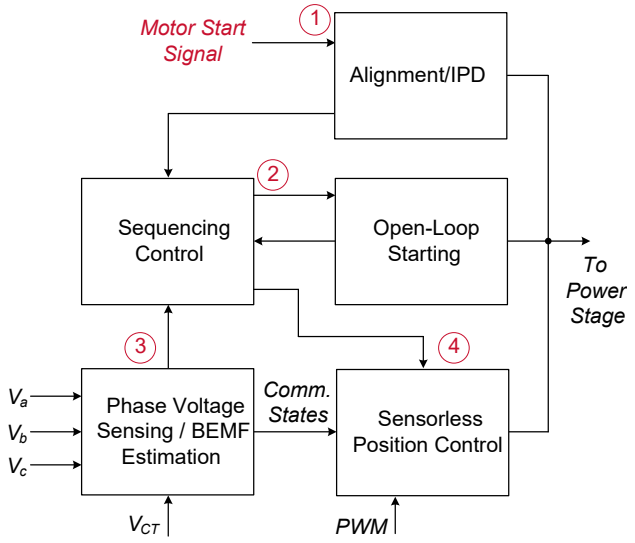

Figure 3: Sensorless Control Block Diagram

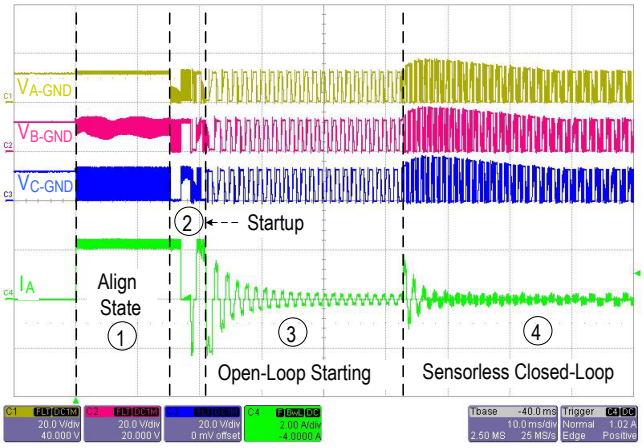

Figure 4: Overall Startup Waveforms

STARTUP TECHNIQUES—ALIGN AND GO

In the conventional align-and-go start method, the rotor is aligned to a fixed position, and open-loop pulses of increasing frequency are applied to increase the speed to a sufficient level for proper back-emf detection. Rotor acceleration is determined by motor inertia:

- For high inertia motors, the acceleration is set low such that the rotor is able to increase in speed.
- For lower inertia motor, the acceleration can be increased to reduce the overall startup time.

  The main advantage of this startup mode is the simplicity and nondependence on motor parameters, such as motor resistance or inductance. However, due to the position alignment, the rotor can move in either direction. Therefore, this startup mode is used in applications that do not require features like zero reverse rotation.

The align-and-go startup waveforms of the A89303 device are shown in Figure 5. As shown in this figure, the rotor is quickly aligned to a known position (initial peak current), and open-loop pulses of increasing frequency are applied.

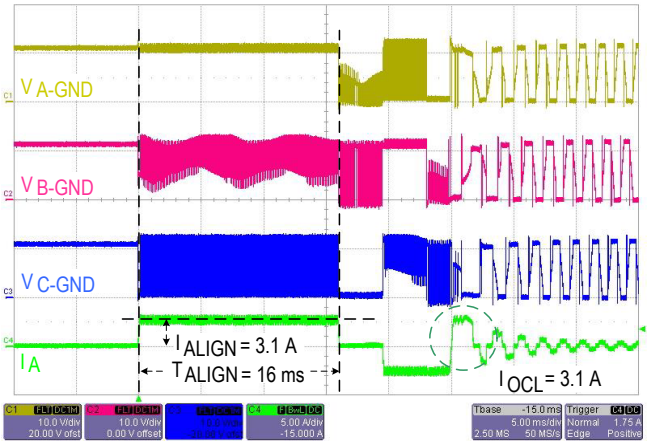

Figure 5: BLDC Motor Align Condition

STARTUP TECHNIQUES—INITIAL POSITION DETECTION

The initial position detection (IPD) algorithm is designed to detect the rotor position without any movement of the rotor. The IPD algorithm is designed for applications where reverse rotation of the BLDC motor is not acceptable. Moreover, because the align functionality is not required further and only open-loop starting pulses are applied, the total start-up time in IPD is less than the align-and-go startup technique. The principle of operation lies in the fact that the inductance of the motor varies as a function of rotor position. This algorithm injects short-duration current pulses to the motor. These pulses are short enough that they do not overcome the inertia of rotor, so rotor movement is not observed.

The A89303 uses a two-pulse IPD scheme comprising two stages—the complimentary drive and detect (CDD) stage and the polar axis current injection (PACI) stage.

The CDD stage involves a complementary and balanced (50% duty) switching between phases in sequential order: Phase A to Phase B (AB), then Phase B to Phase C (BC), then Phase C to Phase A (AC). Inductance variations during these sequences are detected by monitoring the floating phase voltage. The 50% duty cycle ensures that the average voltage applied is zero and there is no residual voltage that can lead to rotor movement in multiple such PWM cycles.

To express the CDD stage mathematically, consider the case of two phases that are excited (e.g., Phase AB), where current flows from VBB to Phase A to Phase B and sinks to GND, as shown in Figure 6.

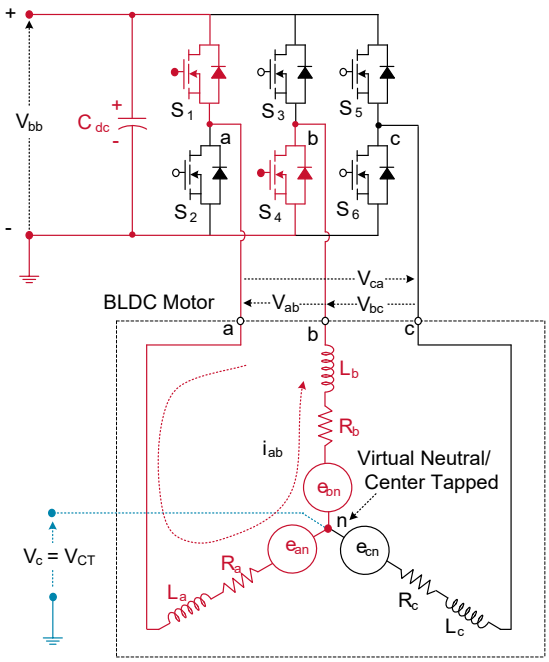

Figure 6: BLDC Motor Modeling

Because Phase C is a nonconducting phase, floating voltage—i.e., V_{CT} (center-tapped voltage)—is calculated from Phase A as:

Equation 1:

$$V_{CT} = V_{bb} - i_{ab} \times R_a - L_a \frac{d}{dt}(i_{ab}) - e_{an}$$; and

voltage, V_{CT}, is calculated from Phase B as:

Equation 2:

$$V_{CT} = i_{ab} \times R_b + L_b \frac{d}{dt}(i_{ab}) - e_{bn}$$.

Because the rotor does not move for operation, the back-emf (e_{an} and e_{bn}) is zero, and Equation 1 and Equation 2 can be rewritten as:

Equation 3:

$$V_{CT} = V_{bb} - i_{ab} \times R_a - L_a \frac{d}{dt}(i_{ab})$$; and

Equation 4:

$$V_{CT} = i_{ab} \times R_b + L_b \frac{d}{dt}(i_{ab})$$.

When Equation 3 and Equation 4 are added and rearranged, the voltage at the floating phase, C (V_C), is:

Equation 5:

$$V_C = V_{CT} = \frac{V_{bb}}{2} + \frac{i_{ab}}{2} \times (R_b - R_a) + \frac{(L_b - L_a)}{2} \frac{d}{dt}(i_{ab})$$.

For a balanced BLDC motor where phase resistances are equal ($R_a = R_b$), Equation 5 can be rewritten as:

Equation 6:

$$V_C = \frac{V_{bb}}{2} + \frac{(L_b - L_a)}{2} \frac{d}{dt}(i_{ab})$$.

Hence, the floating phase voltage is dependent on the variation of the inductance (L_a and L_b). Based on this dependency, the floating phase voltage is higher or lower than the threshold according to:

Equation 7:

$$\text{if } L_b > L_a \Rightarrow V_C > \frac{V_{bb}}{2} \parallel L_b < L_a \Rightarrow V_C < \frac{V_{bb}}{2}$$.

To compare the inductances of two phases, this floating voltage (V_C) needs to be compared with the $V_{bb}/2$ voltage reference level, as shown in Figure 7.

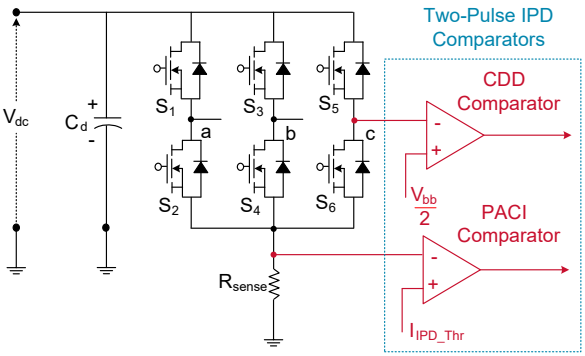

Figure 7: Comparators in Two-Pulse IPD

The two-pulse IPD waveforms in the CDD stage are shown in Figure 8, where the floating phase (Phase C, blue), exhibits back-emf (i.e., V_{CT}) that pulsates between levels that are greater than or less than the $V_{bb}/2$ level.

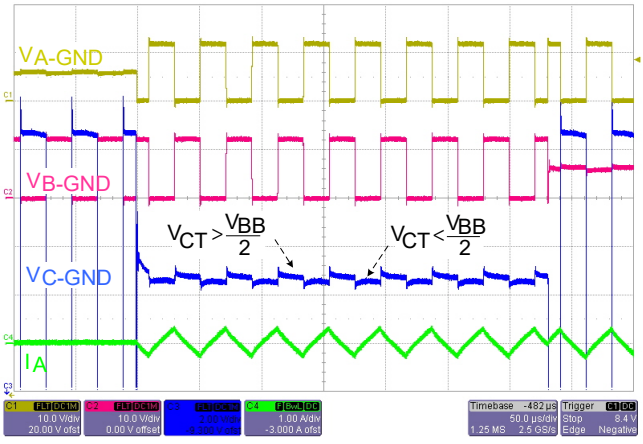

Figure 8: Comparators in Two-Pulse IPD

In this way, rotor position is detected in one sector of the quadrant pairs, as shown in Figure 9, which includes an example of the CDD stage with quadrant data. In this figure, if Phase AB is excited with complimentary pulses, the CDD algorithm detects if the rotor is in Quadrant 2 or Quadrant 3.

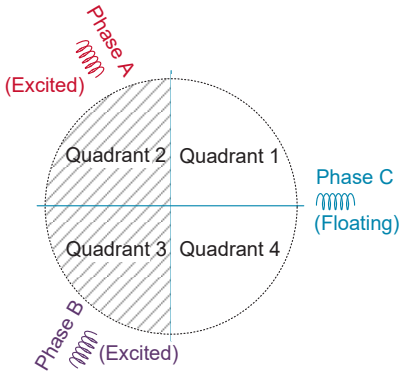

Figure 9: CDD Quadrant Pairs

Similarly, Phase AC and Phase BC are excited sequentially, and the rotor can be positioned in two of the 12 sectors, as shown in Figure 10.

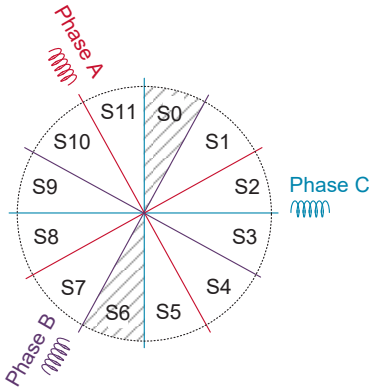

Figure 10: Two-Sector Detection from CDD Stage

These 12 sectors are formed by three quadrants offset by 120 degrees. Based on the three sequential phases and the outcome of the floating phase voltage (0 when $V_{CT} < V_{bb}/2$; and 1 when $V_{CT} > V_{bb}/2$), the rotor position is determined to be aligned in one of two angles, as shown in Table 1. For example, in Figure 10, the rotor is aligned in either the S0 sector or the S6 sector.

Table 1: Angle of Alignment with Code

Code	Angle
001	30 or 210
011	60 or 240
010	90 or 270
110	120 or 300
100	150 or 330
101	180 or 0

Once CDD is complete, the PACI is used to determine in which of two sectors (identified in CDD) the rotor is located. During the first pulse, phase current is driven in one direction until the V_{BB} current reaches the PACI threshold, and the time for the V_{BB} current to reach the PACI threshold is measured. In the second pulse, current is applied in the opposite direction, and the time is noted as with the previous measurement. The shorter time measurement corresponds to the sector where north pole is aligned to the corresponding phase.

The two-pulse IPD waveforms of the DC link current and the phase current are shown for the CDD and PACI stages in Figure 11 and Figure 12, respectively. Because the CDD occurs during a high-frequency state, the CDD stage takes much less time than the PACI stage, as shown. The PACI stage demonstrates current excitation during Phase CA and Phase AC; this excitation corresponds to the sector detected during the CDD stage. Because Phase AC is shorter in duration, the rotor is aligned in Phase AC.

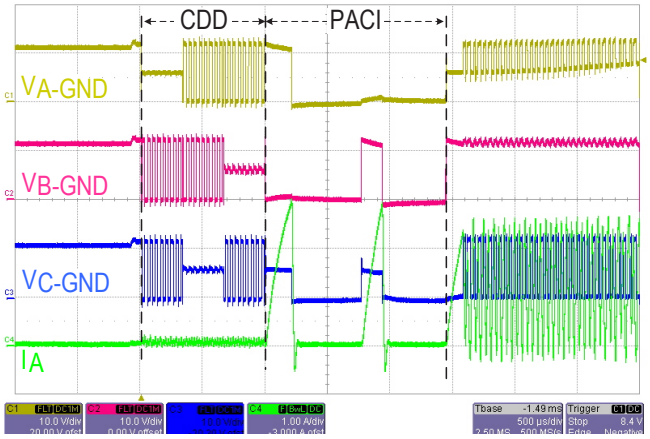

Figure 11: Two-Pulse IPD Waveforms with DC Link Current

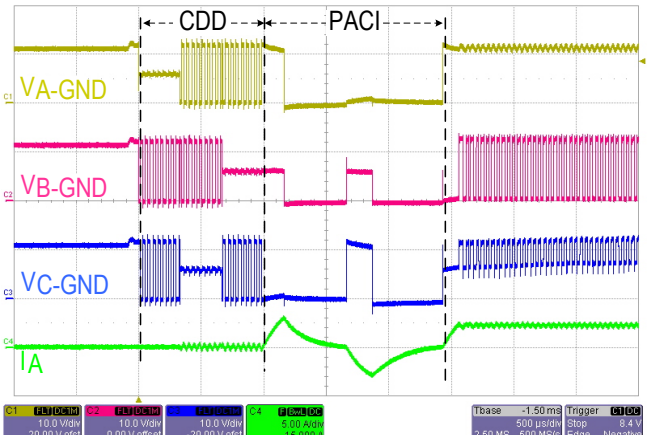

Figure 12: Two-Pulse IPD Waveforms with Phase Current

The two-pulse IPD procedure is:

CDD Phase:

1. Drive the first pair (AB) of phase voltages, and measure the floating voltage (C).
2. Drive the second pair (AC) of phase voltages, and measure the floating voltage (B).
3. Drive the third pair (BC) of phase voltages, and measure the floating voltage (A).
4. Determine the possible sector location of the rotor.

PACI Phase:

5. Drive current in one direction, and measure the time to reach the threshold.
6. Drive current in the other direction, and measure the time to reach the threshold.

Compare the times obtained in steps 5 and 6, and determine the rotor position. The two-pulse IPD has various advantages over the conventional six-pulse IPD technique.

- **Quiet Operation:** There is no significant acoustic noise or vibration because it operates at a higher switching frequency (25 kHz).
- **Detection Time:** Rotor position detection time is faster due to the higher switching frequency.
- **Position Resolution:** Less resolution is achieved (30 degrees compared to 60 degrees).
- **Torque:** Less torque is required because fewer pulses are used.
- **Maximum Torque:** Approximately 50% less torque is required because the maximum required torque is proportional to the degrees of resolution:
  - Six-pulse IPD: Proportional to sin (60/2) = 0.5.
  - Two-pulse IPD: Proportional to sin (30/2) = 0.258.
- **Accuracy:** Accuracy is better because the PACI technique compares two sectors that may be in alignment or in opposition to one another.
- **Tolerance:** The unbalanced windings have better tolerance because two pulses are applied, and the unbalanced motor winding error is canceled.

SALIENT FEATURES OF A89303

The Allegro A89303 device provides various advantages that make it attractive for fuel pump applications, such as:

- Fast start-up features with advanced initial position detection algorithm (two-pulse IPD) to reduce the BLDC motor startup time, which enables an easier kick-start.
- Inbuilt logic regulator for the internal digital core without the need for an external capacitor. This reduces both EMI and the bill of materials (BOM).
- The sensorless motor control eliminates the need for Hall-effect position sensors in BLDC motors and thus lowers the BOM cost for the motor.
- In-built digital algorithms and EEPROM parameter settings provide design flexibility and reduce overall development time and cost.
- Advanced features, such as an overlapping mode, provide a speed boost to the motor by adaptively adjusting the phase advance angle.
- Smaller QFN package offers the smallest system footprint.

SPEED CONTROL OPTIONS

A89303 can be designed for either: 1) fixed-speed operation; or 2) variable-speed operation, controlled via an external controller.

Fixed-Speed Option

In the fixed-speed option, the PWM/SCL pin of the A89303 is tied directly to the power supply via a Zener diode and a biasing resistor, as shown in Figure 13. The Zener diode provides a regulated voltage of 5 V to the PWM/SCL pin at varying supply voltages.

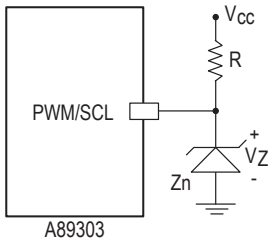

Figure 13: Fixed-Speed Connections to A89303

The input impedance of the PWM/SCL pin, being an input, is very high. Therefore, the input current requirement for this pin is very low and can be neglected. The supply voltage can vary from 8 V (minimum operating voltage) to 40 V (at load dump). Considering a typical value of Zener current as 1 mA, the value of a current-limiting resistor, R, is:

Equation 8:

$$I_Z = \frac{V_{bb} - V_Z}{R}$$

The maximum value of the resistor is calculated at the minimum supply voltage as:

Equation 9:

$$R_{\max} = \frac{\left(V_{bb\_\min} - V_Z\right)}{I_Z} = \frac{8V - 5V}{1mA} = 3\ \ \Omega k$$

The power dissipation of the resistor is calculated for the maximum input voltage as:

Equation 10:

$$P_R = \left(I_{MAX}\right)^2 R = \frac{V_{MAX}{}^2}{R} = \frac{40^2}{3k} = 0.533\ W$$

Hence, an appropriate package for the resistor must be used for dissipation of such power. Because this high voltage is expected for a shorter duration (load-dump peak time), the transient power rating of the resistor can be considered.

Variable-Speed Option

In the variable-speed option, a microcontroller can be used to change the PWM duty cycle to alter the speed of the BLDC motor. The PWM/SCL pin of the A89303 can be directly connected to the PWM peripheral of the microcontroller, as shown in Figure 14.

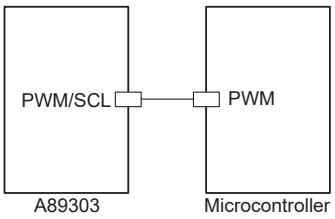

Figure 14: Variable-Speed Connections to A89303

The many advantages of using PWM-based speed control of a BLDC motor in a fuel pump include:

- The PWM control reduces excess fuel intake. When an intake of excess fuel occurs, the excess enters constant recirculation, which causes heating of fuel via absorbed energy from the pump and engine. By reducing excess fuel intake using the PWM control, high-speed heating is avoided and fuel pump performance, fuel pump life, and fuel density are all enhanced.
- In the fixed-speed option, to cater to excess fuel intake that may occur at lower load on the engine, the increased amount of fuel that passes through the regulator requires greater capacity in both the line to the regulator and the return path. This can be eliminated using PWM control.
- The noise of the fuel pump increases at lighter load if it is running at full speed. Therefore, speed control helps reduce system noise.

PARAMETER CONFIGURATION

This section includes various parameter configurations and their impact on the application.

- **Direction:** This setting is used for the selection of motor direction of rotation, either in the ABC direction or the ACB direction.
- **Brake if Moving:** As soon as the motor start command is issued, before the start operation commences, the A89303 device checks to see if the motor is moving. If motion is detected, the motor brake (where all three low-side FETs are turned on) is applied before attempting to start. For faster startup, this setting can be disabled.
- **IPD Enable:** This setting defines which algorithm is used:
  - If enabled, the initial position detection algorithm is used when required.
  - If disabled, the IC enables the conventional align-and-go algorithm.

- **IPD Decay Mode:** During the second stage of IPD (i.e., the PACI stage), phase current is injected. This setting determines the mode of current decay after the injection pulse. The current decay can be set for either slow decay or fast decay. The drive stage, where the high-side MOSFET (S1) of Phase A and the low-side MOSFET (S4) of Phase B are turned on, is shown in Figure 15. In fast decay (coasting) mode, both phases are turned off, and the current decays through the body diodes of S2 and S3, as shown in Figure 16. Because a negative voltage is applied to the back-emf, current decays very quickly in this mode. However, in slow decay (brake mode), the low-side MOSFET of the bridge is turned on, as shown in Figure 17. The current decay in this mode is slow because the current is limited only by winding resistance and the on-state resistance of the MOSFET.

  The IPD slow-decay and fast-decay modes of the A89303 device are shown in Figure 18 and Figure 19, respectively. Decay time is approximately 200 µs in slow-decay mode and approximately 40 µs in fast-decay mode.

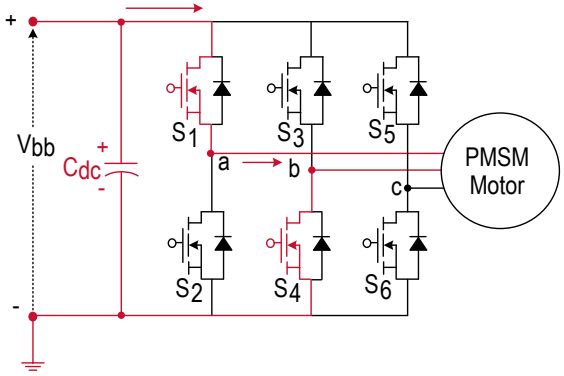

Figure 15: Driving Stage

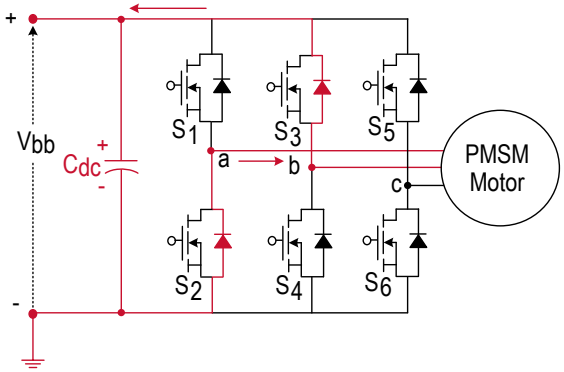

Figure 16: Coasting Stage (Fast Decay)

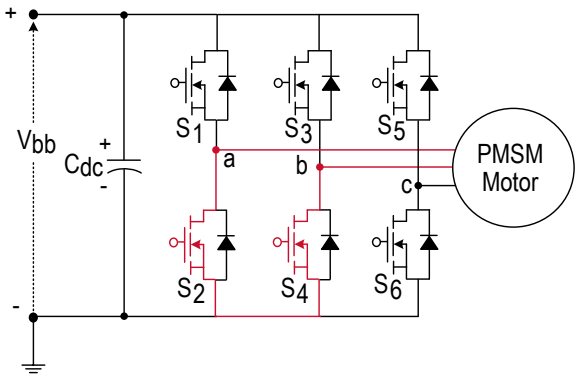

Figure 17: Braking Stage (Slow Decay)

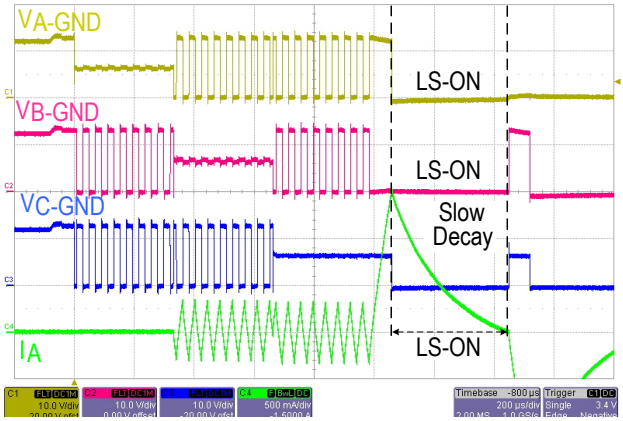

Figure 18: IPD Slow-Decay Mode

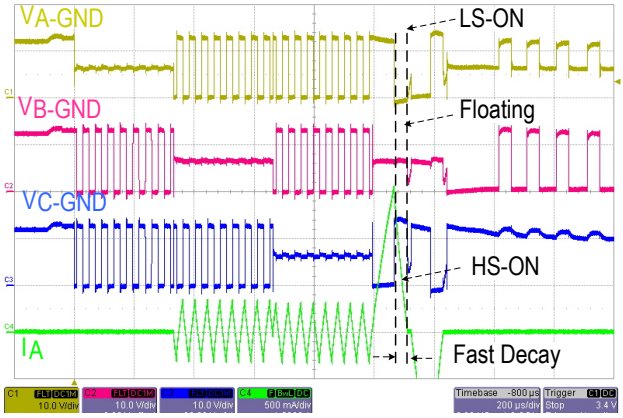

Figure 19: IPD Fast-Decay Mode

- **Initial Step IPD:** This parameter defines the peak current threshold for the IPD algorithm. The IPD current threshold must be set high enough for reliable motor startup, yet as low as possible to minimize acoustic noise during startup. The peak current (I_{IPD}) can be calculated as:

  Equation 11:

$$I_{IPD} = CODE \times \left(\frac{10mV}{R_{SENSE}} \right),$$

  where CODE is the decimal value programmable from 0 to 31 and R_{SENSE} is the sense resistor value.

  The initial step IPD current settings are shown in Figure 20 and Figure 21 as 3.1 A (Code: 31) and 1.5 A (Code: 15), respectively. For this evaluation, the sense resistor is 100 mΩ.

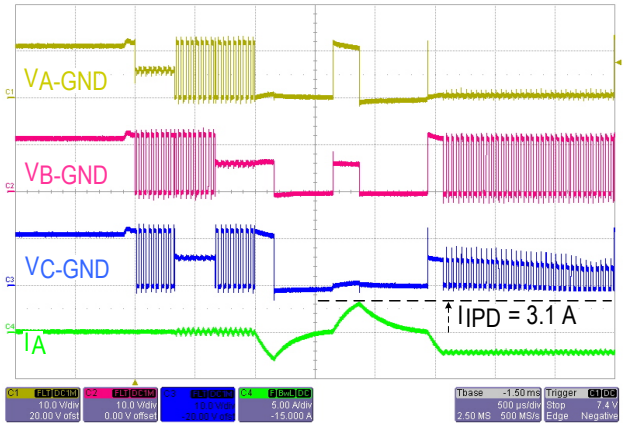

Figure 20: Initial Step IPD as 3.1 A (Code: 31)

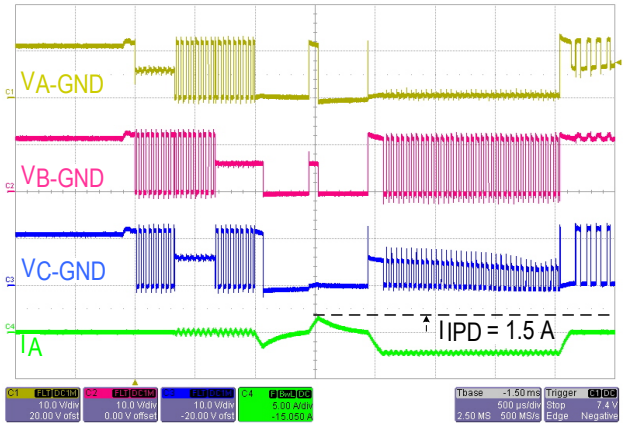

Figure 21: Initial Step IPD as 1.5 A (Code: 15)

- **IPD Step Size:** If the IC is not able to detect the position of the rotor on the first attempt, this setting determines the steps of consecutive IPD pulse currents. The maximum number of attempts is four. For example, if the initial step is 10 (i.e., 1 A) and the step size is 3, current pulses of 1 A, 1.3 A, 1.6 A, and 1.9 A are applied.

- **Align Time:** The align-and-go algorithm (IPD enable bit is low), aligns the rotor to a fixed position, then applies open-loop pulses of increasing frequency. The align time is the duration of the peak current during motor alignment. If the duration of this alignment is sufficiently long, the rotor becomes aligned to a known position. In this operation, the high-side MOSFET of Phase A and the low-side MOSFET of Phase B are turned on, and Phase C remains in a high-impedance (high-Z) state. A low-inertial motor-like pump can proceed with operation quickly because it does not require a waiting period for the rotor to settle into a known position. For fastest startup, the align time can be set to 2 ms.

  During alignment, the alignment current is held at the set reference level. Example performance is shown in Figure 22 and Figure 23 for a 3.1 A current with an 8 ms alignment time and a 1.5 A current with a 16 ms alignment time, respectively.

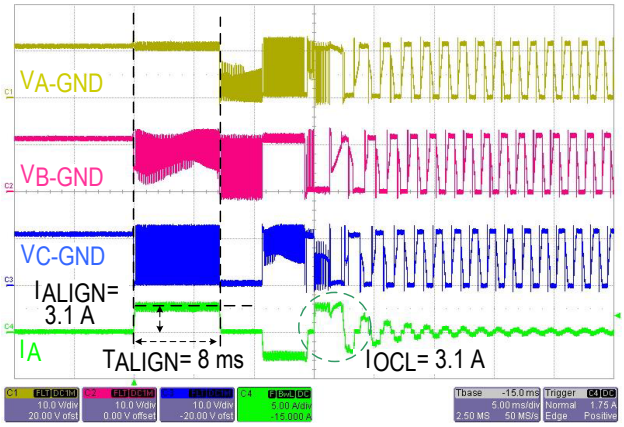

Figure 22: Alignment Time = 8 ms, Alignment Current = 3.1 A with Same Alignment-Overcurrent Limit (OCL) and OCL Levels

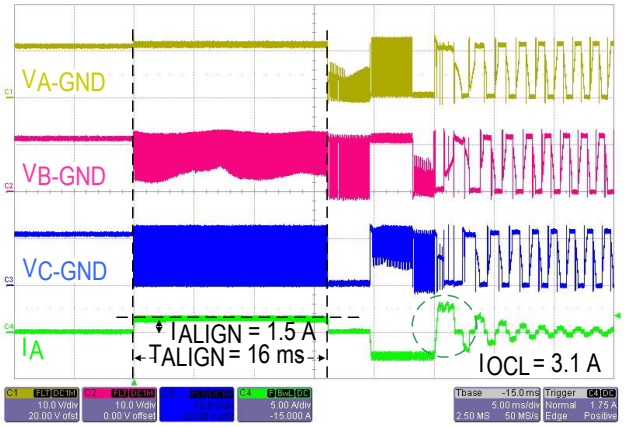

Figure 23: Alignment Time = 16 ms, Alignment Current = 1.5 A with Different Alignment OCL and OCL Levels

- **Align OCL:** Align OCL is the peak current applied during the align state and can be configured in two ways:
  - **OCL Level:** In this setting, the align OCL (I_{ALIGN}) is equal to the OCL level (I_{OCL}) and is configured as:

    Equation 12:

    $$I_{ALIGN} = I_{OCL} = CODE(15-31) \times \left(\frac{10mV}{R_{SENSE}} \right),$$

    where CODE is a decimal value programmable from 15 through 31.
  - **IPD Initial Step Level:** The align OCL setting can be set to a lower level, configured by the initial step IPD setting. Because this setting has the potential to quicken the time needed for the rotor to settle into position, it is particularly beneficial for applications that require long alignment times due to rotor settling. After the alignment is complete, operation commences with the typical OCP level, calculated as:

    Equation 13:

    $$I_{ALIGN} = I_{IPD} = CODE(0-31) \times \left(\frac{10mV}{R_{SENSE}} \right),$$

    where CODE is a decimal value programmable from 0 through 31.
- **Startup Oscillator Time:** This variable defines the commutation time for the initial steps after the alignment stage. A startup oscillator time of 3.5 ms is observed immediately after the alignment time expires, as shown in Figure 24.

  Moreover, the startup oscillator time is also used during the sensorless mode of operation as the maximum limit of the commutation state. During this operation, if the back-emf is not detected properly within the startup oscillator time, the sequencer advances to the next state.

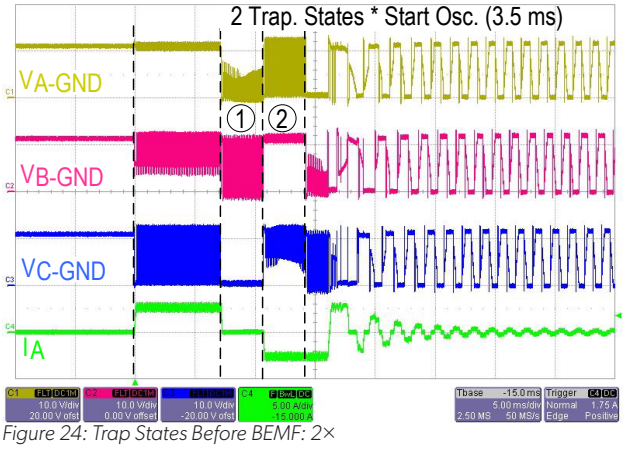

Figure 24: Trap States Before BEMF: 2×

- **Trap Steps Before BEMF:** This variable defines the number of steps to be taken before the back-emf detection circuitry is activated. The duration of the individual step is defined by the startup oscillator time.

  The 2× and 4× trap states are shown in Figure 24 and Figure 25, respectively, with a startup oscillator time of 3.5 ms.

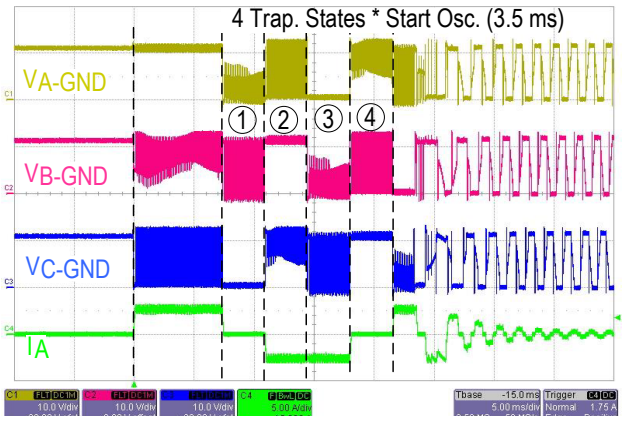

Figure 25: Trap States Before BEMF: 4×

- **BEMF Hysteresis:** The sensorless algorithm determines the rotor position by comparing the back-emf voltage of the floating phase (high-impedance state) to the center-tap voltage during the stage that corresponds to zero phase current. This comparator incorporates a hysteresis voltage to cater to the noise on the phase-node sensing.

  A block diagram of the back-emf sensing circuitry is shown in Figure 26. This includes a back-emf voltage comparator with programmable hysteresis voltage and programmable digital filter (explained in the next section). The back-emf hysteresis programmable settings are 50 mV, 200 mV, 300 mV, and 550 mV.

  NOTE: The back-emf hysteresis is only enabled during startup or when the motor drive is disabled. During typical operation, the back-emf hysteresis level is set to 0 mV automatically.

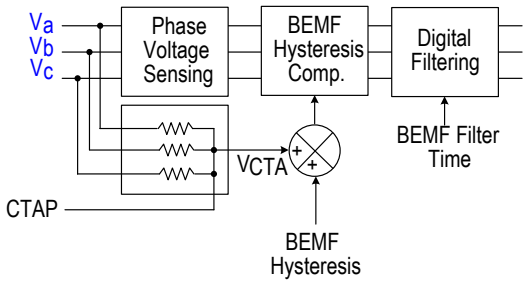

Figure 26: BEMF Comparators and Filters

- **BEMF Filter:** The back-emf filter is a digital time filter designed to eliminate PWM noise during back-emf sensing. These transients appear coincident with the edges of the PWM signal, and proper position measurement requires these transients to be filtered out. Noise pickup during the back-emf sensing of the floating phase is shown in Figure 27; as shown, due to initial transients, the back-emf measurement must be performed with at least 8 µs filtering.

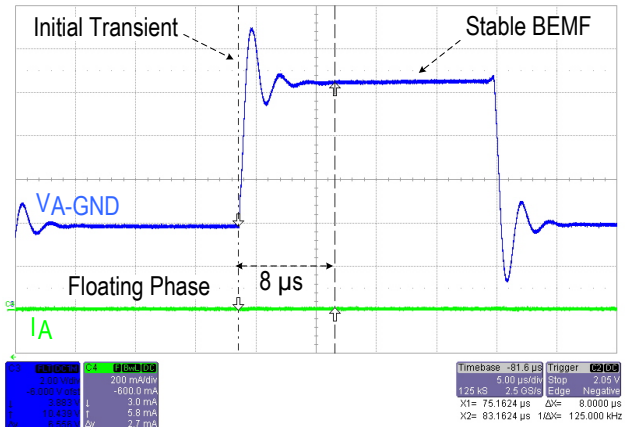

Figure 27: Comparators and Filters

The CTAP pin is also provided in the A89303 device as shown in Figure 26. This pin can be connected directly to the midpoint of the star connection of the BLDC motor. This compensates for any error in the back-emf estimation due to the unbalanced phase windings.

Lock Time: This parameter defines the waiting period before the IC attempts to restart, which is required after the lock condition is detected. Lock times of 100 ms and 300 ms are shown in Figure 28 and Figure 29, respectively. Longer lock times are recommended to allow the motor enough time to cool down from any excessive heating that may have occurred in the lock condition.

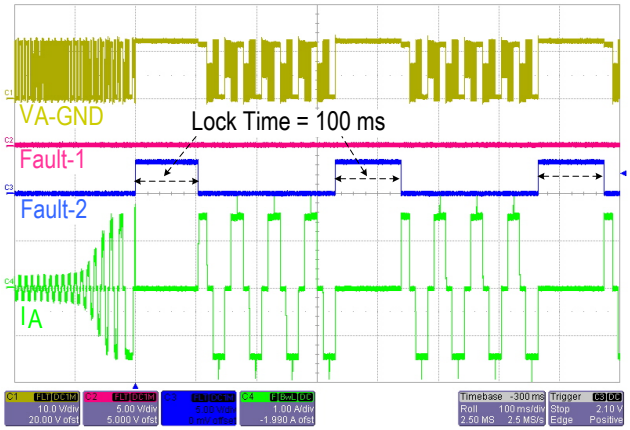

Figure 28: Lock Time of 100 ms

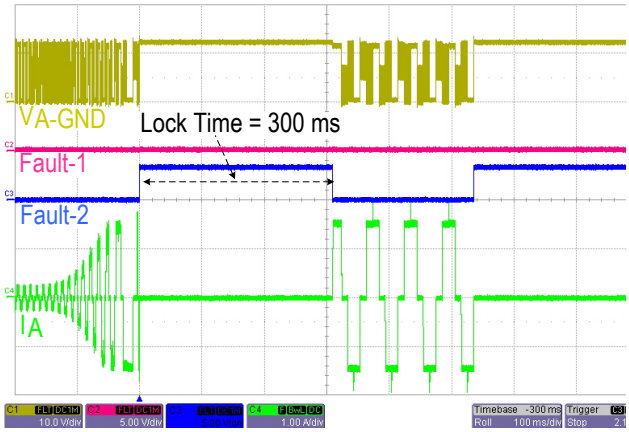

Figure 29: Lock Time of 300 ms

- **Commutation-State Stall Limit:** This variable defines the number of commutation states that can occur before the lock-detection logic is checked. The lock-detection logic checks for valid back-emf crossings and increments a counter when incorrect and decrements the counter when the correct commutation state is detected. In this way, the logic determines if the rotor is locked and can shut down to avoid motor overstress.

  The commutation-state stall limits are shown for 44 and 22 commutation states in Figure 30 and Figure 31, respectively.

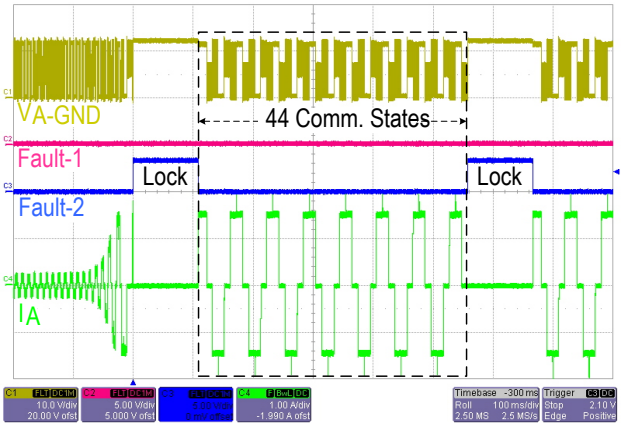

Figure 30: 44 Commutation-State Stall Limit

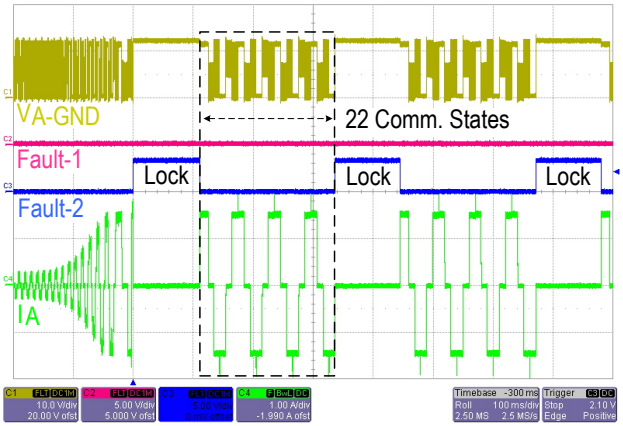

Figure 31: 22 Commutation-State Stall Limit

- **Quick Startup Retry:** Typically, when a lock condition is detected, the motor shuts off for the programmed lock time. The quick-start option ignores the lock timer and attempts a restart immediately. If the following restart is also not successful, the typical lock time is used. Operation of the A89303 is shown without and with the quick-retry operation in Figure 32 and Figure 33, respectively. As shown in Figure 33, during the quick-retry operation, a quick startup is attempted before the lock condition is detected.

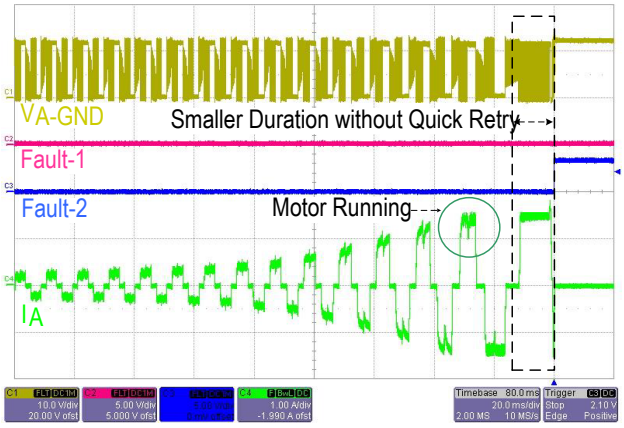

Figure 32: Motor Operation without Quick-Retry Operation

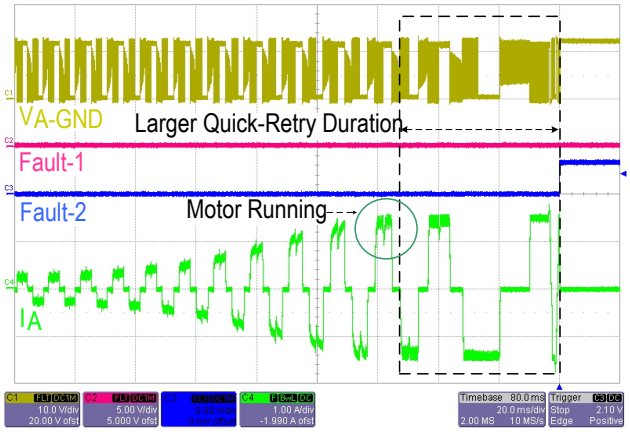

Figure 33: Motor Operation with Quick-Retry Operation

- **OCL Methods:** The overcurrent limit (OCL) functionality in the A89303 has two options:
  - **Fixed Off-Time Method:** After the current limit is reached, the appropriate driver is turned off for the time defined by the OCL off-time variable. The fixed off-time (40 µs) waveform of the driver operating at the current limit is shown in Figure 34.
  - **PWM Cycle Method:** After the current limit is reached, the driver is turned off for the remaining portion of the PWM cycle. The PWM period is fixed at 40 µs (25 kHz PWM frequency). The current limit operation clearly exhibits a period of 25 kHz (i.e., 40 µs), as shown in Figure 35.

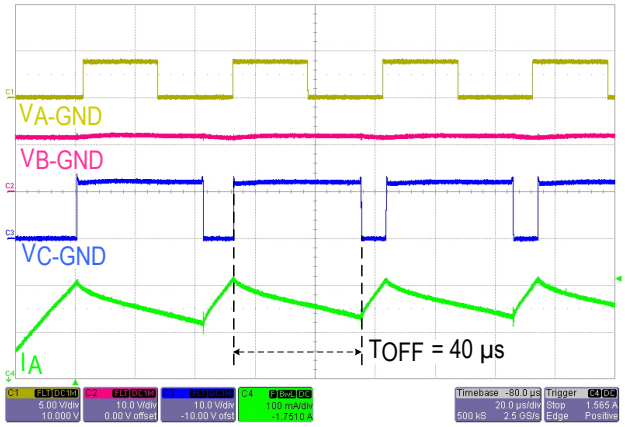

Figure 34: Fixed Off-Time Method

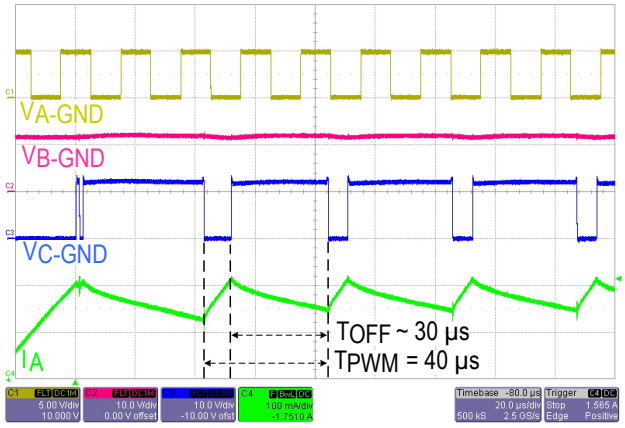

Figure 35: PWM Cycle Method

- **OCL Level:** The OCL level is the peak current applied during startup and typical operation of the motor (other than the align state). This can be configured as:

  Equation 14:

$$I_{ALIGN} = I_{OCL} = CODE\left(15-31\right)\times\left(\frac{10mV}{R_{SENSE}}\right),$$

  where CODE is a decimal value programmable from 15 through 31.

- **OCL Off-Time:** When the driver is operating with a fixed off-time, the off-time can be programmed with any of four options—8 µs, 16 µs, 32 µs, or 40 µs. The fixed off-time OCL operation is shown in Figure 34 and Figure 36 for 40 µs and 16 µs off-times, respectively. Both options of overcurrent limit have advantages and limitations:
  - The PWM cycle option has a fixed PWM frequency, so emissions related to switching are predictable and filter design is easier. However, due to fixed-frequency operation, if the inductor is not completely discharged, the current can become saturated by the motor inductance. This leads to a subharmonic instability at higher-duty operation.
  - The fixed off-time option allows a longer off-time, which can eliminate inductance saturation. However, due to variations in the switching frequency of the system, the filter design becomes complex.

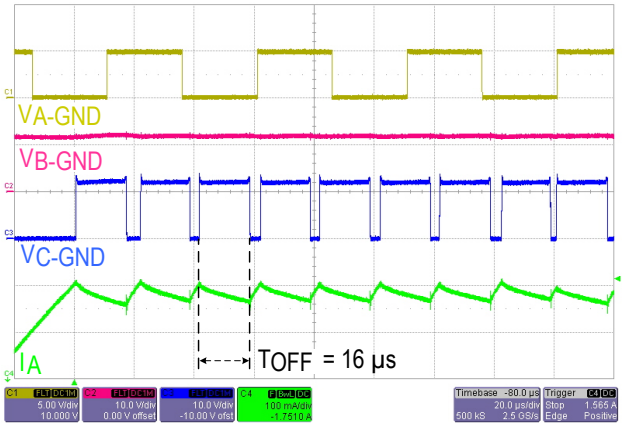

Figure 36: Fixed Off-Time Method with 16 µs Off-Time

- **Overcurrent Protection:** The A89303 device is protected against any overcurrent scenario (current higher than I_{OCP} = 5 A minimum) by the overcurrent protection trip. The OCP circuit of each FET monitors the drain-to-source voltage (V_{DS}) and disables the current flow through the FET by removing the gate drive in the case of overcurrent. Fault pin FF1 is set low and fault pin FF2 is set high to indicate a motor-lead fault. The OCP is a latched fault and requires a power-cycle to restart the device.

  Driver operation in the OCP scenario is shown in Figure 37, which includes overshoot due to the deglitch filter.

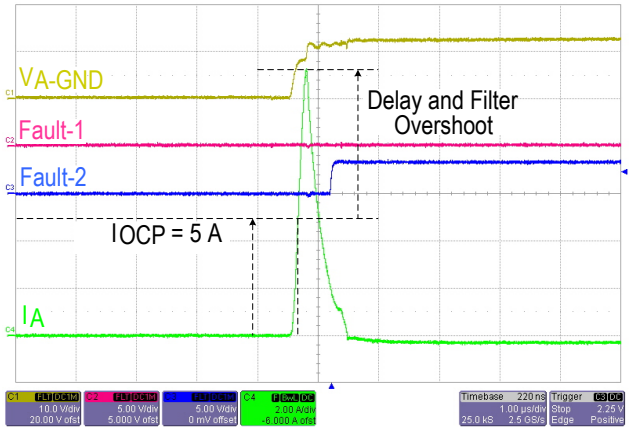

Figure 37: Overcurrent Protection

- **VBB UVLO:** A VBB undervoltage scenario occurs when the supply voltage decreases below the VBB undervoltage threshold (V_{BBUVLO}). Two configuration options are available for the VBB UVLO operation:
  - **Disable Output Option:** If the disable output option is chosen, the fault flag is signaled, and output is disabled. Operation with output disabled is shown in Figure 38.
  - **Fault Flag Only Option:** If the fault flag only option is chosen: The outputs are not disabled, and the fault is flagged as shown in Figure 39. If the fault flag only option is chosen and the supply voltage decreases, upon detection of the charge pump undervoltage, motor output becomes disabled. Charge pump overvoltage is detected when supply voltage is in the range of 3.9 V, which gives an extra margin for the device to operate before it turns off due to charge pump fault, as shown in Figure 39.

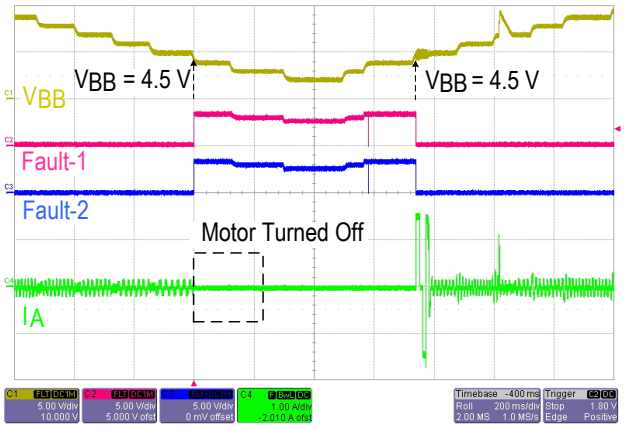

Figure 38: VBB UVLO with Output Disabled

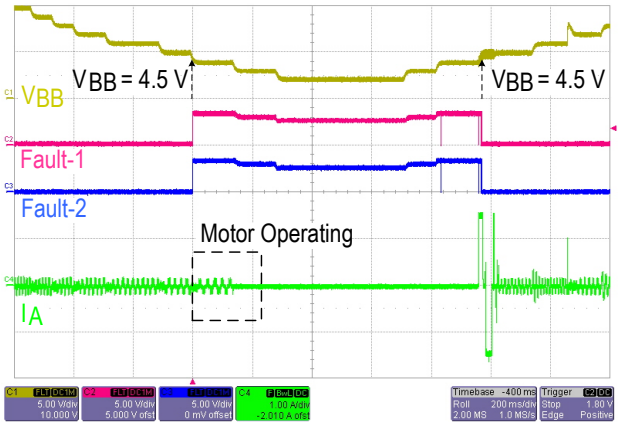

Figure 39: VBB UVLO with Faults Flag Setting

- **VBB OVP:** If the input supply voltage rises above the VBB overvoltage threshold (V_{BBOV}), the driver enters the high-impedance state, as shown in Figure 40. When the supply overvoltage condition is removed, typical operation resumes (i.e., the driver operation and the fault pins return to the reset state).

  The A89303 device also supports an option to disable this overvoltage protection (OVP) feature, as shown in Figure 41. this option is recommended if extended transient voltage suppressor (TVS) diode range is desired, for instance, to support higher voltage during a load-dump scenario.

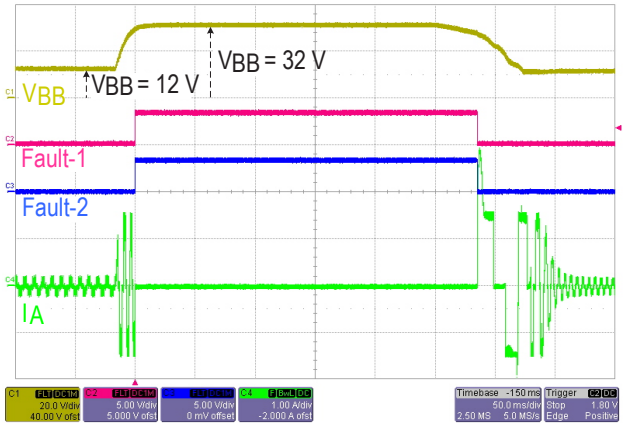

Figure 40: VBB OVP Enabled

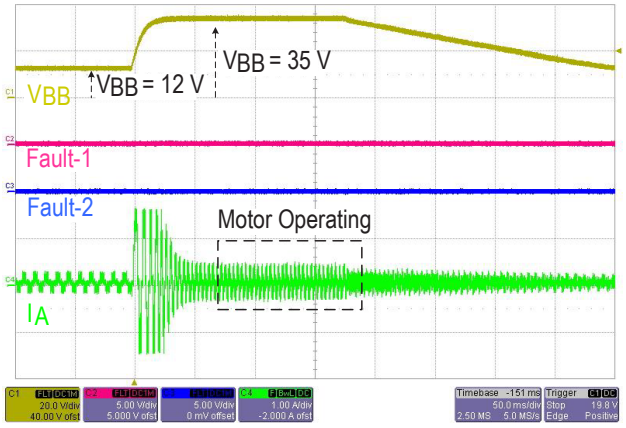

Figure 41: VBB OVP Disabled

- **Thermal Protection:** If the junction temperature exceeds thermal shutdown limits (T_{JTSD}), all FETs in the driver are disabled and fault pin FF1 is driven high. After the die temperature decreases to a value within the specified limits, typical operation resumes automatically.
- **Overlapping Mode:** A89303 is equipped with an overlapping mode that allows an efficient operation of the BLDC motor by adaptively adjusting (leading) the phase angle of the applied voltage. This phase-leading also results in extraction of maximum power from the BLDC motor. Operation of the overlapping mode is shown in Figure 42. The overlap angle (phase advance, $\theta_{Advance}$) for the maximum power is estimated as:

  Equation 15:

$$\theta_{Advance} = \frac{\theta_{Comm}}{2} = \frac{\omega_L I_{Phase} L_{Phase}}{2V_{BB}},$$

  where θ_{comm} is the commutation angle, ω_L is the motor speed in rad/s, I_{phase} is the Phase Current, L_{phase} is the phase inductance, and V_{BB} is the DC bus voltage.

  From Equation 15, it is evident that higher-current, higher-inductance motor operation at higher speed requires a greater advance angle. Operation of A89303 is shown without the overlapping mode, with 100% PWM duty in Figure 43 and Figure 44 (zoomed). As shown in Figure 44, the high side of Phase A is turned on as soon as the high-side of Phase C is turned off. The current in Phase C reduces and decays to zero and floating back-emf is observed in a high-Z state.

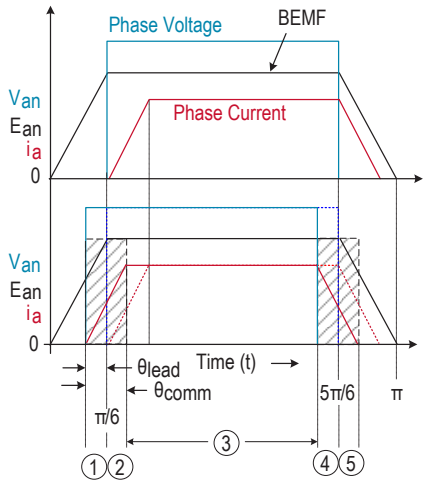

Figure 42: Overlapping Mode Operation

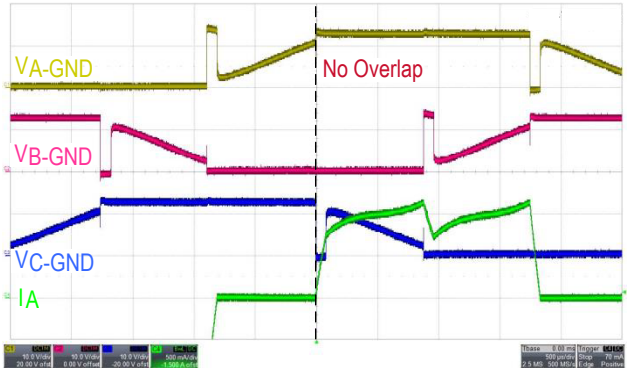

Figure 43: Overlapping Mode Disabled in 100% PWM Duty

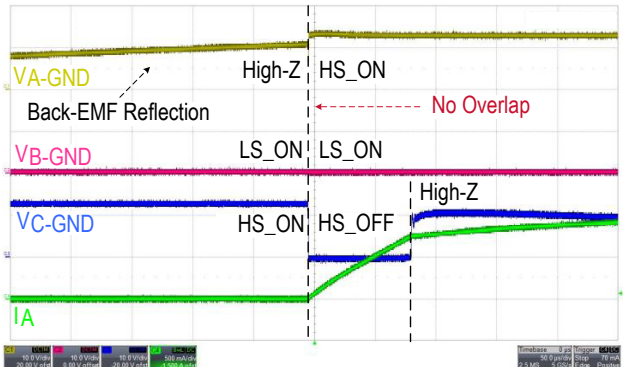

Figure 44: Overlapping Mode Disabled in 100% PWM Duty (Zoomed)

Operation of A89303 with 100% PWM duty with overlapping mode enabled is shown in Figure 45 and Figure 46 (zoom). As shown in Figure 45, the turn-on timings of high-side switches of Phase A and Phase C overlap. This shows that Phase A is turned-on before Phase C is turned off completely, thus providing an advance angle.

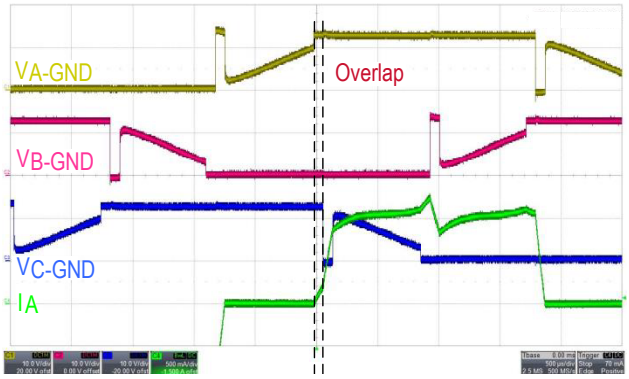

Figure 45: Overlapping Mode Enabled in 100% PWM Duty

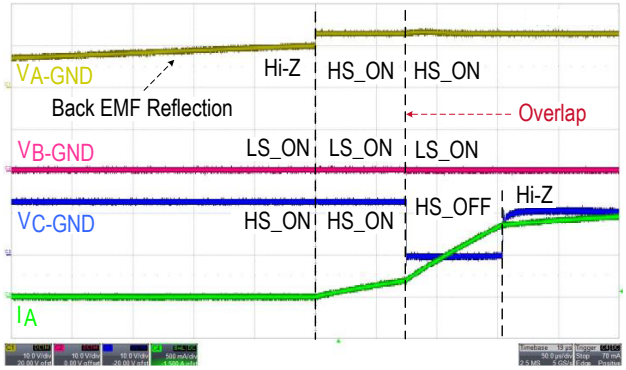

Figure 46: Overlapping Mode Enabled in 100% PWM Duty (Zoomed)

Operation without enabling the overlapping mode, with the motor operating at 50% PWM duty, is shown in Figure 47 and Figure 48 (zoomed).

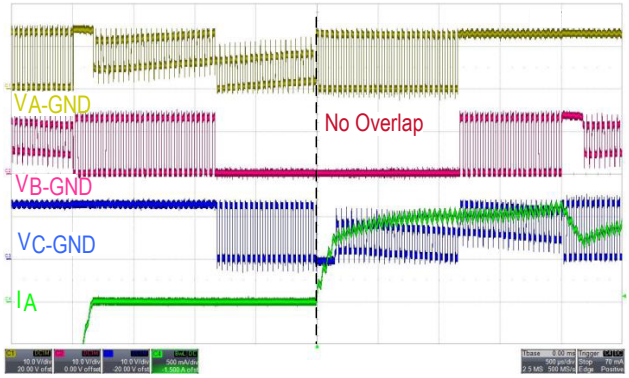

Figure 47: Overlapping Mode Disabled in 50% PWM Duty

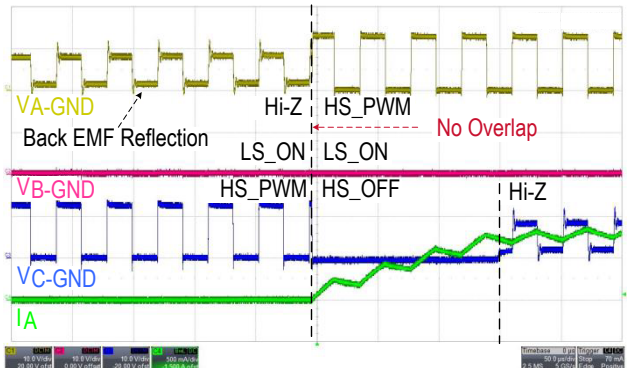

Figure 48: Overlapping Mode Disabled in 50% PWM Duty (Zoomed)

Operation of the A89303 with 50% PWM duty with overlapping mode enabled is shown in Figure 49 and Figure 50 (zoomed). As shown in Figure 50, an overlap of Phase A and Phase C is observed. During the time of this overlap, both Phase A and Phase C operate in PWM switching mode; once the overlap period is over, switching is performed by Phase A only. The commutation angle is calculated in every electrical cycle and the corresponding phase advance (overlap) is added automatically in the next cycle.

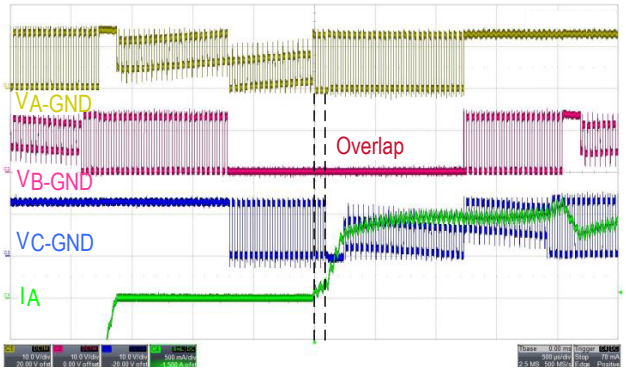

Figure 49: Overlapping Mode Enabled in 50% PWM Duty

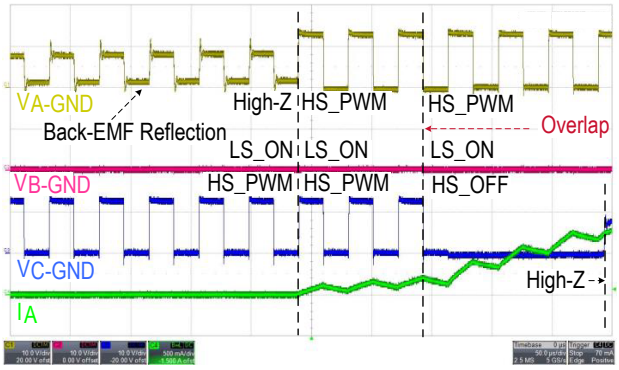

Figure 50: Overlapping Mode Enabled in 50% PWM Duty (Zoomed)

EFFICIENCY AND THERMAL CONSIDERATIONS

The total power dissipation in the A89303 device has four primary components—conduction losses, switching losses, diode freewheeling losses, and quiescent power losses. The synchronous switching waveform of Phase A (OUTx) of the A89303 device is shown in Figure 51. Here, the high-side MOSFET turns off while the low-side MOSFET turns on; the correspond conduction losses (CL), switching losses (SL), and diode freewheeling losses (DL) are shown in the figure.

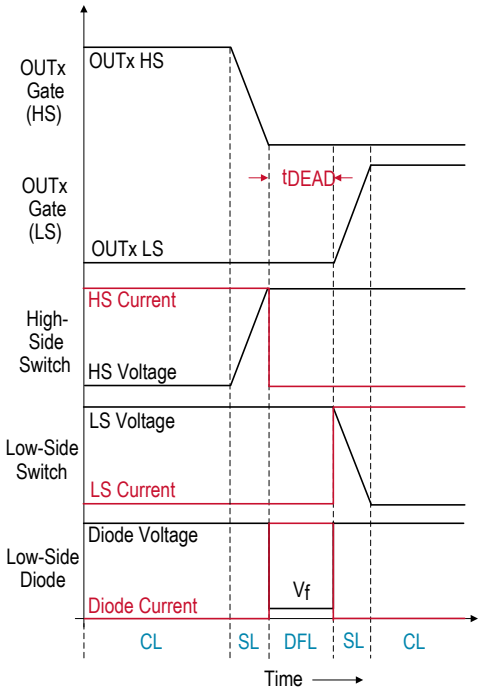

Figure 51: Power Dissipation Waveforms

Conduction Losses

Conduction losses depend primarily on the average phase current and on-state resistance of the high-side and low-side MOSFETs. The on-state resistance of the MOSFET varies with temperature, as shown in Figure 52, which assumes a linear variation of on-state resistance that considers the value of on-state resistance at 25°C and 125°C.

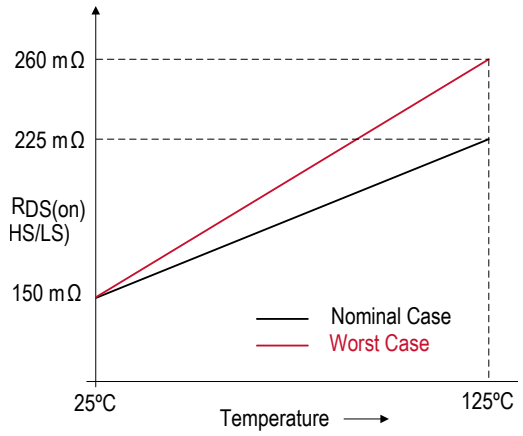

Figure 52: MOSFET $R_{DS(On)}$ Variation with Temperature

The equations for the variation of $R_{ds(on)}$ (nominal value, $R_{Nom@TJ}$) with temperature can expressed as:

Equation 16:

$$\left(R_{Nom@TJ} - 150\right) = \left(\frac{225-150}{125-25}\right)\left(T_J - 25\right)$$
$$\Rightarrow R_{Nom@TJ} = 0.75 \times T_J + 131.25 \quad .$$

Similarly, the maximum value of $R_{ds(on)}$ ($R_{Max@TJ}$) is expressed as:

Equation 17:

$$\left(R_{Max@TJ} - 150\right) = \left(\frac{260-150}{125-25}\right)\left(T_J - 25\right)$$
$$\Rightarrow R_{Max@TJ} = 1.1 \times T_J + 122.5 \quad .$$

The conduction losses (nominal and maximum) in a single MOSFET are expressed as:

Equation 18:

$$P_{Con\_nom} = \left(I_{Phase}\right)^2 R_{Nom@TJ}$$
$$= \left(I_{Phase}\right)^2 \left(0.75 \times T_J + 131.25\right) mW \text{; and}$$

Equation 19:

$$P_{Con\_max} = \left(I_{Phase}\right)^2 R_{Max@TJ}$$
$$= \left(I_{Phase}\right)^2 \left(1.1 \times T_J + 122.5\right) mW \quad .$$

Switching Losses

The power loss due to the PWM switching frequency depends on the slew rates, i.e., rise time (t_{RISE}), fall time (t_{FALL}), supply voltage (V_{BB}), motor phase current (I_{phase}), and PWM switching frequency (f_{PWM}).

The switching losses (rise time and fall time losses) in a single MOSFET during the rise and fall times can be expressed as:

Equation 20:

$$P_{SW\_rise} = \frac{1}{2} \times V_{BB} \times I_{Phase} \times t_{Rise} \times f_{PWM}$$; and

Equation 21:

$$P_{SW\_fall} = \frac{1}{2} \times V_{BB} \times I_{Phase} \times t_{Fall} \times f_{PWM}$$.

Total switching loss in a switch is calculated as:

Equation 22:

$$P_{SW} = P_{SW\_rise} + P_{SW\_fall}$$.

The measured rise and fall times of the A89303 device are shown in Table 2.

Table 2: Measured Rise and Fall Times

Parameter	Value
Rise Time (HS) t_{rise_HS}	85 ns
Fall Time (HS) t_{fall_HS}	55 ns
Rise Time (LS) t_{rise_LS}	93 ns
Fall Time (LS) t_{fall_LS}	70 ns

Diode Freewheeling Losses

To avoid shoot-through current, a dead time is inserted in the synchronous- switching operation of the high-side and low-side MOSFETs. During this dead time, to cater to the continuous inductor current in motor, the low side-diode conducts as shown in Figure 51. Losses associated with the diode are dependent on the phase current (I_{phase}) and the forward voltage drop of the diode (V_F):

Equation 23:

$$P_{DIODE} = V_F \times I_{Phase} \times t_{Dead} \times f_{PWM}$$.

Quiescent Power Losses

Quiescent current is the active current used by the IC to operate various circuitries. This constitutes continuous power drop (P_Q), which is expressed as:

Equation 24:

$$P_Q = V_{BB} \times I_Q$$.

Total Power Dissipation in IC

The total power dissipation in the IC can be considered using an example: a fuel pump with motor phase current of 1 A (I_{phase}), nominal supply voltage (V_{BB}) of 12 V, PWM frequency (f_{PWM}) of 25 kHz, and ambient operating temperature (T_A) of 65°C.

The total conduction loss is calculated for two MOSFETs that conduct all the time to achieve the 120-degree mode of conduction (trapezoidal control) of the BLDC motor. Therefore, the total conduction (nominal and maximum) loss is calculated as:

Equation 25:

$$P_{TCon\_nom} = 2 \times \left(I_{Phase}\right)^2 \left(0.75 \times T_J + 131.25\right)$$

$$= 2 \times (1)^2 \left(0.75 \times 65 + 131.25\right) = 360\,mW$$; and

Equation 26:

$$P_{TCon\_max} = 2 \times \left(I_{Phase}\right)^2 \left(1.1 \times T_J + 122.5\right)$$

$$= 2 \times (1)^2 \left(1.1 \times 65 + 122.5\right) = 388\,mW$$.

The low-side switch is fully turned on and the PWM is applied to the high-side switch. Hence, switching loss corresponds

to a single switch (high-side) that exhibits both rise-time and fall-time losses, calculated as:

Equation 27:

$$P_{SW\_rise\_HS} = \frac{1}{2} \times V_{BB} \times I_{Phase} \times t_{Rise\_HS} \times f_{PWM}$$
$$= \frac{1}{2} \times 12 \times 1 \times 85n \times 25k = 12.75\,mW$$; and

Equation 28:

$$P_{SW\_fall\_HS} = \frac{1}{2} \times V_{BB} \times I_{Phase} \times t_{Fall\_HS} \times f_{PWM}$$
$$= \frac{1}{2} \times 12 \times 1 \times 55n \times 25k = 8.25\,mW$$.

Therefore, total switching loss is calculated as:

Equation 29:

$$P_{SW} = P_{SW\_rise\_HS} + P_{SW\_fall\_HS}$$
$$= 12.75 + 8.25 = 21\,mW$$.

The diode freewheeling loss is calculated for the dead time of 400 ns as:

Equation 30:

$$P_{DIODE} = V_F \times I_{Phase} \times t_{Dead} \times f_{PWM}$$
$$= 0.7 \times 1 \times 400n \times 25k = 7\,mW$$.

The nominal and the maximum quiescent power losses are calculated for the nominal (8.5 mA) and maximum (12 mA) quiescent current as:

Equation 31:

$$P_{Q\_nom} = V_{BB} \times I_Q = 12 \times 8.5m = 102\,mW$$; and

Equation 32:

$$P_{Q\_max} = V_{BB} \times I_{Q\_max} = 12 \times 12m = 144\,mW$$.

Hence, the total power dissipation (nominal and maximum) is calculated as:

Equation 33:

$$P_{Total\_nom} = P_{TCon\_nom} + P_{SW} + P_D + P_{Q\_nom}$$
$$= 360 + 21 + 7 + 102 = 490\,mW$$; and

Equation 34:

$$P_{Total\_max} = P_{TCon\_max} + P_{SW} + P_D + P_{Q\_max}$$
$$= 388 + 21 + 7 + 144 = 560\,mW$$.

Therefore, the junction temperature (nominal and maximum) is calculated as:

Equation 35:

$$T_{J\_nom} = T_A + P_{Total\_nom} \times R_{\theta JA\_ET}$$
$$= 65 + 0.490 \times 40 = 84.6^o C$$; and

Equation 36:

$$T_{J\_max} = T_A + P_{Total\_max} \times R_{\theta JA\_ET}$$
$$= 65 + 0.560 \times 40 = 87.4^o C$$.

Power Dissipation in Board Components

There are two options for reverse battery protection—connect a Schottky diode or a PMOS FET. The Schottky resistor is cost-effective but has higher power loss. The PMOS option is more expensive but has significantly reduced power loss.

Power dissipation in a Schottky diode is calculated as:

Equation 37:

$$P_{Sck} = V_{F\_Sck} \times I_{DC}$$
$$= 0.3 \times 1 = 0.3\,W$$.

Power dissipation in a PMOS FET is calculated as:

Equation 38:

$$P_{PMOS} = (I_{DC})^2 \times R_{DSon\_PMSOS}$$
$$= (1)^2 \times 50\,m = 50\,mW$$.

The other heat-dissipating component on the PCB is the sense resistor. The location of the sense resistor (i.e., its proximity to the IC), can directly impact the junction temperature of the IC. The power dissipation of a sense resistor is calculated as:

Equation 39:

$$P_{RSEN} = (I_{DC})^2 \times R_{SEN}$$
$$= (1)^2 \times 25\,m = 25\,mW$$.

LAYOUT GUDELINES

A schematic for the automotive fuel pump using the A89303 for fixed-speed operation is shown in Figure 53.

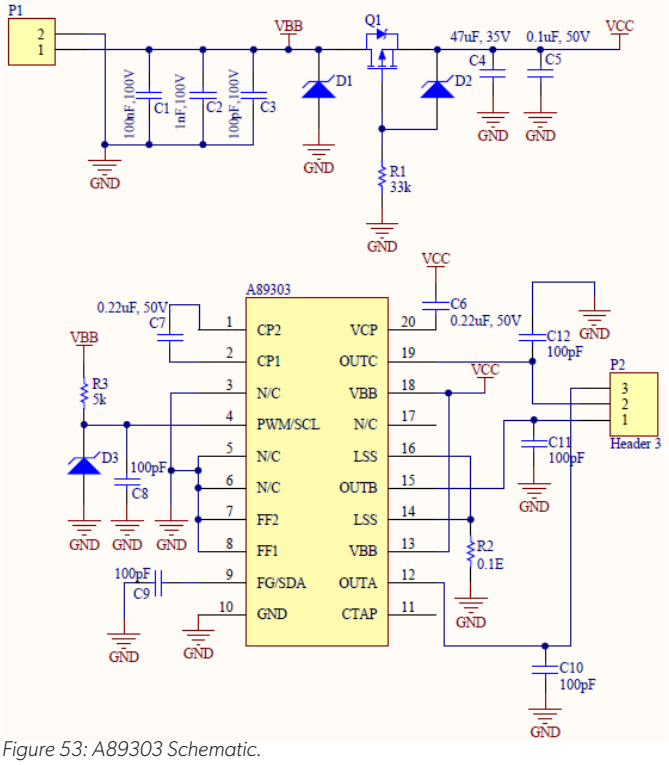

Figure 53: A89303 Schematic.

The various components, including placement guidelines and impact to EMI and thermal characteristics, are:

- C1, C2, C3—Optional EMI Capacitors: These capacitors can be included to eliminate noise in a frequency of concern.
- D1—Surge Protection Diode: This transient voltage suppressor (TVS) diode manages the voltage surge on the battery due to load dump. The sizing of this diode is determined based on the peak power that needs to be absorbed.
- Q1, D2 and R1—Reverse Battery Protection: This circuitry is for reverse battery protection using a PMOS FET to avoid extra power loss in the Schottky diode. D2 and R1 are the biasing components for controlling the PMOS.
- C4—Bulk Capacitor: This high-capacitance-value capacitor must provide enough energy to the A89303 device during transients such that the voltage drop is minimal.
- C5—Bypass Capacitor: This capacitor is used to eliminate high-frequency ripple at the VBB node of the A89303 device. The recommended placement of this capacitor is closer to the VBB pin.
- C6, C7—Charge Pump Capacitors: These capacitors are required for the proper operation of the A89303 charge pump. Because the capacitor operates at higher switching frequency, the recommended placement for these capacitors is as close as practicable to the pins.
- R3, D3—PWM Pin Connection to VBB: If the PWM pin needs to be connected to 3.3 V/5 V for 100% duty operation, this circuit can be used to protect the PWM pin from higher voltage.
- C8, C9—Optional EMI Capacitors for I2C Lines: these optional capacitors can be used to mitigate noise emitted from the I2C communication lines. For programming, a pull-up resistor must be connected to the SCL/SDA lines. Resistor placement is recommended on the production programming board, as explained in the next section, not on the board shown in Figure 53.
- C10, C11, C12—Optional EMI Capacitors for Motor Connections: These optional capacitors can be used to mitigate noise emitted by the motor connection traces.
- R2—Sense Resistor: This is the motor current sense resistor. The package of this resistor should be selected based on the necessary power dissipation. For effective power dissipation, use of a larger thermal plane is recommended for this resistor.

The top layer layout (component placement and routing) of the QFN package is shown in Figure 54 and Figure 55. The bottom layer layout (component placement and routing) is shown in Figure 56 and Figure 57.

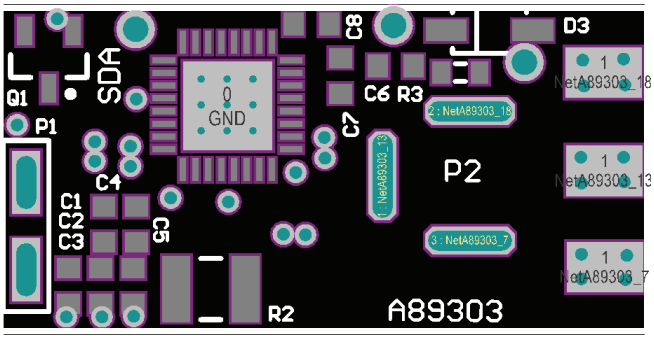

Figure 54: QFN Top Layer Layout (Component)

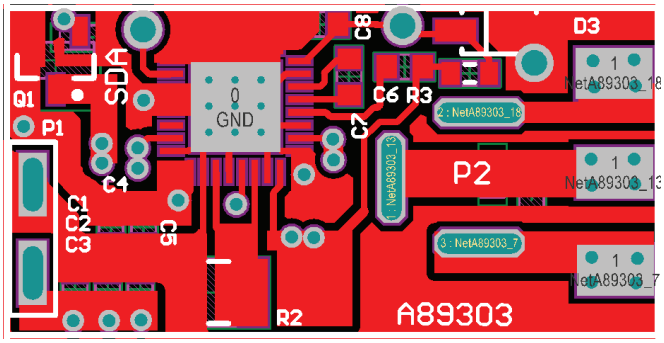

Figure 55: QFN Top Layer Layout (Routing)

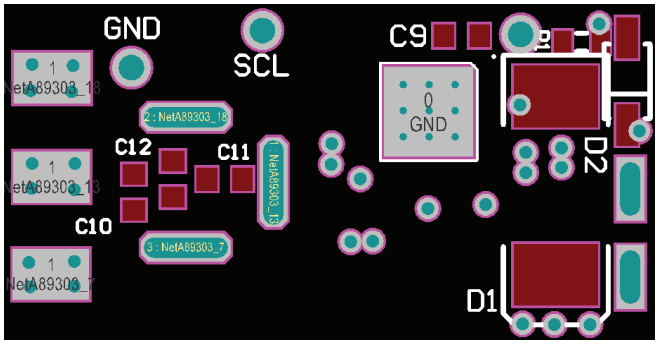

Figure 56: QFN Bottom Layer Layout (Component)

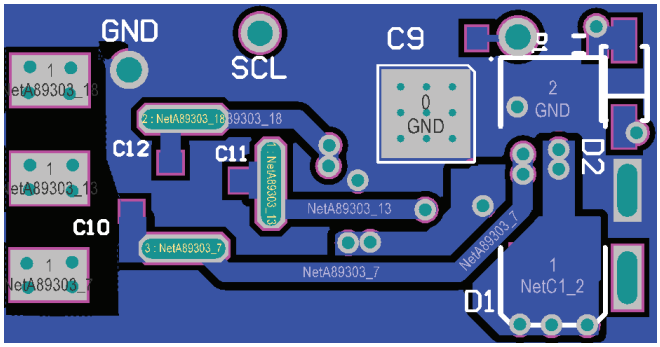

Figure 57: QFN Bottom Layer Layout (Routing)

The top layer layout (component placement and routing) of the HTSSOP package is shown in Figure 58 and Figure 59. The bottom layer layout (component placement and routing) is shown in Figure 60 and Figure 61.

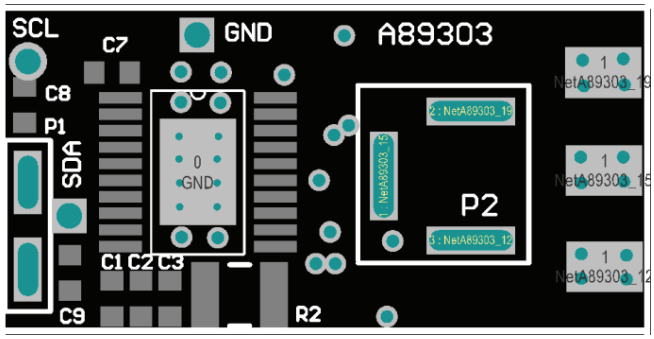

Figure 58: HTSSOP Top Layer Layout (Component)

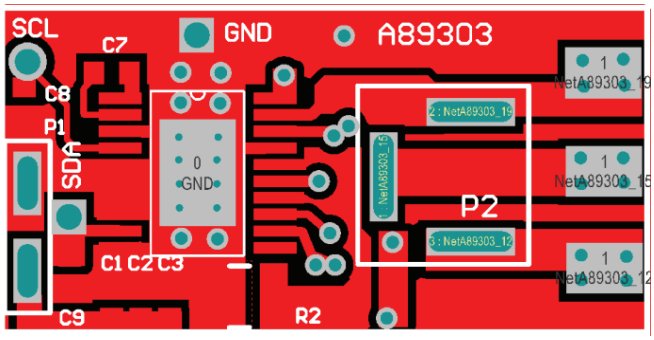

Figure 59: HTSSOP Top Layer Layout (Routing)

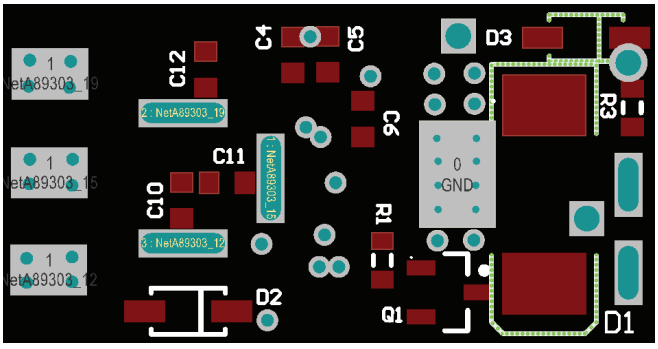

Figure 60: HTSSOP Bottom Layer Layout (Component)

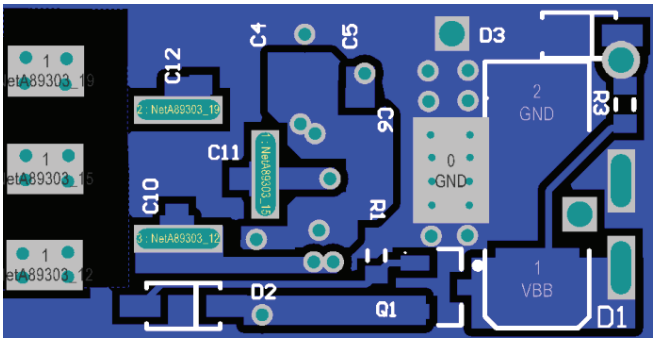

Figure 61: HTSSOP Bottom Layer Layout (Routing)

PROGRAMMING PERSPECTIVE

The SCL/SDA pins in the A89303 devices are open-drain pins; therefore, a pull-up resistor is required, as shown in Figure 62. During power up, the contents of the EEPROM are loaded into the IC registers. These registers are temporary storage locations and are cleared when the IC is powered down. The device can be tuned for the desired performance, then the EEPROM locations can be programmed.

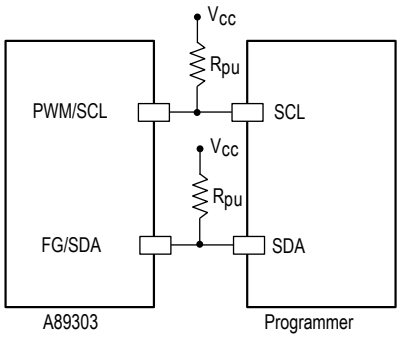

Figure 62: A89303 Programming Connection.

The evaluation board also provides an option for programming the external device, as shown in Figure 63. Switch SW1 releases the connection to the onboard A89303 device, when set in the external configuration. Thereby, the SCL and SDA pins of the external device can be directly connected to the SCL/SDA pins of the evaluation module for its programming.

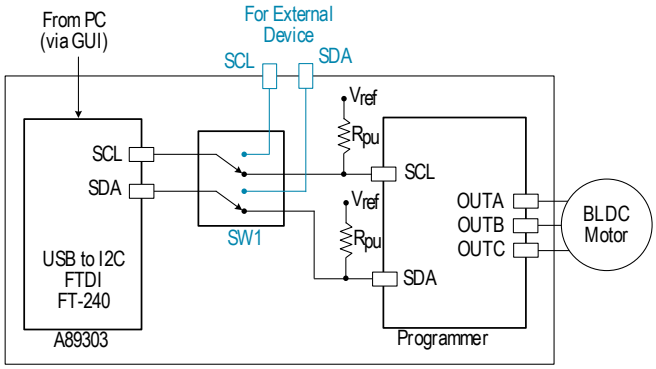

Figure 63: A89303 Evaluation Module for Programming an External Device

The A89303 GUI is shown in Figure 64. Various parameters are configured using the GUI. Once the parameters are tuned, they can be written to the EEPROM using the Write All Settings to EEPROM button.

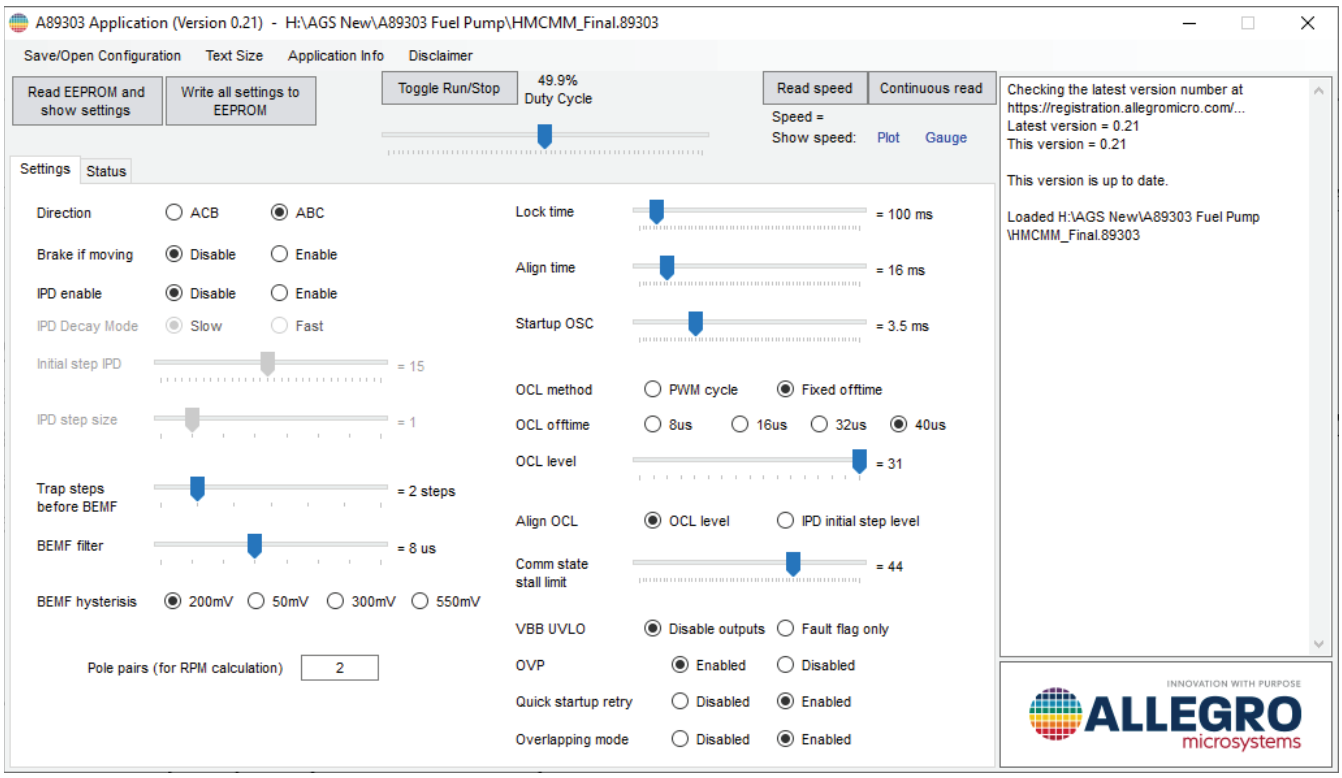

Figure 64: A89303 GUI

MOTOR SPEED LIMITATION AND SOLUTION

This section presents the relation between the speed and the number of turns of the motor as an initial approximation.

The back-emf of the BLDC motor is proportional to the number of turns as well as the speed and is given as:

Equation 40:

$$E_{BEMF} \propto \omega \times N = k_b \omega N ,$$

where k_b is the back-emf constant in volts/(rpm-turns).

The voltage drop in the BLDC motor is expressed as:

Equation 41:

$$V_{dc} = I_{Ph} \times R_{L-L} + L_{L-L} \frac{d}{dt}\left(I_{Ph}\right) + E_{BEMF} .$$

Using the back-emf from Equation 40, Equation 41 can be expressed as:

Equation 42:

$$V_{dc} = I_{Ph} \times R_{L-L} + L_{L-L} \frac{d}{dt}\left(I_{Ph}\right) + k_b \omega N .$$

For a fan-type load application, the load torque (T_L) is proportional to the square of the speed (ω), expressed as:

Equation 43:

$$T_L \propto \omega^2 = k_\omega \omega^2 ,$$

where k_ω is the torque constant expressed in N-m/sq-A.

Moreover, the electromagnetic torque (T_e) is expressed as a function of load torque (T_L) as:

Equation 44:

$$T_e = T_L + J \frac{d}{dt}(\omega) + B\omega ,$$

where J is the moment of inertia, and B is the viscous coefficient.

Using Equation 43, Equation 44 can be expressed as:

Equation 45:

$$T_e = k_\omega \omega^2 + J \frac{d}{dt}(\omega) + B\omega .$$

Moreover, the electromagnetic torque is also proportional to the motor phase current, expressed as:

Equation 46:

$$T_e \propto I_{Ph} = k_i I_{Ph} .$$

Therefore, equating Equation 45 to Equation 46 gives:

Equation 47:

$$k_i I_{Ph} = k_\omega \omega^2 + J \frac{d}{dt}(\omega) + B\omega .$$

From this, the value of phase current can be expressed as:

Equation 48:

$$I_{Ph} = \frac{k_\omega}{k_i}\omega^2 + \frac{J}{k_i}\frac{d}{dt}(\omega) + \frac{B}{k_i}\omega .$$

For simplicity, considering the rate of change of speed at steady-state operation as zero and neglecting the drop due to viscous coefficient, the phase current is expressed as:

Equation 49:

$$\omega^2 = \frac{k_i}{k_\omega} I_{Ph} = k_{\omega i} I_{Ph} \Rightarrow I_{Ph} = \frac{\omega^2}{k_{\omega i}} .$$

Using this expression of I_{ph} in Equation 42 allows the DC bus voltage to be expressed as:

Equation 50:

$$V_{dc} = \frac{\omega^2}{k_{\omega i}} \times R_{L-L} + L_{L-L} \frac{d}{dt}\left(\frac{\omega^2}{k_{\omega i}}\right) + k_b \omega N .$$

If the voltage drop due to the inductor is neglected for simplicity, Equation 48 becomes:

Equation 51:

$$k_{\omega i} V_{dc} = R_{L-L}\omega^2 + k_b k_{\omega i} \omega N .$$

Rewriting the equation in quadratic form gives:

Equation 52:

$$\left(R_{L-L}\right)\omega^2 + \left(k_b k_{\omega i} N\right)\omega - k_{\omega i} V_{dc} = 0 .$$

The roots of this quadratic equation fit the form:

Equation 53:

$$\omega = \frac{-\left(k_b k_{\omega i} N\right) \pm \sqrt{\left(\left(k_b k_{\omega i} N\right)^2 + 4R_{L-L} k_i V_{dc}\right)}}{2R_{L-L}} .$$

The only possible positive root of this equation is:

Equation 54:

$$\omega = \frac{\sqrt{\left(\left(k_b k_{\omega i} N\right)^2 + 4R_{L-L} k_i V_{dc}\right)} - \left(k_b k_{\omega i} N\right)}{2R_{L-L}} .$$

Therefore, Equation 54 shows the initial approximation of the change in speed with number of turns.

An example of a motor can be considered with line-to-line resistance of 2 Ω, rated speed of 12 000 rpm, number of turns of 1000, rated current of 1 A, DC bus voltage of 12 V, and back-emf voltage of 10 V. The values of k_b and k_ω are calculated from Equation 40 and Equation 49. The number of turns is varied by ±10%, and the variation of speed is plotted using Equation 54, as shown in Figure 65.

As shown in Figure 65, as the number of turns reduces, the speed of the BLDC motor increases. Hence, the number of stator turns can be reduced to a limited extent to increase the speed of the BLDC motor. This plot is an ideal estimate: It does not consider many nonidealities and nonlinearities of the system. Such nonlinearities include the inductance drop, impact of rate of change of speed and moment of inertia, and impact of viscous coefficient and inductance saturation in increasing the current when the motor turns are reduced.

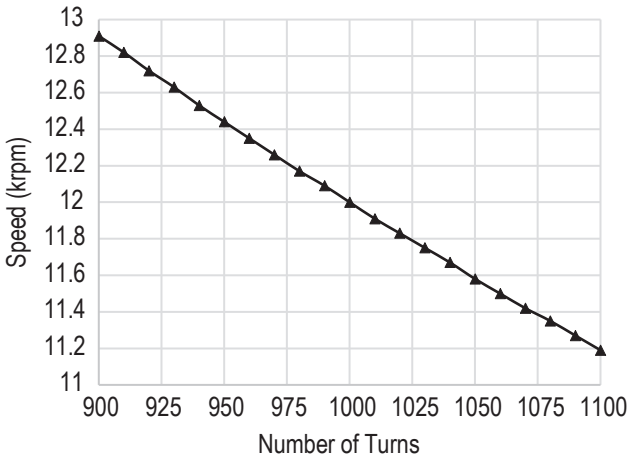

Figure 65: Variation of Speed with Number of Turns

CONCLUSION

This application note has explored key considerations in design of a BLDC motor driver for the automotive fuel pump application. Advantages such as fast startup, smaller footprint, less EMI emission, and advanced features like the overlapping mode make this device ideal for automotive fuel pump application. The A89303 device provides easy configuration of various parameters, with options that benefit motor-drive performance, power dissipation, thermal behavior, layout, and device programming.

Revision History

Number	Date	Description	Responsibility
–	June 26, 2023	Initial release	V. Bist, S. Wekhande
1	July 1, 2024	Removed footnote (page 4).	J. Henry

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM