IN-PAD VIAS IMPROVE THERMAL PERFORMANCE FOR ALLEGRO CURRENT SENSORS

INTRODUCTION

This application note discusses the effectiveness of using in-pad vias and other additional printed circuit board (PCB) layout techniques to improve heat dissipation for current sensors with integrated conductors. Optimal heat sinking is necessary to protect the IC from exceeding its maximum junction temperature of 165°C.

BACKGROUND

Integrated Allegro Current Sensor Packages

The Allegro current sensor IC families are fully-integrated current sensing solutions and are leading the industry in power density. Current enters the package through the integrated conductor leads (IP+, IP-) and the resistance of that conductor generates heat that must be dissipated in order to maintain an IC temperature of less than 165°C. Without any active heat sinking, the main source of passive heat sinking is into the PCB itself. The more metal that is directly connected to the integrated conductor, the more effective the heat sinking becomes. The goal of this application note is to illustrate how to maximize the passive heat sinking into the PCB.

A summary of integrated current sensor packages included in this application note is provided in Table 1. A comparison of the die heating from 25°C versus sensed current applied to the package is shown in Figure 1 and Figure 3 for various Allegro current sensor packages. A comparison of the die heating from 125°C versus sensed current applied to the package is shown in Figure 2 and Figure 4.

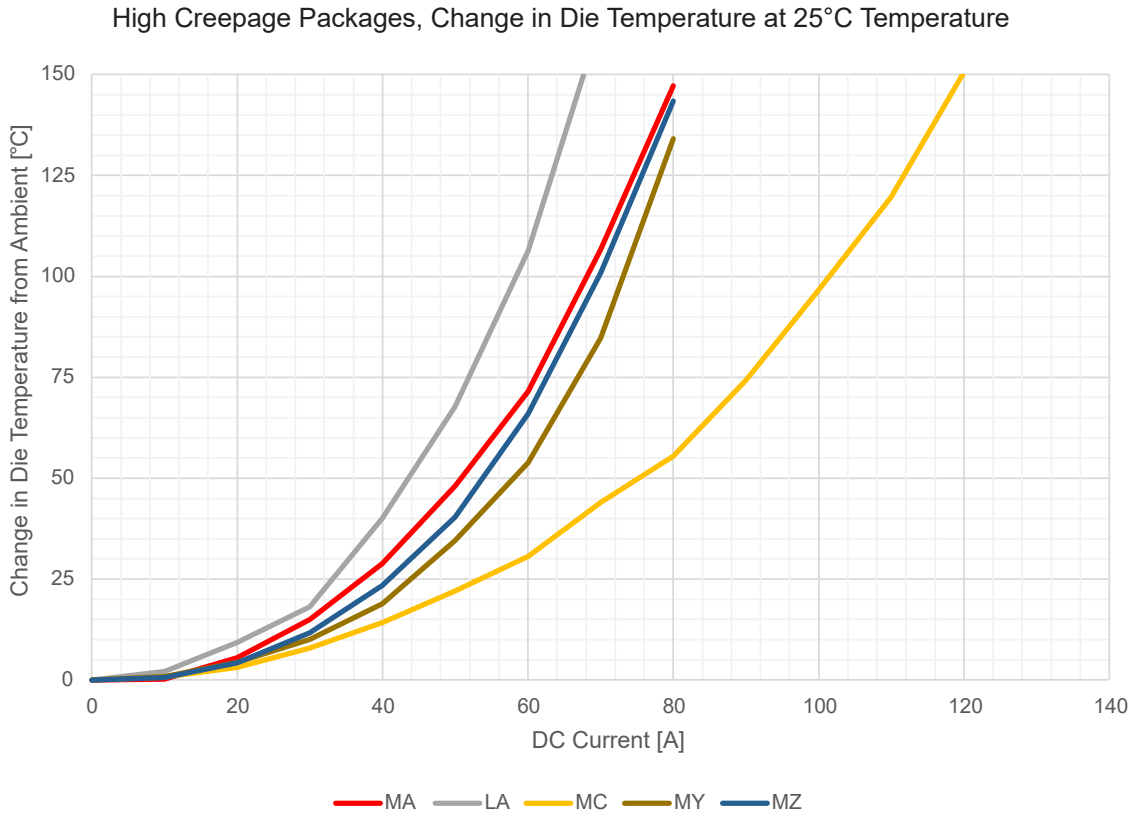


Figure 1: In-Pad Vias—Allegro lab results for high creepage packages, 25°C

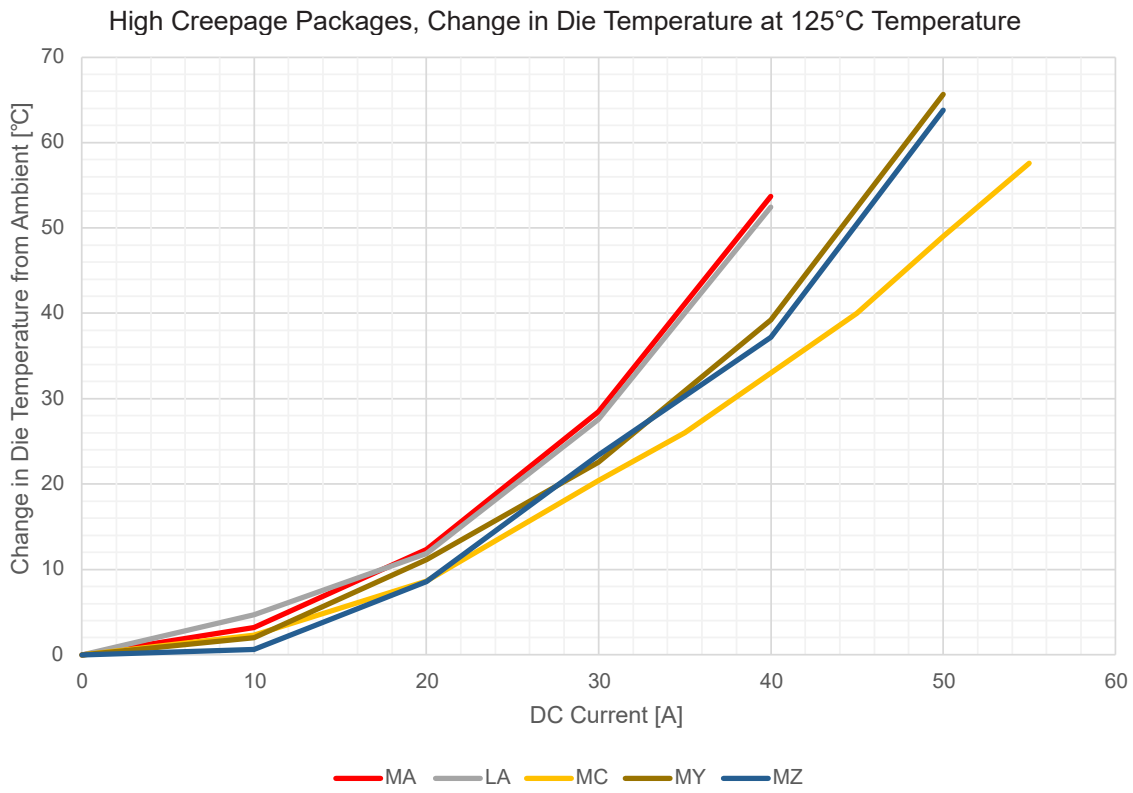


Figure 2: In-Pad Vias—Allegro lab results for high creepage packages, 125°C

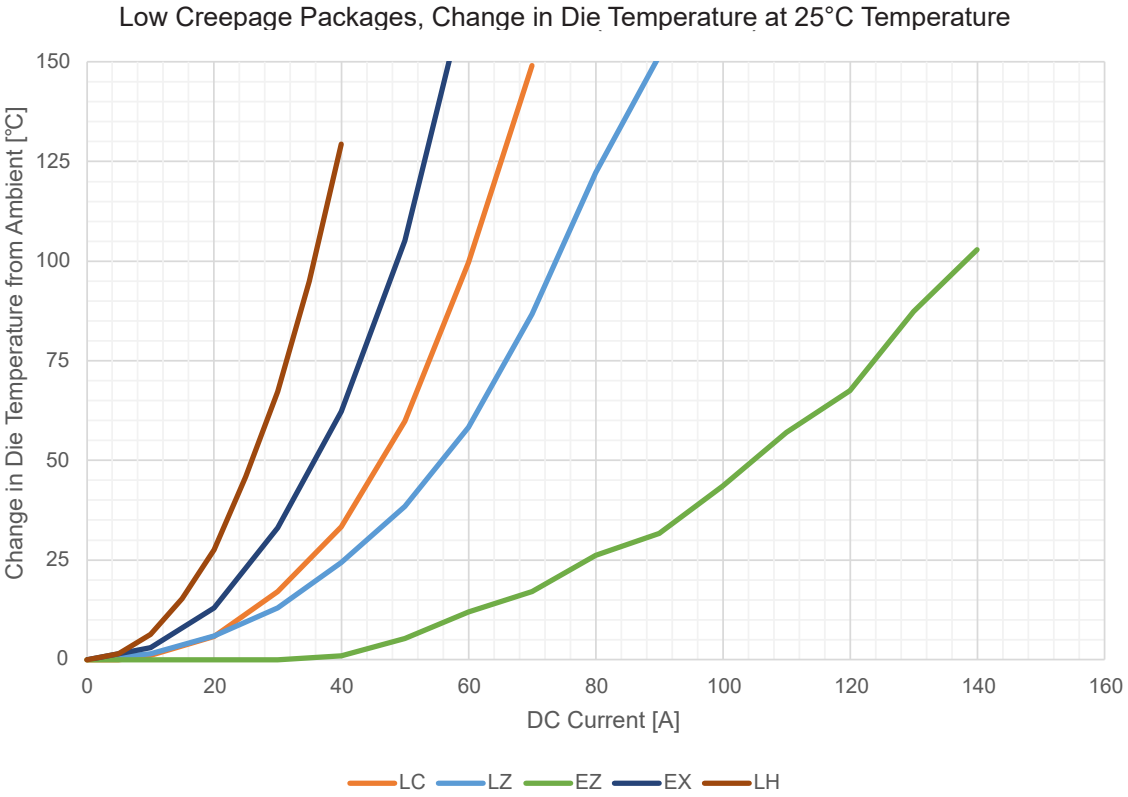


Figure 3: In-Pad Vias—Allegro lab results for low creepage packages, 25°C

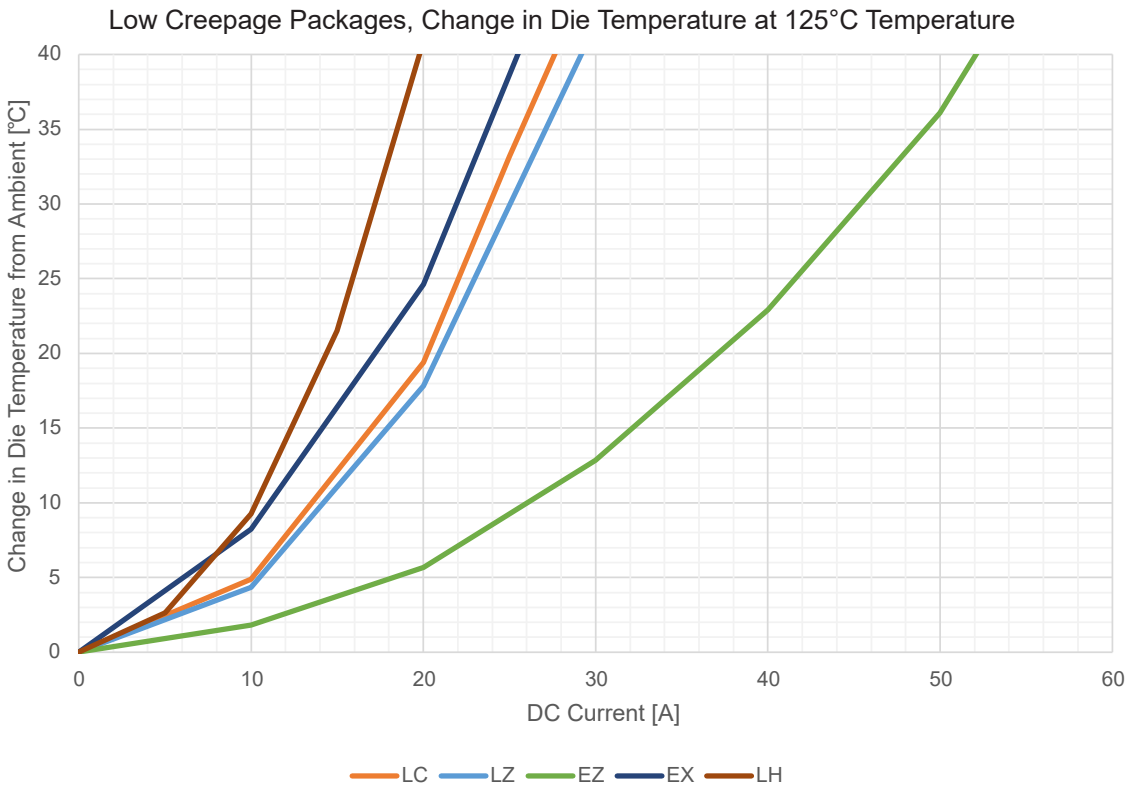
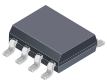
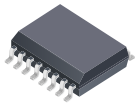
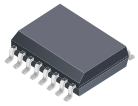
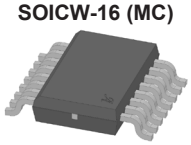


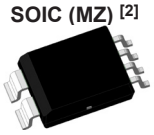
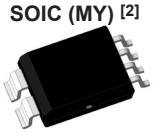
Figure 4: In-Pad Vias—Allegro lab results for low creepage packages, 125°C

Table 1: Summary of Allegro Integrated Current Sensor Packages

Package	Primary Conductor Resistance [mΩ]	Size [1] [mm³]	Working Voltage for Functional Isolation [V_{RMS}]	Working Voltage for Basic Isolation [V_{PK}]	Working Voltage for Reinforced Isolation [V_{PK}]	Thermal Characteristics [3][4]	
						Junction to Ambient, $R_{\theta JA}$ [°C/W]	Junction to Top, Ψ_{JT} [°C/W]
6-Pin SOIC (LZ) [2] 	0.68	4.89 × 3.9 × 1.47	–	1188	594	16	0
SOIC-8 (LC) 	1.2	4.9 × 6 × 1.62	–	420	—	19	0
SOICW-16 (MA) 	0.85	10.3 × 10.3 × 2.65	—	1550	800	20	2
SOICW-16 (LA) 	1	10.3 × 10.3 × 2.65	—	870	—	16	–2
SOICW-16 (MC) 	0.27	11.3 × 13 × 3.01	—	1618	809	19	2
7-Pin QFN (EZ) 	0.1	4 × 4 × 1.45	100	—	—	55	7
QFN (EX) 	0.6	3 × 3 × 0.75	100	—	—	18	1
SOT23–W 5 Pin (LH) [2] 	2	2.9 × 2.975 × 1	—	300	—	32	3

[1] PCB layout recommendations can be found in the Appendix.
[2] Certification is pending.
[3] $R_{\theta JA}$ is a system-level thermal resistance to heat flow from power dissipated in the package between the circuitry on the chip (junction) and ambient environment. $R_{\theta JA}$ is commonly based on a two-layer PCB layout as specified in JESD51. In the case of current sensors, the JEDEC standard board is inadequate because it is unable to handle high currents. $R_{\theta JA}$, as defined here, is based on the Allegro application boards mentioned in this application note, which are optimized for carrying high currents. $R_{\theta JA}$ is highly dependent on the PCB and environment and is good for rough estimation of thermal performance of a package and for comparison between packages.
[4] Ψ_{JT} is a thermal metric for power dissipated in the package, defined as the difference between the junction temperature and the maximum temperature at the top of the package. It is a useful shorthand way to determine junction temperature by measuring the temperature on the top of the package. This metric is highly dependent on the PCB and environment. Technically, it is not a resistance and can be negative. This is because, unlike most IC packages, the primary heat source (the integrated current loop) is not in the same location as the die, which can result in negative values when the top of the package is hotter than the junction.

Table 1: Summary of Allegro Integrated Current Sensor Packages (continued)

Package	Primary Conductor Resistance [mΩ]	Size [1] [mm³]	Working Voltage for Functional Isolation [V_{RMS}]	Working Voltage for Basic Isolation [V_{PK}]	Working Voltage for Reinforced Isolation [V_{PK}]	Thermal Characteristics [3][4]	
						Junction to Ambient, $R_{\theta JA}$ [°C/W]	Junction to Top, Ψ_{JT} [°C/W]
6-Pin Fused Lead SOIC (MZ) [2] 	0.8	10.31 × 5.85 × 2.54	—	1550	800	18	–1
6-Pin Fused Lead SOIC (MY) [2] 	0.9	10.31 × 5.85 × 2.54	—	1414	707	17	–3

[1] PCB layout recommendations can be found in the Appendix.
[2] Certification is pending.
[3] $R_{\theta JA}$ is a system-level thermal resistance to heat flow from power dissipated in the package between the circuitry on the chip (junction) and ambient environment. $R_{\theta JA}$ is commonly based on a two-layer PCB layout as specified in JESD51. In the case of current sensors, the JEDEC standard board is inadequate because it is unable to handle high currents. $R_{\theta JA}$, as defined here, is based on the Allegro application boards mentioned in this application note, which are optimized for carrying high currents. $R_{\theta JA}$ is highly dependent on the PCB and environment and is good for rough estimation of thermal performance of a package and for comparison between packages.
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BENEFITS OF IN-PAD VIAS

The in-pad via technique implements a via directly under a surface-mount component pad connecting the inner layers to the top layer. When using in-pad vias, the vias should be filled so the solder does not become sucked into the hole, reducing the solder joint quality. The most common via filling material is nonconductive. The via can be also filled with electrically and thermally conductive material, which tends to be more expensive than nonconductive material, and provides marginal improvements over nonconductive fill material. Vias under the copper pads of the LZ package versus no vias under the copper pads are shown in Figure 5 and Figure 6.

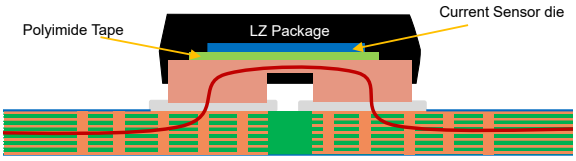

Figure 5: Vias Under Copper Pads, using LZ package in example

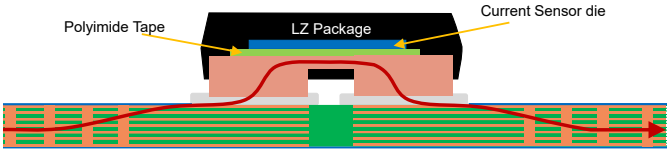

Figure 6: No Vias Under Copper Pads, using LZ package in example

In-pad vias are commonly used for thermal performance, space saving, and reduction in electrical resistance:

1. Thermal Performance: By placing the vias directly under the integrated conductor leads, the PCB pad acts as both a current conductor and thermal relief, as shown in Figure 5. In this way, the heat generated by the component can be more efficiently dissipated through the board to the inner metal layers, where the heat can spread more efficiently away from the part.
2. Saving Space: Placing the via directly in the pad can be useful in some designs where space is at a premium, allowing components to be placed closer together. However, in the case where the vias are used to dissipate heat, additional components near the integrated conductor should be minimized to maximize the amount of unbroken metal planes for heat conduction.
3. Reduced PCB Trace Resistance: Because the vias directly connect multiple layers in parallel in the PCB, the resistance from the current source to the integrated conductor leads can be minimized on the PCB, as shown in Figure 5. Resistance in the current-carrying layers around the IC creates heat in the PCB (see Figure 9). This raises the temperature of the PCB around the IC, reducing the temperature gradient for the heat to flow away from the IC.

RESULTS OF IN-PAD VIAS VERSUS NO IN-PAD VIAS

Allegro MicroSystems offers evaluation boards with optimized heat sinking for quickly evaluating Allegro current sensors in a lab environment (shown in Figure 9). In the comparisons that follow, data are collected from two of these evaluation boards. The boards are identical except one has in-pad vias and the other has vias outside of the pads. (The two evaluation boards used to evaluate the LC/LZ package are shown in Figure 7 and Figure 8; for all other packages, reference layout views showing in-pad vias are provided in the Appendix. Note that these figures are not to scale). The size of each via used in the in-pad via is 0.5 mm. The via type is IPC-4761 Type VII: Filled & Capped Via. Nonconductive via fill material is used. These boards have six layers, each being 2 oz copper weight.

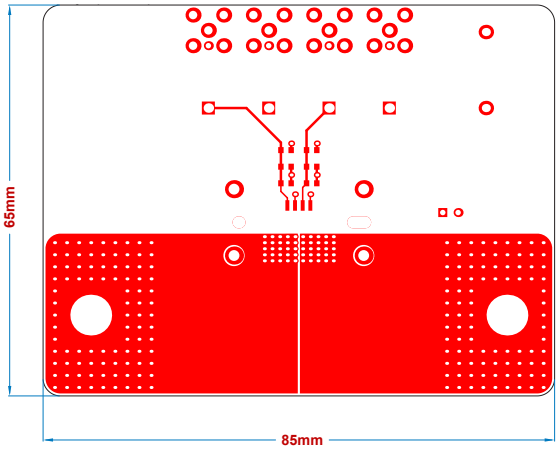

Figure 7: LC/LZ PCB Layout Reference View With In-Pad Vias

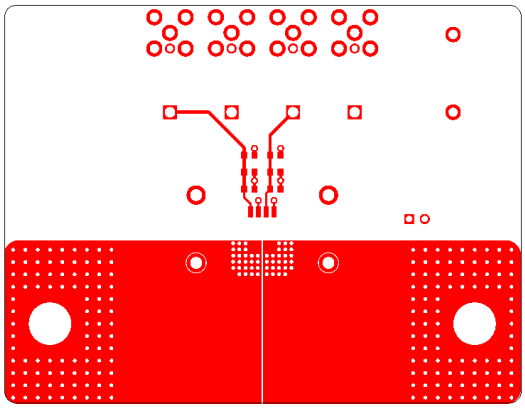

Figure 8: LC/LZ PCB Layout Reference View Without In-Pad Vias

Testing was conducted at 25°C and 125°C ambient temperatures. The current was conducted to the PCB through 2AWG gauge cables. DC current was then sent through the integrated conductor leads of the device. Die temperature was measured by using the on-chip temperature sensor located after it came to thermal equilibrium. (Note that the on-chip temperature sensor is not available to customers). The change in die temperature was determined by subtracting the measured ambient temperature from the measured die temperature.

Comparison of the thermal performance with and without in-pad vias for all the packages can be observed in the plots that follow. Additionally, comparison of the thermal performance for 25°C vs. 125°C can be observed in the plots that follow.

NOTE: Only the evaluation boards with in-pad vias were used for testing at 125°C. As mentioned, the die temperature should not exceed 165°C or a rise of 140°C from room temperature (140°C + 25°C = 165°C).

The data demonstrates that using in-pad vias provides a smaller increase in die temperature than not using in-pad vias. Use of in-pad vias is recommended by Allegro for all current sensors with integrated conductors.

For the most accurate results, Allegro recommends that the parts undergo a standard reflow process instead of hand-soldering. Too much or not enough solder can affect the results. This is especially true for QFN-type packages (EZ and EX) where solder voiding is not visible under the part and can significantly affect the heat sinking to the PCB.

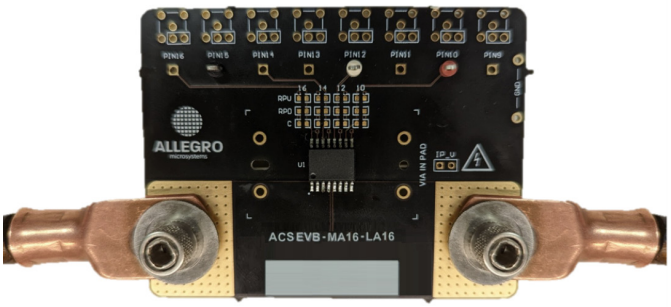

Figure 9: Connection between evaluation board and current-carrying cables

LZ Package

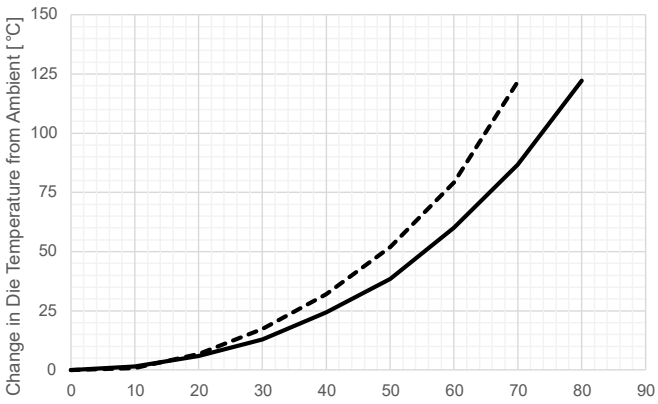

Figure 10: LZ Package Comparison with and without In-Pad Vias

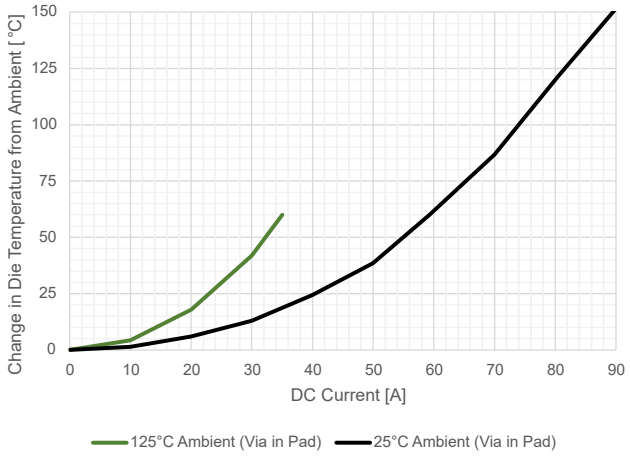

Figure 11: LZ Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

LC Package

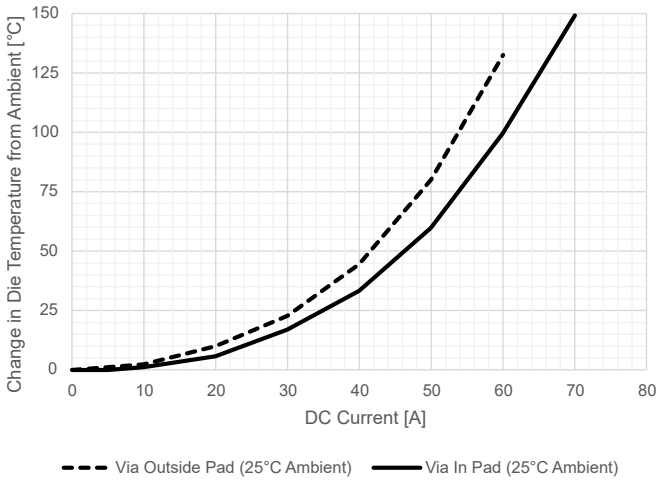

Figure 12: LC Package Comparison with and without In-Pad Vias

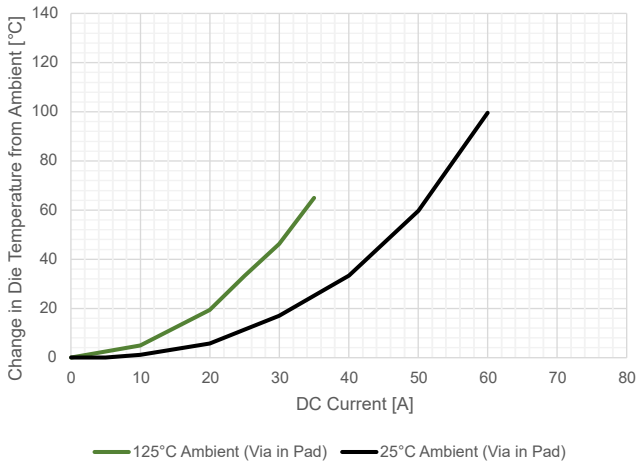

Figure 13: LC Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

MA Package

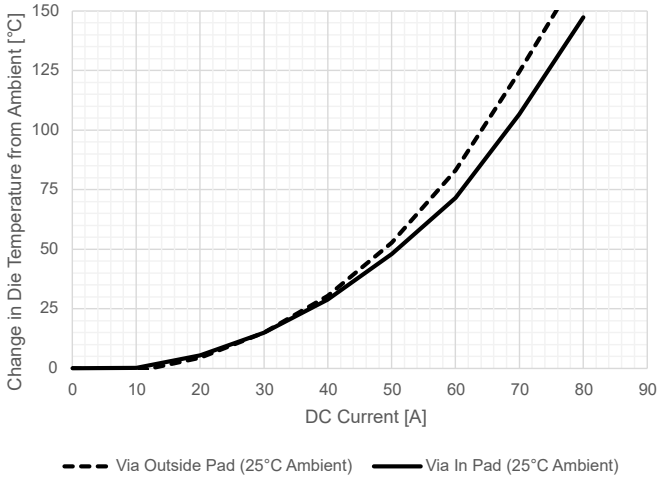

Figure 14: MA Package Comparison with and without In-Pad Vias

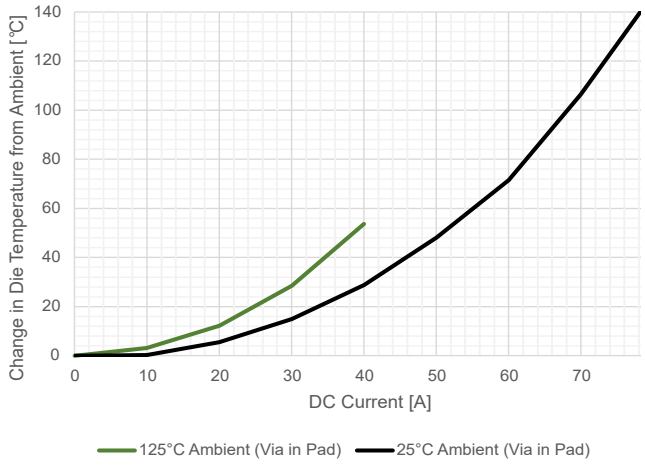

Figure 15: MA Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

LA Package

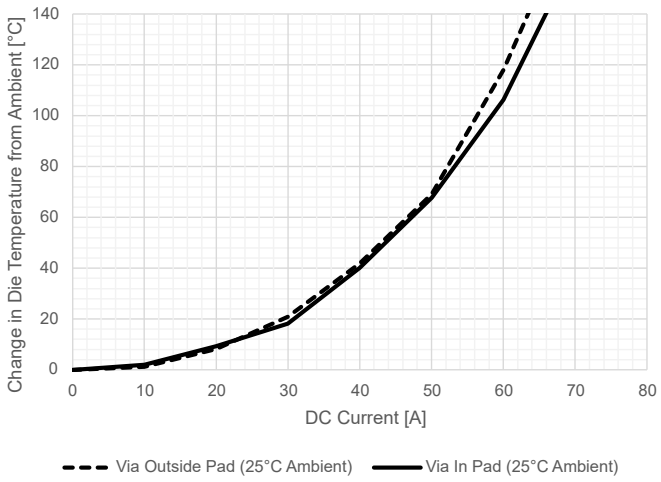

Figure 16: LA Package Comparison with and without In-Pad Vias

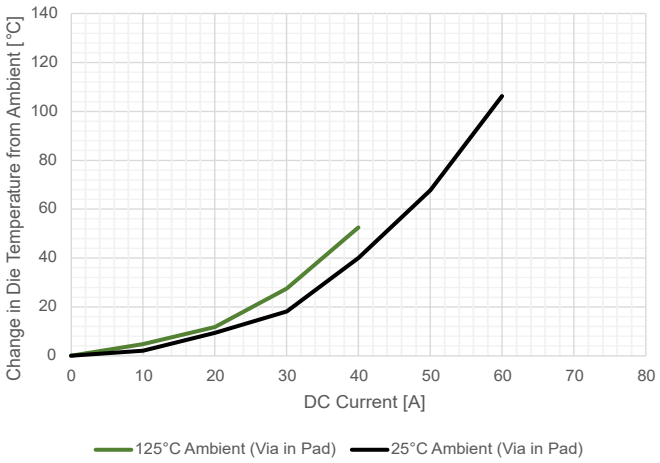

Figure 17: LA Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

MC Package

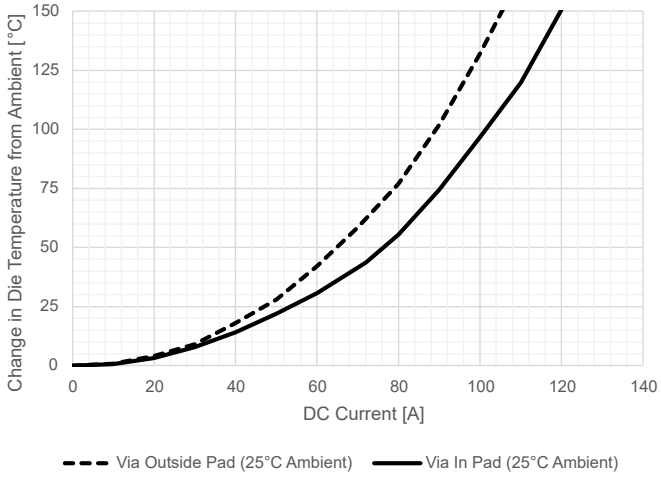

Figure 18: MC Package Comparison with and without In-Pad Vias

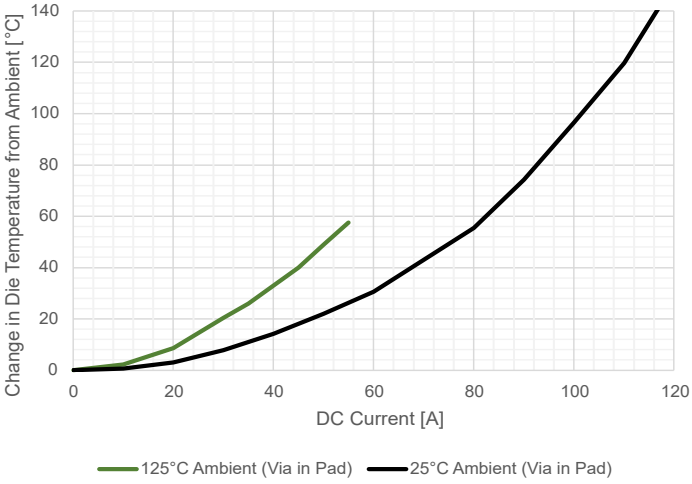

Figure 19: MC Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

EZ Package

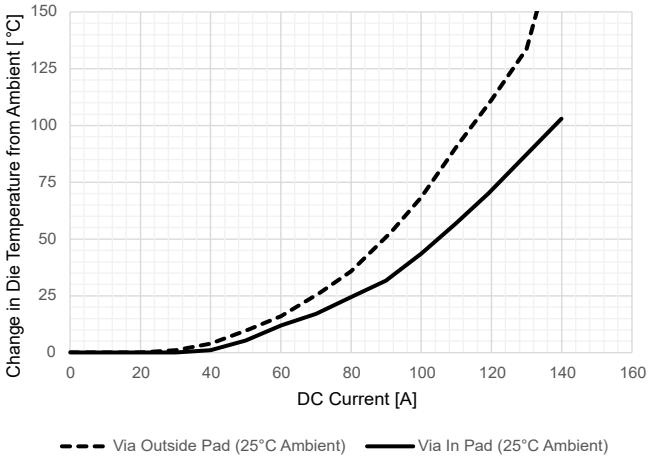

Figure 20: EZ Package Comparison with and without In-Pad Vias

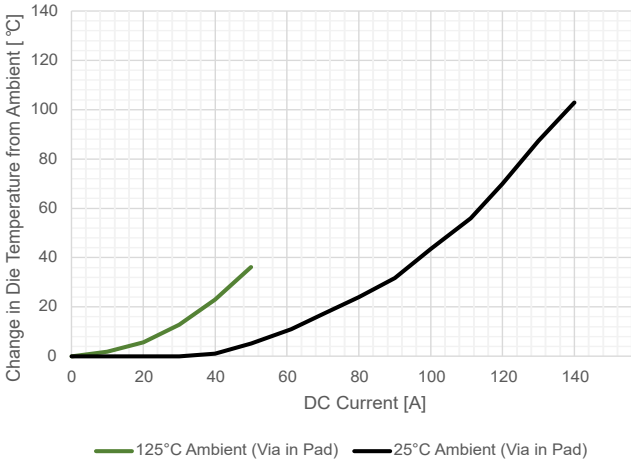

Figure 21: EZ Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

EX Package

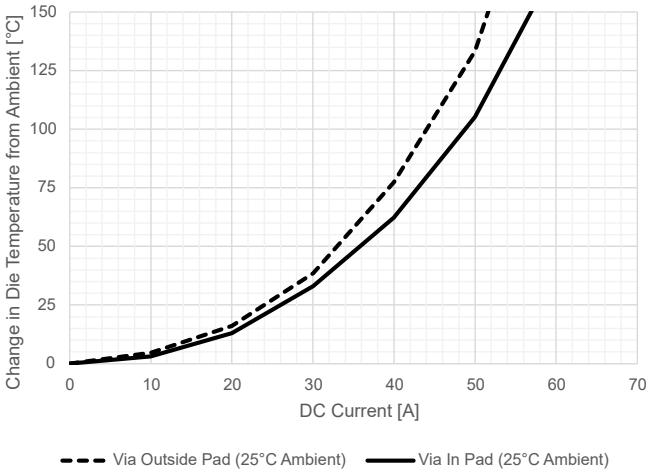

Figure 22: EX Package Comparison with and without In-Pad Vias

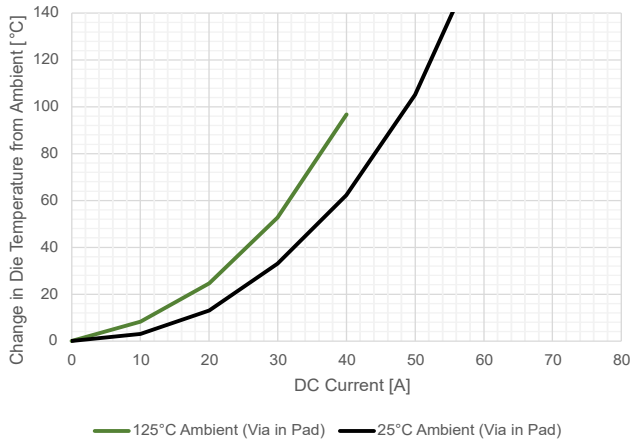

Figure 23: EX Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

LH Package

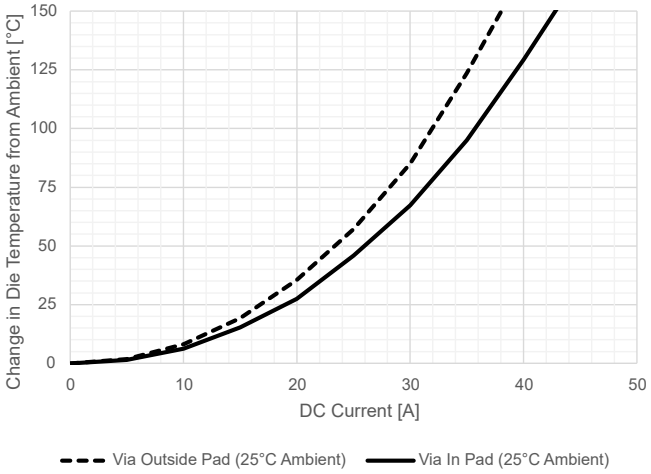

Figure 24: LH Package Comparison with and without In-Pad Vias

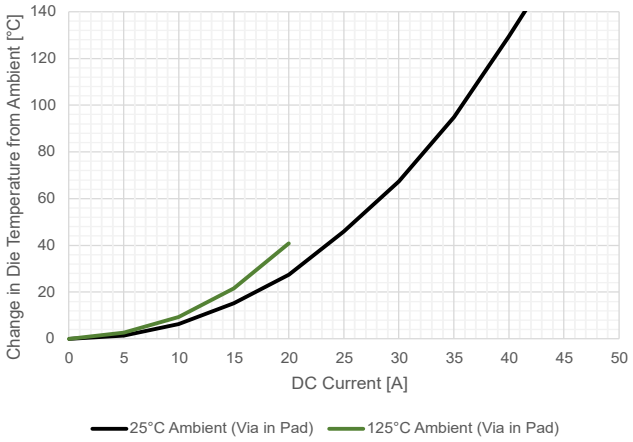

Figure 25: LH Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

MY/MZ Package

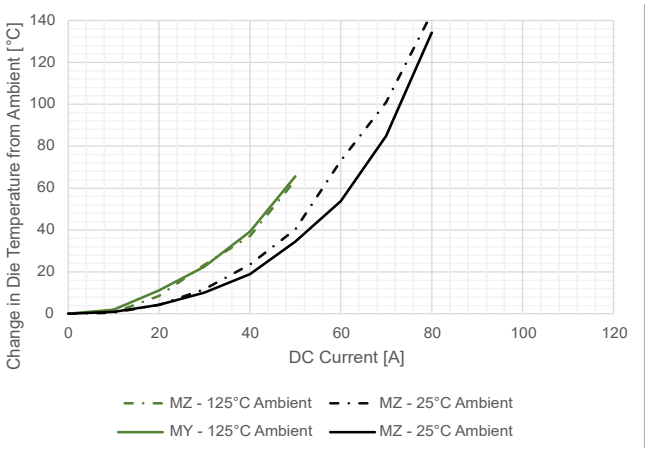

Figure 26: MY/MZ Package Comparison 25°C and 125°C ambient temperatures with In-Pad Vias

Impact of the Temperature Coefficient of Cu

The internal conductor is a copper alloy primarily composed of copper with small amounts of other metals, and thermal behavior can be considered to be similar to pure copper. Copper has a positive resistive temperature coefficient (+0.393 percent per degree C), which means that, as the temperature of the conductor increases, its resistance increases as well. This is an almost 40% increase in the power dissipated in the package for an ambient temperature rise of 100°C with no current applied.

For example, 50 A_{RMS} into the MA package, with a resistance of 0.85 mΩ at 25°C ambient, generates 2.125 W of power inside the package. At 125°C ambient, the power generated increases to 2.95 W. This does not account for the temperature rise due to the power dissipated in the conductor when current flows. This positive feedback is further reason to remove heat efficiently from the package, to reduce the chance of thermal runaway.

Additional Board Layout Considerations

There are additional important considerations to consider when designing these evaluation boards:

1. Pad Layout: It is recommended to completely overlap the top copper layer with the primary current pads to optimize thermal performance, leaving only a small gap separating the IP+ from the IP– internal conductor pins. The size and quantity of the vias in the overlapping area should be maximized based on the design rules for the PCB manufacturing process.
2. Thermal Management: Additional passive heat-sinking or active-cooling techniques at the system level may be necessary to dissipate heat away from the current sensor, allowing the junction temperature to remain at less than 165°C. For isolated applications, it is not advisable to add heat sinks to the top of the package, because these could compromise the creepage distance of the package, unless proper high-voltage isolation methodologies are followed. Because most dielectric insulating materials are also good thermal insulators, adding isolation between the package and heat sink generally reduces any heating-sinking efforts. Passive heat sinking through the top of the package can be problematic, and heating through the PCB is the preferred method.
3. Component Placement: Having other components that generate significant amounts of heat near the current sensor can reduce the temperature gradient that allows heat to flow away from the current sensor. The best design practice is to space out the heat-generating components as much as practical.
4. Copper Layers: Thicker copper layers have two benefits—better heat conduction away for the part and lower electrical resistance that creates heat. Maximizing the thickness of each layer and maximizing the number of layers that are in direct contact with the current sensor through in-pad vias minimizes the die junction temperature.
5. Trace Width: High-current traces must be wide enough to keep voltage drop and inductance to a minimum and wide enough to prevent excessive heating. The largest practical PCB traces and board area usage around the current sensor is recommended.
6. Solder Stencil: Voids in the solder on the large-current conductor pads (IP+ to IP–) for the QFN EZ package increases the resistance of the solder joint and reduces the heat-sinking to the PCB. Voids should be minimized in the solder joint under the package. Voids can be created by solder flux outgassing. By giving the outgassing a way to escape from under the package during solder reflow, voids can be minimized. Adding a grid in the solder stencil creates a path for outgassing to escape from under the package during the wetting process of the reflow.

CONCLUSION

Placing vias under the copper pads of the Allegro current sensor minimizes the current path resistance and improves heat-sinking to the PCB for optimal thermal performance when compared to having vias outside of the pads. Additional standard layout techniques can be implemented to further minimizes die heating in operation of integrated conductor current sensors.

APPENDIX

PCB Layout References

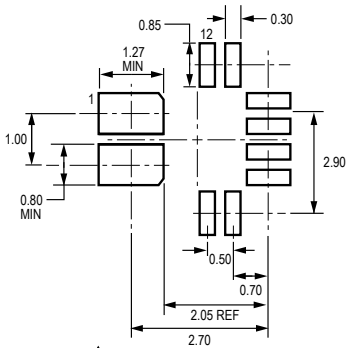

Figure 27: EX PCB Layout Reference View

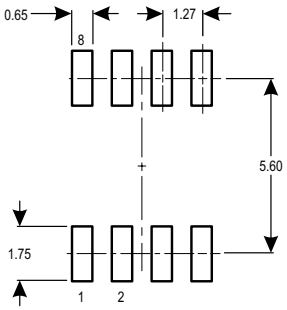

Figure 28: LC PCB Layout Reference View

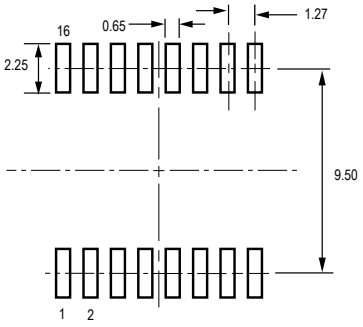

Figure 29: MA/LA PCB Layout Reference View

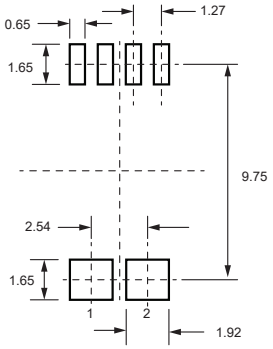

Figure 30: MY/MZ PCB Layout Reference View

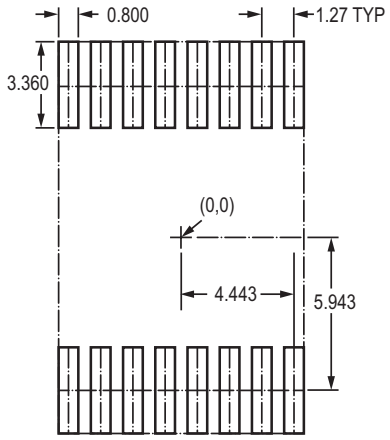

Figure 31: MC PCB Layout Reference View

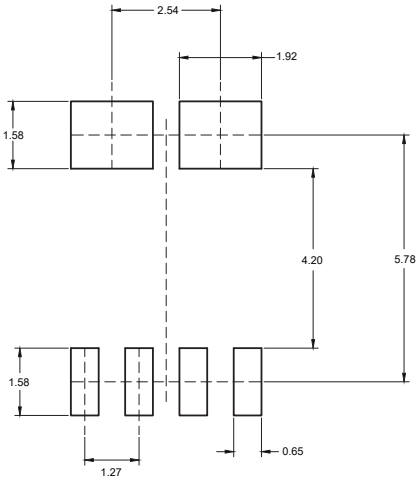

Figure 32: LZ PCB Layout Reference View

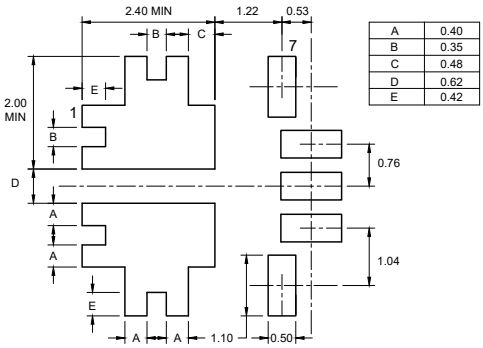

Figure 33: EZ PCB Layout Reference View

Top Layer Showing Layout References of In-Pad Vias

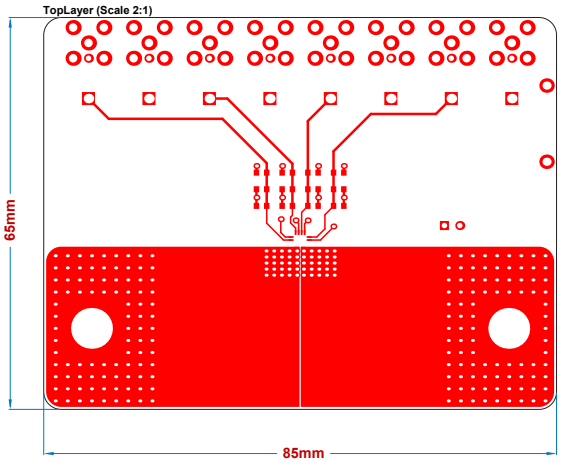

Figure 34: EX PCB Layout Reference View

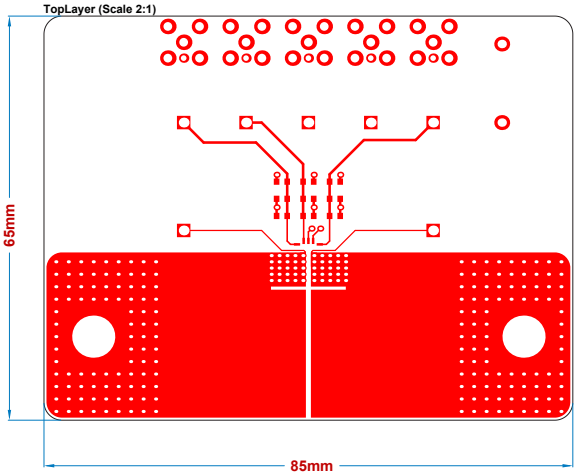

Figure 37: MC PCB Top Layer

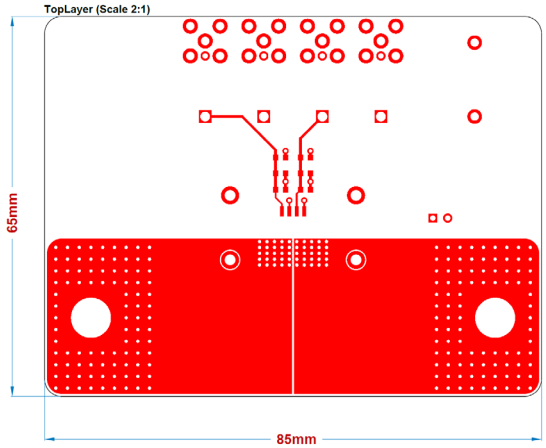

Figure 35: LC PCB Top Layer

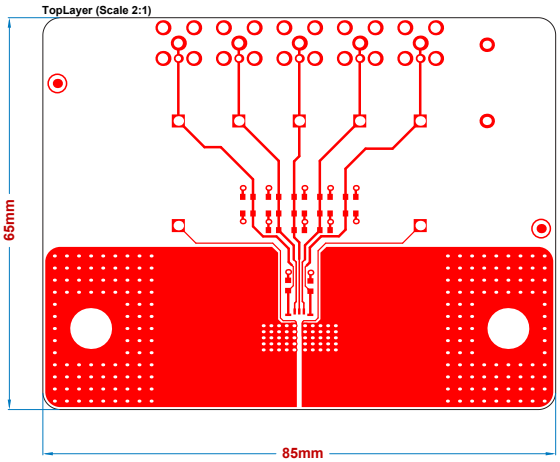

Figure 38: EZ PCB Top Layer

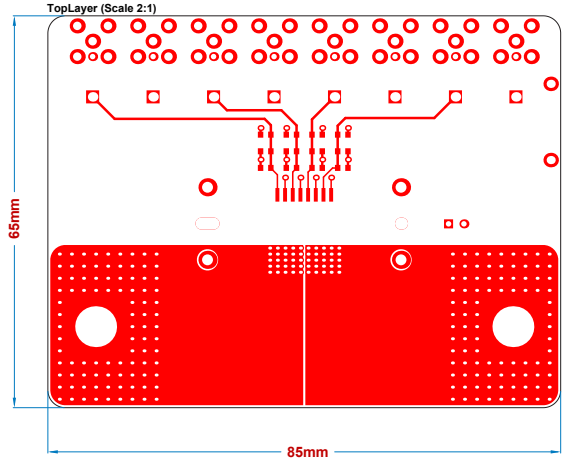

Figure 36: MA/LA PCB Top Layer

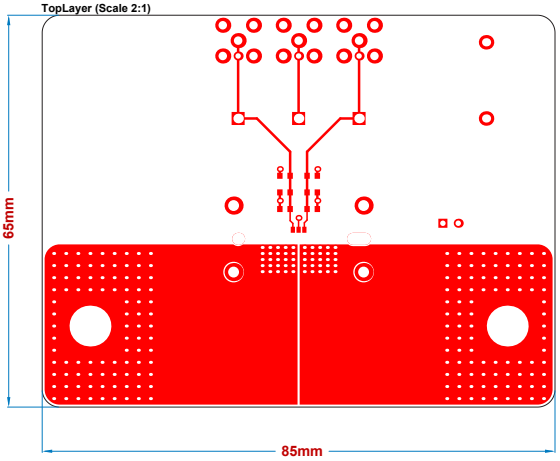

Figure 39: LH PCB Top Layer

Top Layer Showing Layout References of In-Pad Vias

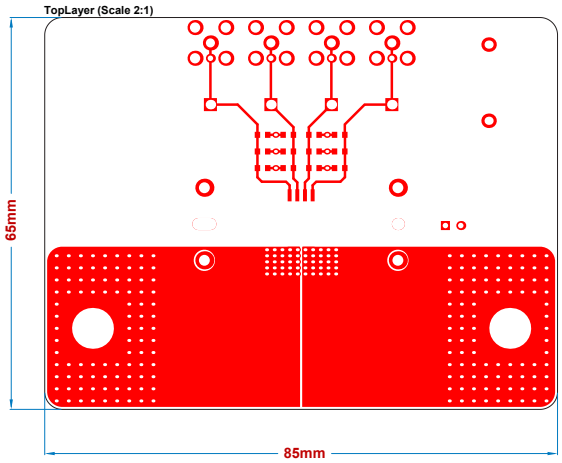

Figure 40: MZ/MY PCB Layout Reference View

Revision History

Number	Date	Description	Responsibility
–	August 28, 2023	Initial release	K. Hampton
1	October 2, 2023	Added Thermal Characteristic values to Table 1 (page 2); added footnote [3] and [4] to Table 1 (page 2); corrected wire gauge size (page 3); minor editorial updates (all pages)	K. Hampton
2	January 24, 2024	Added 125°C application information (page 2), minor editorial updates (all pages)	K. Hampton
3	February 13, 2024	Corrected temperature in Figure 1 caption (page 1)	K. Hampton
4	September 23, 2024	Added LH package (all pages) and made minor editorial changes throughout including elimination of the future tense (will), and standardization of terminology (vias-in-pad changed to in-pad vias to align throughout)	K. Hampton
5	January 9, 2025	Added MY and MZ packages (all pages); updated Figure 1 and Figure 2 (page 1 and 2); updated rounding calculation for thermal resistance metrics (page 4); deleted Related Documentation and Application Support page (page 13)	K. Hampton

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