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PACKAGE THERMAL RESISTANCE FOR ALLEGRO CURRENT SENSORS WITH INTEGRATED CONDUCTORS

Current Sensors System Engineering
Allegro MicroSystems

JUNCTION-TO-AMBIENT THERMAL RESISTANCE ($R_{\theta JA}$)

For any semiconductor, the die temperature cannot exceed the maximum junction temperature specified in the datasheet for extended periods of time. For Allegro integrated current sensors, 165°C is the maximum junction temperature, while many competing products are limited to 150°C. If the temperature exceeds the 165°C limit specified in the datasheet, there is a risk that the performance of the PN junctions on the device will change, thus affecting the performance of the IC and/or the long-term reliability of the part. Thermal resistance, $R_{\theta JA}$ (thermal resistance between junction and ambient), of integrated circuit packages is an industry standard metric for determining what the die temperature will be under certain conditions. By knowing the $R_{\theta JA}$ for a package and the ambient temperature, the junction temperature can be determined for a given power dissipated in the package.

Usually, $R_{\theta JA}$ is based on JEDEC-standard boards, which can be helpful for relative thermal performance between packages. However, for a particular application, standard $R_{\theta JA}$ numbers can be misleading because heat dissipation is a strong function of the PCB and the ambient environment, as well as the package construction. This is especially true for high-power applications where power-optimized PCBs and specialized packages like the Allegro current sensors are often used. For power components, $R_{\theta JA}$ should be determined based on a PCB that has been optimized for thermal performance for comparison purposes or, ideally, on the board to be used in the application being evaluated.

This application note discusses: 1) the Allegro integrated current sensor package constructions (MA, MC, LA, LZ, EZ and LH) and how they affect thermal metrics; 2) industry-standard thermal metrics; 3) methods that can be used for thermal measurements to quantify the metrics in a particular application; and 4) thermal results of the Allegro current sensor evaluation boards.

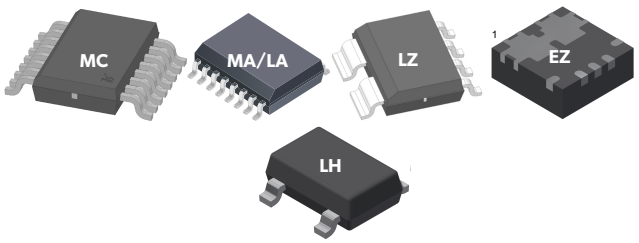

Figure 1: Allegro packages discussed in this application note (not to scale)

PACKAGE CONSTRUCTION AND THERMAL MODEL

Allegro integrated current sensors come in two basic types of packages:

- Die-up constructions (MA, MC, and LH packages), where the die sits directly on top of the integrated conductor to sense the magnetic field created by the current in the primary-side internal conductor (IP loop), with a polyimide insulating layer in between. This configuration has wire bonds to connect the secondary side of the device (VDD, GND, and I/O) to the leads (refer to Figure 2, wire bonds shown in white).
- Flip-chip constructions (LA, LZ, and EZ packages), where the top of the die is located closer to the sensor Hall plates, thus increasing magnetic coupling. This configuration uses solder balls to connect the secondary side to the leads (refer to Figure 3, solder ball bonds shown in blue).

Table 1: Allegro Integrated Package Summary

Package	Footprint (mm)	IP Resistance (mΩ)	Size (mm^3)	Configuration
MA	106.1	0.85	10.3 × 10.3 × 2.65	Die-up
MC	146.9	0.27	11.3 × 13 × 3.01	Die-up
LA	106.1	0.68	10.3 × 10.3 × 2.65	Flip-chip
LZ	29.3	1	4.89 × 3.9 × 1.47	Flip-chip
EZ	16	0.1	4 × 4 × 1.45	Die-up
LH	8.6	1.6	2.9 × 2.97 × 1	Die-up

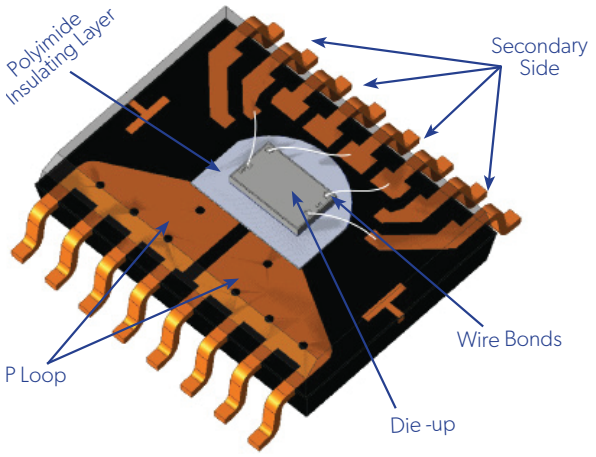

Figure 2: Die-up internal construction showing wire bonds in white

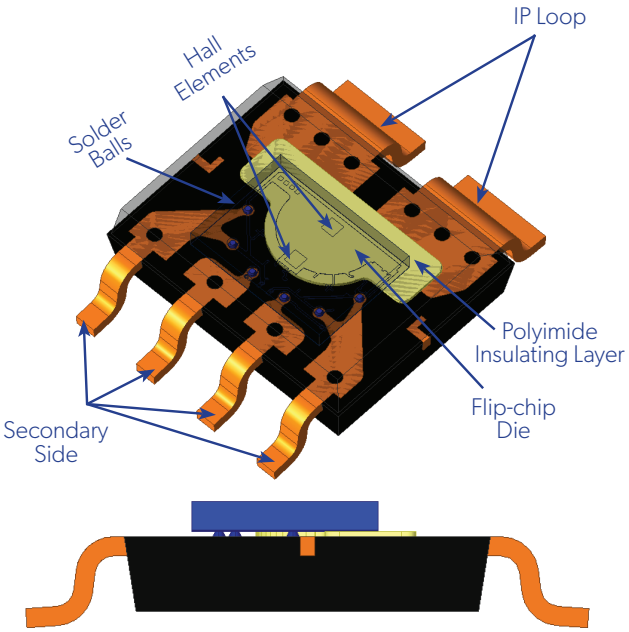

Figure 3: Flip-chip internal construction showing solder balls in blue

With most standard integrated circuit components, the main heat source is the die itself, and the temperature of the heat source (Q) is assumed to be the junction temperature. In the case of current sensors with integrated conductors, the main heat source is the IP loop which can dissipate several watts of power. This is more than a magnitude larger than the power of the die itself, generally no more than 75 mW, which can be ignored for worst-case analysis.

The main heat source in the package is the IP loop, which—as shown in Figure 4—is separated from the die by a gap filled with high-voltage insulation material, the polyimide insulating layer. The polyimide insulating layer (also referred to as the polyimide insulating tape) is a good thermal insulator, so the temperature of the heat source cannot be assumed to be the same as the junction temperature, which is the usual assumption for $R_{\theta JA}$. The thermal resistance of the gap (R_{GAP}) can be larger than the thermal resistance of the surrounding mold compound (R_{MC2}). This has implications for the temperature on the top of the case (T_C). In some cases, the temperature on the top of the package can be the same or lower than the junction temperature (T_J).

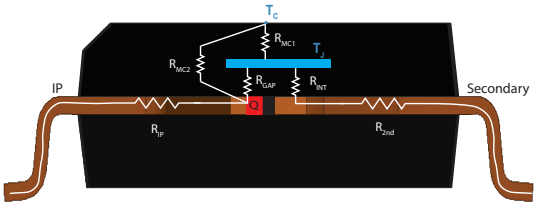

Figure 4: Thermal resistance summary of package

On the other side of the die, there is a thermal resistance for the electrical interconnects (R_{INT}) that connect the die to the secondary side of the copper leadframe, with thermal resistance (R_{2nd}). The gold wire bonds for die-up package configurations have poor thermal conductance through the thin wire bonds. The flip-chip packages with solder balls have short metal interconnects that have good thermal conductance from the die to the copper leadframe. Therefore, the flip-chip packages have better heat sinking from the die to the PCB, in most applications. This assumes that there is minimal air flow or heat sinking through the top of the package. Note that heat sinking the top of the package is usually not recommended for high-voltage applications because it would significantly reduce the creepage and clearance needed for high-voltage isolation.

Because the Allegro current sensors have two leadframes with different thermal resistances and gaps between the heat source and the junctions, this thermal model is much more complex than for standard semiconductors. The thermal model is given here to illustrate the difference between the standard semiconductor model and the Allegro current sensor model (refer to Figure 4). This model is too complex to use in practical applications. Empirical data is needed to obtain an accurate measure of the $R_{\theta JA}$ of the Allegro integrated current sensors.

DEFINING THERMAL METRICS

$R_{\theta JA}$ is a lumped thermal resistance to describe the heat flow from the power dissipated in the package between the circuitry on the die and the ambient environment. Because $R_{\theta JA}$ is a single lumped parameter, it incorporates the entire thermal system including the die, package, PCB, and heat sinking to the ambient environment. Any change in the PCB or environment affects the value of $R_{\theta JA}$. Caution must be

used when considering $R_{\theta JA}$ in any thermal analysis, because misuse of the parameter can result in misleading data.

$R_{\theta JA}$ is commonly based on a two-layer PCB layout, as specified in JESD51. In the case of current sensors, the JEDEC-standard board is inadequate because it is unable to handle the high currents that Allegro integrated current sensor packages are designed for. $R_{\theta JA}$, as defined here, is based on the Allegro evaluation board used in this application note, and these boards are optimized for carrying high current. $R_{\theta JA}$ is highly dependent on the PCB and environment and is compared in various packages later in this application note.

Another set of common metrics used to determine the junction temperature is $R_{\theta JC}$ (junction-to-case) and $R_{\theta JB}$ (junction-to-board), which assume a simple model of the package and are independent of the end application (refer to Figure 5). This model is simplified from the complicated three-dimensional structure in Figure 4 in order to be practical for system-level thermal simulations. The $R_{\theta JC}$ and $R_{\theta JB}$ metrics out of context can be misleading for Allegro current sensors as they assume idealized heat flow from the case to ambient and from the board to ambient. Allegro provides these thermal resistance values for several packages, allowing users to use these metrics in their own thermal models and simulations.

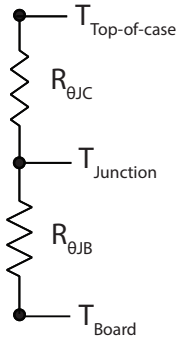

Figure 5: Simple model of thermal simulations

$R_{\theta JC}$ is a package thermal resistance between the junction and top of the package (or convection to ambient) and is useful for calculating the heat dissipation through the top of the package for heat sinking in low-voltage applications. This metric is often determined with very low thermal impedance to ambient and with a slug of copper on the top of the package as specified in JESD51-1 (refer to Figure 6).

$R_{\theta JB}$ is a package thermal resistance between the junction and PCB and is useful for calculating the heat dissipation through the board for heat sinking or convection to ambient. This metric is often determined with very low thermal impedance to ambient with a copper enclosure as specified in JESD51-8 (refer to Figure 7). The simulated results for $R_{\theta JC}$ and $R_{\theta JB}$ for several Allegro current sensor packages are shown in Table 2.

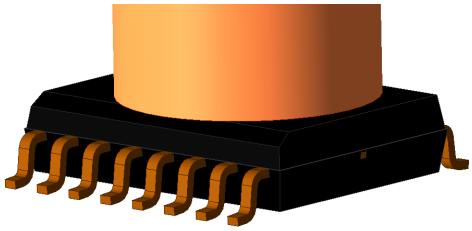

Figure 6: $R_{\theta JC}$ model

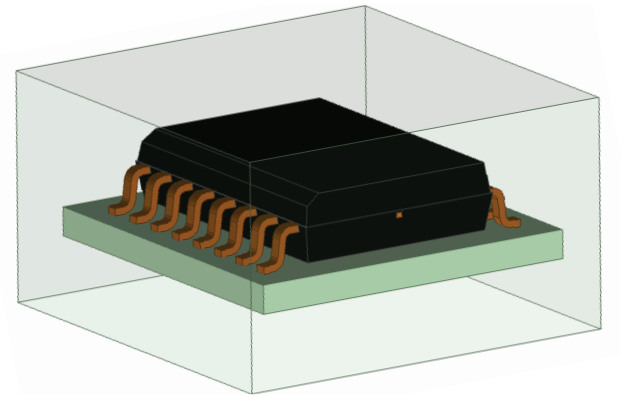

Figure 7: $R_{\theta JB}$ model

Table 2: Allegro Integrated Package Simulated Summary

Package	$R_{\theta JC(simulated)}$	$R_{\theta JB(simulated)}$
MA	14	14
MC	15	7
LA	10	8
LZ	23	12
EZ	70	1
LH	155	19

$R_{\theta JC}$ and $R_{\theta JB}$ are idealized for system-level simulations and are not useful for empirical measurements.

$R_{\theta JC}$ is a function of the surface area of the top of the package; thus, the smallest package described in this application note, the LH package, has the highest $R_{\theta JC}$. The MA package and the MC package have a larger polyimide insulating layer, and the resistance to the top of the package is larger than the LA with the smaller tape.

The $R_{\theta JB}$ is a function of the metal used to dissipate the heat from the die to the evaluation board. The EZ package has the lowest $R_{\theta JB}$ as the package is connected directly to the PCB through the bottom surface of the package. The MC package has a lower $R_{\theta JB}$ than the MA package because the MC package has a leadframe material that is twice as thick as the MA package. The $R_{\theta JB}$ for the LA package is low because it has solder balls to aid in heat sinking using the leads on the secondary side. The LZ package has fewer leads. The MA

and MC packages do not have the benefit of heat sinking with the secondary leads.

Ψ_{JT} is a practical thermal metric of the temperature difference between the junction temperature and the maximum temperature at the top of the package. Because of the complex heat flow paths, Ψ_{JT} must also be determined based on the end application. Once determined for the application, Ψ_{JT} can be used to empirically determine the die temperature by measuring the temperature at the top of the package for different load conditions in the application. Ψ_{JT} is not a resistance and can be negative because the primary heat source is not in the same location as the die, which can result in negative values when the top of the package is hotter than the junction.

Ψ_{JB} is the thermal metric of the temperature difference between the board and the junction, but it is less useful for Allegro integrated conductor current sensors because the heat sinking to the board creates different temperatures at each side of the part due to the package construction previously described.

MEASURING JUNCTION TEMPERATURE

To determine $R_{\theta JA}$ and Ψ_{JT}, and to yield accurate metrics, laboratory measurements of the die temperature and case temperature are needed on a bench setup that closely mimics the final application.

Die Temperature Measurement

Since the die is embedded in a plastic mold compound, the only accurate way to measure die temperature is directly. One technique is to use an electrostatic discharge (ESD) diode from VDD to ground. The voltage across the ESD diode, from VDD to GND or between any unconnected pin and ground varies linearly with temperature for a given current. Using this characterization, the ratio between the change in temperature and the change in voltage ($\Delta V/\Delta T$) can be determined using the setup shown in Figure 8. Note that this does not yield an absolute temperature, but a change from a known ambient temperature.

To determine $\Delta V/\Delta T$, inject a known current (usually approximately 1 mA) into the GND pin across the ESD diode to VDD pin. Measure the voltage change across the diode at two different known ambient temperatures (for accuracy, a wide temperature variation between the two known ambient temperatures is recommended, e.g., 25 °C and 125 °C). The current sensor must be unpowered and the IP loop must not contain current. Before taking the measurements, allow sufficient time for the die to reach thermal equilibrium.

With $\Delta V/\Delta T$ known, the die temperature change from the current ambient condition can be determined by injecting a current into the IP loop and by measuring the ΔV. This provides the most direct measure of the die temperature for the current applied. The drawback, however, is that this method cannot be used in operation: It is intended to be used for engineering evaluation only. Each Allegro current sensor part number must have its $\Delta V/\Delta T$ measured, but performance will be consistent from part to part for the same part number.

External Temperature Measurements

A thermocouple can be used to measure the temperature on the top of the case, T_C. Using a thermocouple can be challenging because the thermocouple is thermally conductive, and it can sink heat, which reduces the temperature measured. Additionally, making a reliable contact requires adhering the thermocouple to the top of the package, which also increases the heat sinking through the thermocouple. The smallest thermocouple available with the smallest amount of thermal epoxy should be used to minimize heat sinking. The benefits to using a thermocouple are that measurements can be performed both while the current sensor is electrically operating and remotely, in a temperature-controlled chamber.

Another way is to measure T_C externally is to use a thermal camera. This method to measure the temperature at the top of the case is easy to perform in an ambient environment but difficult when the current sensor is in a temperature-controlled chamber or other enclosure. For more accurate results using the thermal camera, care must be taken to reduce the effects of emissivity of reflective surfaces (for camera specification, refer to manufacturer documentation). Allegro used the thermal imaging camera for $R_{\theta JA}$ and Ψ_{JT}.

RESULTS OF ALLEGRO CURRENT SENSOR EVALUATION BOARDS

Allegro current sensor (ACS) evaluation boards (EVBs) are available for most package types. The test setup for the MA and LA packages on an ACS EVB is shown in Figure 8. These PCBs have six layers of 2 oz. copper with in-pad vias for the IP pins to maximize copper heat sinking through the PCB. This reduces current-generated heat on the PCB, which aids with heat sinking by keeping the temperature differential between the current sensor and the PCB as high as possible. Testing was performed with 2 AWG wire, which also provides an additional heat sinking path.

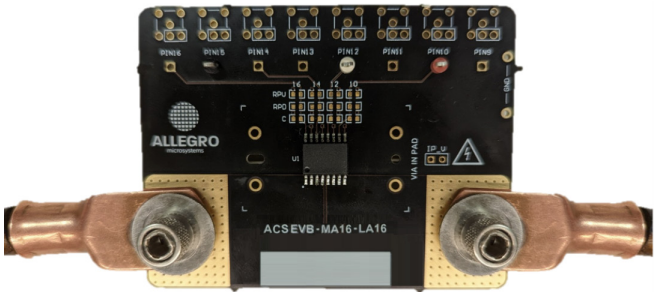

Figure 8: Bench setup

To illustrate the relative heat sinking properties of the packages, 3 W of power was dissipated in each package. For the EZ package, 1.5 W was used because 3 W is beyond its operating range and its PCB is unable to handle that much current. This was performed by measuring the voltage drop across the IP loop and setting the current to generate the desired total wattage in the package. Thermal images of the boards and packages are shown in Figure 10 through Figure 12. Refer to Table 3 for a summary of the currents used to generate the desired wattage.

Table 3: Allegro Integrated Packages—Testing Summary

Package	IP Loop Voltage Drop (V)	Current (A)	Power (W)
MA	0.0532	56	3
MC	0.037	82	3
LA	0.064	47	3
LZ	0.053	56	3
EZ	0.012	124	1.5
LH	0.075	47	3

The MA and MC packages show hot spots on the primary side (IP loop side) of the package, with little heat dissipated on the other side of the package. The LA, LZ, and LH packages show more-uniform heat distribution across the package because the solder balls dissipate heat more efficiently to the other side of the leadframe. The MC package has a leadframe that is two times thicker than the other packages mentioned, and it more-efficiently dissipates heat to the PCB, as evidenced by the higher temperature of the board.

Note that the LZ and MA packages required the same 56 A to achieve 3 W in the package. The LZ package has a lower resistance and better heat sinking to the other side of the package through the solder balls than the MA package. However, the MA package is larger, with more area and thermal mass for heat dissipation. These tradeoffs balance each other out, illustrating that the thermal performance of the package is a complex mix of materials and geometries.

The EZ package shows that heat is more effectively dissipated into the PCB and less through the top of the package, than the leaded packages with larger bodies. The $R_{\theta JA}$ and Ψ_{JT} for the Allegro current sensor packages on these boards are shown in Table 4. Note that the LA and LZ packages have lower $R_{\theta JA}$ and Ψ_{JT} than the MA and MC packages because the solder balls more effectively sink heat away from the die to the PCB. The LA and LZ packages have Ψ_{JT} near 0°C/W, or negative, meaning the temperature on the top of the package is the same or lower than the die. For the EZ package $R_{\theta JA}$ is higher than the other packages because of the small package size and superior dissipation into the PCB.

Table 4: Allegro Integrated Packages—Measured Summary

Package	$R_{\theta JA(measured)}$	$\Psi_{JT(measured)}$
MA	20	2.4
MC	19	2.4
LA	19	0.5
LZ	16	–1.7
EZ	55	7.5
LH	33	3.7

Careful consideration of the heat sinking on the PCB is important to minimize the die temperature for average heat dissipation. Maximize the PCB copper trace area and trace thickness for current paths into the IP loop and use in-pad vias to minimize die temperature rise. Additionally, the current-carrying wires and interconnects bringing current onto the PCB are important factors that affect die temperature. The size of the wires or the PCB trace area dedicated to heat sinking can affect the die temperature by 20°C or more.

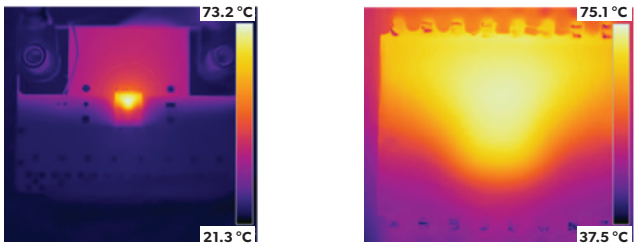

Figure 9: MA package

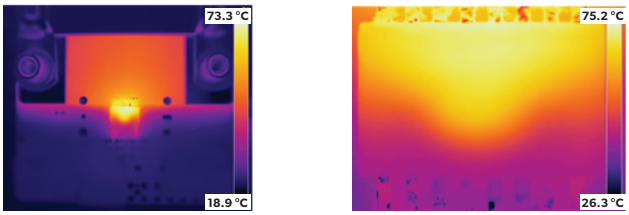

Figure 10: MC package

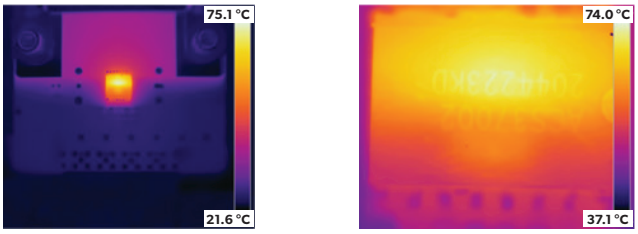

Figure 11: LA package

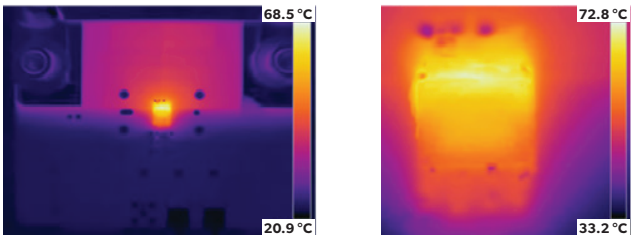

Figure 12: LZ package

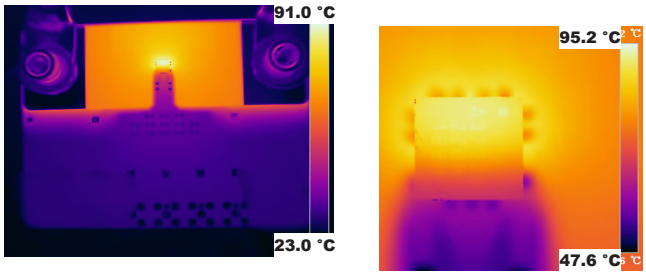

Figure 13: EZ package

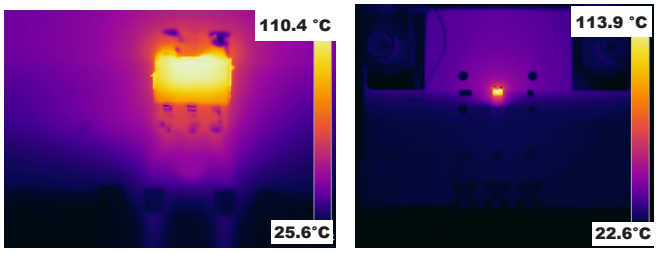

Figure 14: LH package

CONCLUSION

Determining die temperature requires careful consideration of the thermal performance of the package, the PCB, and the rest of the system to keep the die temperature under the maximum specified junction temperature, 165 °C. Use industry standard metrics like $R_{\theta JA}$ with caution because they often apply to a specific set of conditions that may be misleading in any particular application. The results presented here are useful for comparison between the packages and for illustrating the various effects that the package construction has on thermal performance.

Revision History

Number	Date	Description
–	January 31, 2024	Initial release
1	April 16, 2024	Updated packaging options (page 1) and captions of Figure 2 and Figure 3
2	October 9, 2024	Added EZ package (all pages) and LH package (all pages); minor editorial updates (all pages)
3	October 21, 2024	Removed highlights from document

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