AMT49100 START-UP SEQUENCE

By Praveen Kathani, Application Engineer
Allegro MicroSystems

ABSTRACT

This application note is intended to provide user guidelines for the recommended power-up sequence to ensure a robust and reliable start-up when using the Allegro AMT49100 gate driver.

INTRODUCTION

The AMT49100 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for 48 V automotive power applications with high-power inductive loads, such as brushless DC (BLDC) motors.

START-UP SEQUENCE

The sections that follow provide guidance for the start-up sequence for the AMT49100. The start-up sequence depends on whether: 1) an internal buck regulator is used to generate the V_{REG} supply; or 2) an external supply is used to power V_{REG}. The start-up sequences for both cases are discussed next.

Case 1: Buck Regulator Mode

The start-up sequence while using an active internal buck regulator is shown in Figure 1.

Once V_{BB} exceeds 10 V, the RESETn pin can be pulled high to initiate a wake-up sequence. Following the wake-up sequence, the power supplies, including V_{REG} and charge pumps, are active and reach nominal levels within a maximum of 3 ms (t_{INIT}, per datasheet specifications; see Table 1).

The enable pin can then be pulled high. To enable the gate drive function, the system must ensure that any fault flags active at wake-up are acknowledged and cleared appropriately.

Once the enable pin is pulled high, a waiting period of at least 10 µs is recommended before commanding the turn-on of the FETs. This waiting period allows the biases in the gate drive circuitry to become active and stable.

To ensure proper charging of the bootstrap capacitors before turn-on of the high-side FETs, it is recommended that all low-side FETs be turned ON for a short duration adjusted based on the size of the bootstrap capacitors. For example, a duration of 100 µs is suggested for bootstrap capacitors with a capacity of 220 nF.

Once the bootstrap capacitors are adequately charged to approximately V_{REG}, the high-side FETs can be safely activated. Subsequently, the control pins and/or serial peripheral interface (SPI) can be used to control activation or deactivation of the FETs per specific application requirements.

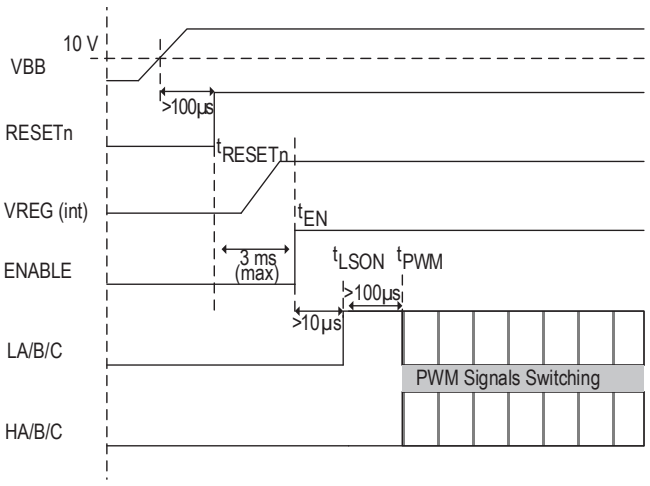

Figure 1: Start-Up Sequence, Buck Regulator Mode (Case 1)

Table 1: Start-Up Time per Datasheet

ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 10 to 80 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Start-Up Time, Buck Regulator Active [1]	t_{INIT}	V_{BB} > 10 V to gate drives enabled, C_{REG} ≤ 10 µF, V_{RESETn} > V_{IH}, V_{BRG} > V_{BRGUV}	–	–	3	ms
Start-Up Time, Buck Regulator Inactive [1]	t_{INIT}	V_{REG} > 10 V to gate drives enabled, V_{RESETn} > V_{IH}, V_{BRG} > V_{BRGUV}	–	–	3	ms

[1] Confirmed by characterization and design. Not production tested.

Case 2: External Regulated Supply Mode

The start-up sequence when the internal buck regulator is inactive and V_{REG} is supplied externally is shown in Figure 2.

Once V_{REG} exceeds 10 V, the RESETn pin must be pulled high. This initiates a wake-up sequence: The internal power supplies and charge pumps become active and reach nominal levels within a maximum of 3 ms (t_{INIT}, per datasheet specifications; see Table 1).

The enable pin can then be pulled high. To enable the gate drive function, the system must ensure that any fault flags active at wake-up are acknowledged and cleared appropriately.

Once the enable pin is pulled high, a waiting period of at least 10 µs is recommended before commanding the turn-on of the FETs. This waiting period allows the biases in the gate drive circuitry to become active and stable.

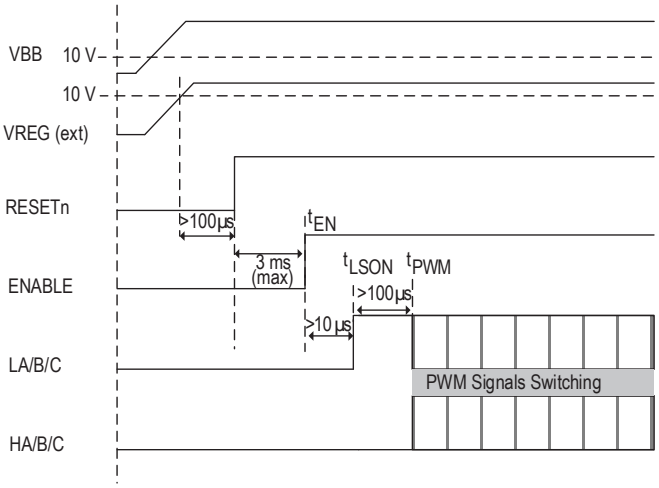

Figure 2: Start-Up Sequence, External Regulated Supply Mode (Case 2)

To ensure proper charging of the bootstrap capacitors before turn-on of the high-side FETs, it is recommended that all low-side FETs be turned ON for a short duration adjusted based on the size of the bootstrap capacitors. For example, a duration of 100 µs is suggested for bootstrap capacitors with a capacity of 220 nF.

Once the bootstrap capacitors are adequately charged to approximately V_{REG}, the high-side FETs can be safely activated. Subsequently, the control pins and/or serial peripheral interface (SPI) can be used to control activation or deactivation of the FETs per specific application requirements.

Notes

In both cases presented here, driving the bridge FETs requires V_{BRG} levels to exceed V_{BRGUV} levels.

Throughout the start-up process and subsequent operation, the SPI remains active, allowing seamless communication and interaction with external devices or systems for precise control and monitoring.

For further detail, refer to the Bootstrap Capacitor Selection and V_{REG} Capacitor Selection sections in the datasheet.

CONCLUSION

In summary, upon pulling the RESETn pin high, before commanding the FETs using PWM control it is essential to allow sufficient time (t_{INIT}) for the part to wake up and the bootstrap capacitors to charge to V_{REG} by turning on all the low-side FETs. The methods presented here allow a robust and reliable start-up when using the AMT49100.

Revision History

Number	Date	Description	Responsibility
–	April 24, 2024	Initial release	Praveen Kathani

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM