PRACTICAL CONSIDERATIONS FOR MOSFET SLEW-RATE CONTROL IN SMART GATE-DRIVER APPLICATIONS

By Asif Jamal, Vashist Bist, Praveen Kathani and Narsimhan Trichy
Allegro MicroSystems

ABSTRACT

This application note examines the critical design considerations of MOSFET slew-rate control in smart gate-driver applications, with a focus on the challenges of 48 V automotive systems. To balance the trade-offs of competing design requirements, effective slew-rate control is essential:

- A high slew rate minimizes switching losses and enhances efficiency, but it can introduce voltage overshoots and oscillations with the potential to damage the gate drive.
- A lower slew rate reduces voltage stress and electromagnetic interference (EMI), but it increases switching losses due to extended transition times.

This application note explores the trade-offs involved in slew-rate selection and provides practical guidelines and design considerations to achieve the desired switching characteristics.

As the industry transitions to higher-voltage platforms, designers of power electronics must manage new complexities in switching transitions. This application note analyzes the impact of peak gate current on slew-rate control.

A distinctive characteristic of next-generation MOSFETs (i.e., MOSFETs used in a 48 V applications) is the comparatively lower gate charge. This application note thoroughly explores the effects of gate-charge levels, along with the significant impact of gate-drain capacitance (C_{GD}) nonlinearity across different operating voltages.

The nonlinearity of C_{GD} can lead to unpredictable switching behavior and an uncontrollably high slew rate, which leads to unwanted gate-driver operations, such as self-turn-on or gate-driver failure. This application note presents comprehensive mitigation techniques, including proper tuning and selection of various smart gate drive-controllable parameters for an Allegro gate-driver unit (GDU), selection strategies for optimized gate-resistance, and approaches to work with the nonlinear behavior of the C_{GD} variation.

Through implementation of the techniques presented in this application note, designers can achieve precise control of switching transitions, minimize EMI generation, reduce switching losses, and enhance overall system reliability in 48 V applications.

INTRODUCTION

For optimized performance and reliability of any power electronic system, control of the switching transitions of the power MOSFETs is crucial. A critical parameter in the management of these transitions is the MOSFET slew rate, defined as the rate of change of the phase-node voltage, $d(V_{SX})/dt$. Whether rapid (high) or slow (low), the slew rate can introduce challenges. Therefore, careful selection of the slew rate is essential to a successful design.

MOSFETs designed for 48 V applications exhibit distinctive capacitance characteristics that significantly impact slew-rate control strategies. Compared to 12 V counterparts, the 48 V MOSFET typically features lower gate-drain capacitance (C_{GD}) values. A lower C_{GD} can help reduce the Miller effect and improve switching speed, but it uniquely presents challenges associated with an increased sensitivity where an unchanged gate current produces a faster voltage transition. This makes the MOSFET more responsive, but also more sensitive to gate-drive variations. Moreover, a lower C_{GD} provides a less-natural damping effect. If not properly controlled, this effect leads to increased ringing and oscillation.

The Allegro smart GDU (such as AMT49100 [1]) can be enabled to easily handle a slew rate of 1 kV/µs on the switching node, which is typically determined by the internal structure of the gate driver, such as the electrostatic-discharge (ESD) clamps and protection. To limit the slew rate in such applications, the smart GDU allows gate-current control.

To meet the growing demands for power applications, the automotive industry is increasingly adopting 48 V electrical systems. While these systems offer advantages like reduced current draw and improved efficiency compared to traditional 12 V systems, this transition creates a new challenge for power electronics design, such as the control of MOSFET slew rates. Higher voltage levels and faster switching speeds in 48 V systems require careful management of gate drive characteristics to prevent voltage overshoots and ringing. The nonlinear behavior of gate-drain capacitance (C_{GD}) in 48 V MOSFETs further complicates slew-rate control. To ensure reliable system operation, smart gate drivers are required.

Typical Gate-Driver System (No Slew Rate Control)

The typical setup to drive a three-phase motor using discrete MOSFETs and a smart gate driver is shown in Figure 1. A single phase of the motor drive with a high-side MOSFET (S_1) and a low-side MOSFET (S_2) is shown. Typically, during operation, S_1 and S_2 are alternately enabled to regulate the current in the motor phase winding. C_{GS}, C_{GD}, and C_{DS} are the intrinsic capacitances, and R_{G_IN} is the internal gate resistance of the MOSFETs. S_X is the switching node, which also acts as a reference node for the high-side gate driver, whereas L_{SS} acts as a reference node for the low-side driver. The bootstrap circuitry in the gate driver is used to maintain the voltage higher than the supply voltage (V_{BRG}) for the high-side gate driver using the bootstrap capacitor (C_{BOOT}).

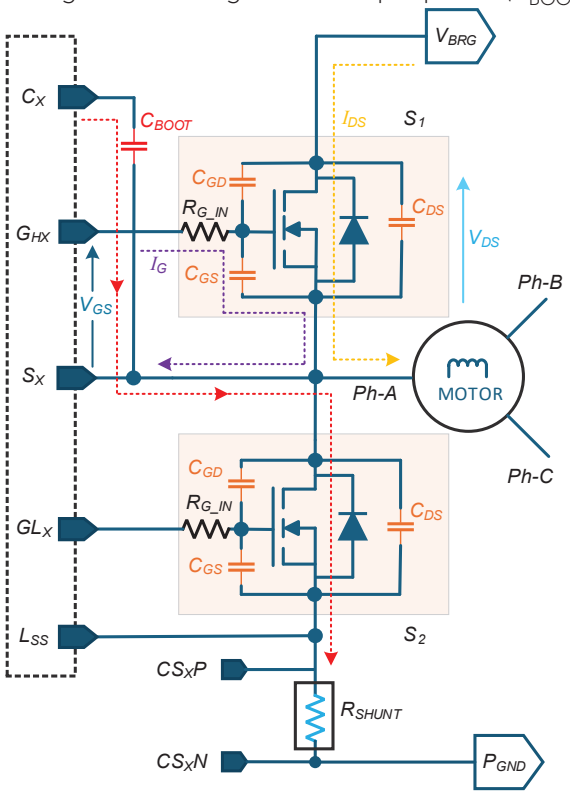

Figure 1: Half-Bridge Power Section of a Three-Phase Motor Driver Showing High-Side and Low-Side MOSFETs

[1] AMT49100/AMT49101 Datasheet, ASIL BLDC MOSFET Gate Drivers for 48 V Battery Systems, Rev. 2, July 2020.

GATE-DRIVER TURN-ON

This section presents the MOSFET turn-on phenomenon, as shown in Figure 2. The overall operation of the MOSFET turn-on has four major timing segments, depicted as zones t_1, t_2, t_3, and t_4, described next.

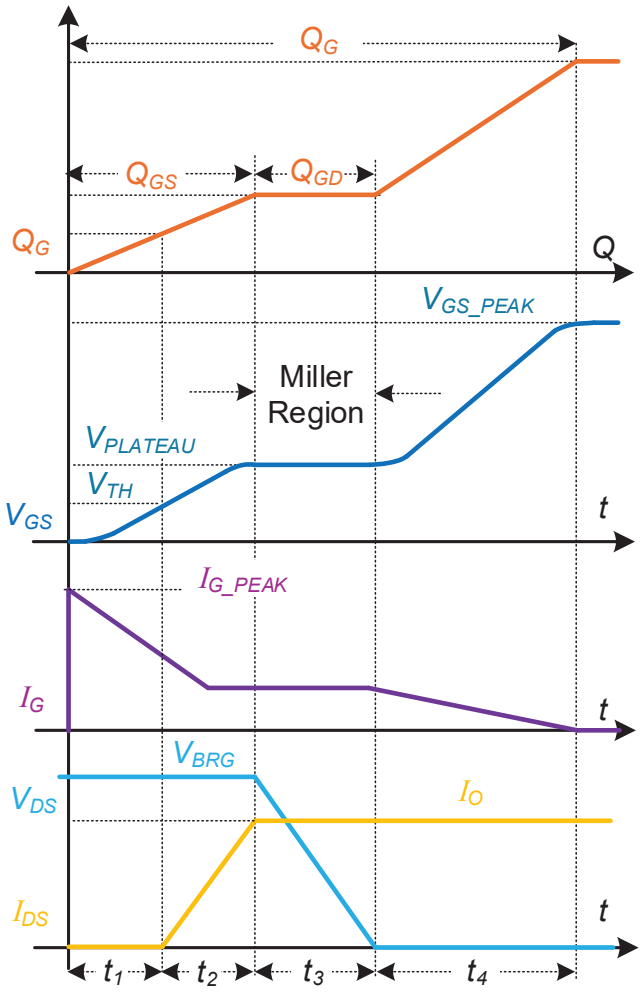

Figure 2: Turn-On Characteristic of MOSFET

Zone t_1

At the beginning of the switching cycle, the MOSFET is off, and V_{GS} is at zero. When a positive voltage is applied to the gate, current begins to flow into the gate, which primarily charges the gate-source capacitance (C_{GS}). As C_{GS} charges, the gate-source voltage (V_{GS}) gradually increases. The rate of V_{GS} increase is determined by the gate-drive current (I_G) and the value of C_{GS}. Because C_{GS} is relatively constant at low V_{GS} values, this initial phase is characterized by a relatively linear increase in V_{GS}.

The t_1 interval ends when V_{GS} reaches the threshold voltage (V_{TH}). This is the critical voltage level at which the MOSFET begins to conduct. At V_{TH}, a channel forms between the drain and source terminals. This channel allows current to flow. However, the MOSFET is not yet fully on at this point.

The peak gate current at the start of t_1 results from the behavior of the capacitor when used as the short circuit. This behavior leads to peak gate current (I_{G_PEAK}) expressed as:

Equation 1:

$$I_{G\_PEAK} = \frac{V_{GS\_PEAK}}{\left(R_{G\_IN} + R_{GDX}\right)}$$

where R_{GDX} is the resistance offered by gate driver.

The gate-source voltage (V_{GS}) is expressed as:

Equation 2:

$$V_{GS} = V_{GS\_PEAK}\left\{1 - e^{\left(-\frac{t}{R_{TOT}\left(C_{GS}+C_{GD}\right)}\right)}\right\}$$

where R_{TOT} is the total resistance in the gate path, expressed as $R_{G\_IN} + R_{GDX}$.

Zone t_2

After completion of zone t_1, V_{GS} further increases and crosses the gate threshold ($V_{GS} > V_{TH}$). Therefore, the MOSFET starts to conduct, and the drain-source current (I_{DS}) starts to flow through the MOSFET.

The change of rate in the current, $d(I_{DSX})/dt$, occurs in this region, and the further increase in V_{GS} helps to widen the channel to allow more current to flow. This period ends when the MOSFET current (I_{DS}) reaches the level of the load current and saturates. The switching-node slew rate ($d(V_{DSX})/dt$) does not change until zone t_2 completes.

Zone t_3

Zone t_3 represents the Miller-plateau region, which is a crucial phase during the turn-on transition. While the drain-source voltage (V_{DS}) decreases, it is characterized by a relatively flat or slow-rising gate-source voltage (V_{GS}), which is the Miller-plateau voltage. The rate of change of V_{DS} voltage (i.e., slew rate, $d(V_{DSX})/dt$) is governed by the gate current and the gate-drain capacitance (C_{GD}) as:

Equation 3:

$$I_G = I_{GD} = C_{GD} \times \frac{d}{dt}(V_{DSX})$$

Therefore, the MOSFET slew rate is a function of the gate current (I_{GD}) and the gate-drain capacitance (C_{GD}) as:

Equation 4:

$$\frac{d}{dt}(V_{DSX}) = \frac{I_{GD}}{C_{GD}}$$

The Miller plateau demonstrates how C_{GD} significantly affects gate-drive requirements and switching speed. This transition zone completes when the V_{DS} voltage reaches its final value, i.e., 0 V.

Zone t_4

Zone t_4 in the MOSFET switching waveform represents the final phase of the turn-on transition. Zone t_4 occurs after the Miller plateau. The gate-source voltage (V_{GS}) continues to rise toward its final value (V_{GS_PEAK}). Because the gate-drain capacitance (C_{GD}) is largely charged, and the gate current now charges the remaining gate-source capacitance, this rise is typically faster than during the Miller plateau. The drain-source voltage (V_{DS}) completes its fall and settles at its final on-state value (V_{DS_ON}) as:

Equation 5:

$$V_{DS(ON)} = I_{DS} \times R_{DS(ON)}$$

where R_{DS_ON} is the on-state resistance of the MOSFET.

GATE DRIVER TURN-OFF

This section presents the MOSFET turn-off phenomenon as shown in Figure 3. The overall operation of the MOSFET turn-off has four major timing segments, depicted as zones t_5, t_6, t_7, and t_8, described next.

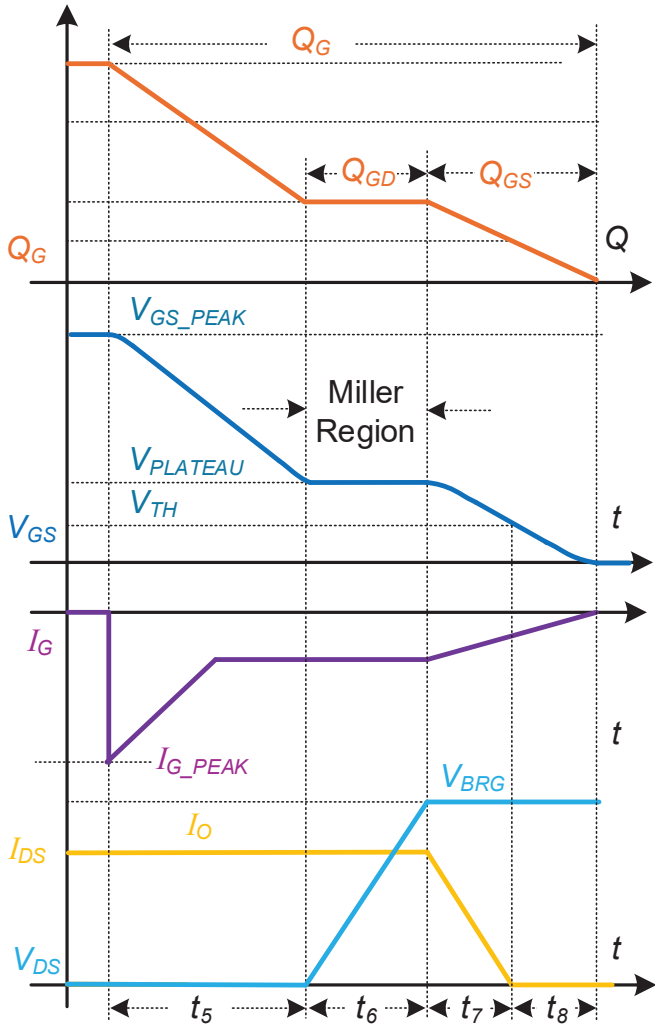

Figure 3: Turn-Off Characteristic of MOSFET

Zone t_5

Zone t_5 marks the beginning of the MOSFET turn-off transition. Zone t_5 is characterized by an initial decrease in gate-source voltage (V_{GS}) from its fully-on value, toward the Miller plateau region, until $V_{GS} = V_{PLATEAU}$. During this period, the gate-source capacitor (C_{GS}) starts to discharge, and the direction of gate current is reversed compared to the turn-on characteristics.

The drain-source voltage (V_{DS}) remains at its low on-state value as determined by Equation 5, and the drain current (I_{DS}) continues to flow at its full value. The MOSFET remains in its fully enhanced state where it operates in the ohmic region.

Zone t_6

Zone t_6 constitutes the Miller region when the gate-source voltage is equal to the plateau voltage, i.e., $V_{GS} = V_{PLATEAU}$. The most significant event during zone t_6 is the rise of the drain-source voltage (V_{DS}). As C_{GD} discharges, V_{DS} increases from its low on-state value, toward the supply voltage (V_{BRG}). The rate of this rise ($d(V_{DSX})/dt$) is directly related to the gate current and C_{GD}. The drain current (I_{DS}) remains relatively constant at its full value. The MOSFET continues to conduct, but it transitions from the linear region to the saturation region.

Zone t_7

Zone t_7 is characterized by the rapid decrease in drain-source current (I_{DS}) while the gate-source voltage (V_{GS}) continues to reduce to less than the Miller-plateau voltage. This phase represents the final stage of active switching of the MOSFET before it fully turns off. The most significant event during zone t_7 is the rapid decrease in drain current (I_{DS}). As V_{GS} reduces to less than $V_{PLATEAU}$, the MOSFET transitions from the saturation region toward cutoff, and the channel conductivity decreases rapidly. This causes I_{DS} to reduce from its full value toward zero. Therefore, this region also contributes to $d(I_{DSX})/dt$.

Zone t_8

Zone t_8 is characterized by a fully-turned-off MOSFET and the cessation of all dynamic switching activity. The device is in cutoff mode, where it effectively behaves like an open circuit between the drain and the source terminals. The V_{GS} has reached its low off-state value, typically zero or a negative voltage if a negative gate drive is used. The V_{DS} is at its maximum off-state value, equal to the supply voltage (V_{BRG}). Because the current does not flow, the voltage does not drop across the MOSFET.

SMART GATE DRIVER

In a current-control gate driver (smart gate driver) such as the AMT49100, the gate-drive current (I_{G_DRV}) is actively controlled (as opposed to being controlled through simple application of a voltage). This allows precise control of the switching behavior of the MOSFET, particularly during the Miller-plateau region. This control is crucial to the minimization of switching losses and EMI.

To control the slew rate, the gate driver provides two pulses of current. These pulses can be adjusted through the serial port interface (SPI) for their respective durations, as per application need. The gate drive provides I_{G1} and I_{G2}, where I_{G1} controls dI/dt, and I_{G2} controls dV/dt, as shown in Figure 4. This figure depicts the MOSFET turn-on with the smart gate driver, showing I_{G1} and I_{G2} control.

In smart gate drivers, the values of I_{G1}, I_{G2}, and time for which I_{G1} is applicable are user-selectable. The selections of I_{G1} and I_{G2} are very important because the charging of gate capacitors C_{GS} and C_{GD} can be aligned at currents I_{G1} and I_{G2}, respectively, for decoupled control of the slew rate.

Similarly, MOSFET turn-off control is accomplished through adjustments to the gate-driver current, I_{G1} and I_{G2}. During MOSFET turn-off, I_{G2} (sink current) is facilitated by the gate drive to discharge the capacitor C_{GS} and C_{GD}. The Miller charge, Q_{GD}, discharges at a rate that depends on the I_{G2} current, as shown in Figure 5.

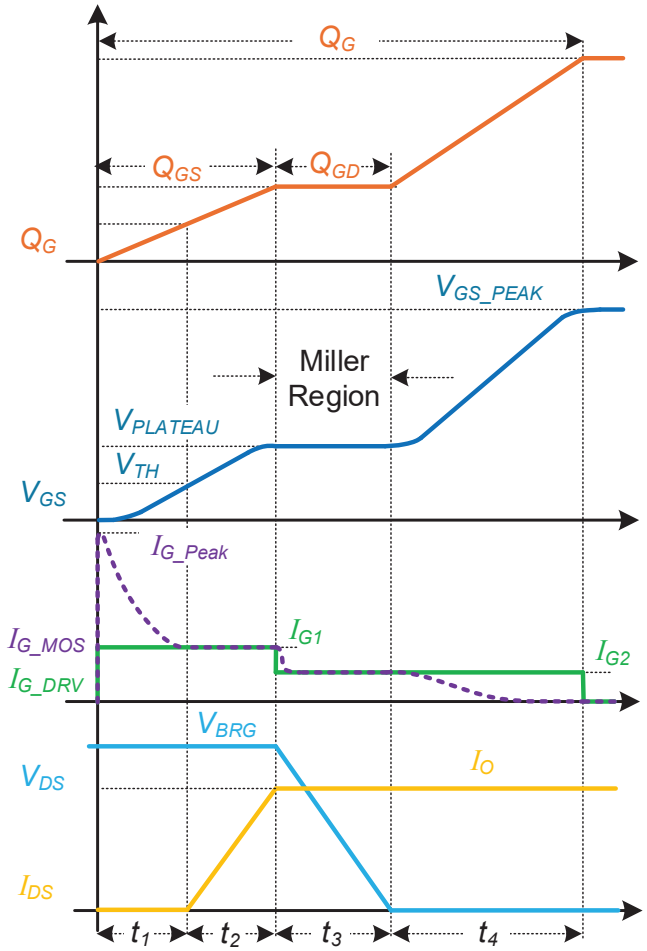

Figure 4: Turn-On Characteristic of MOSFET using a Smart Gate Driver

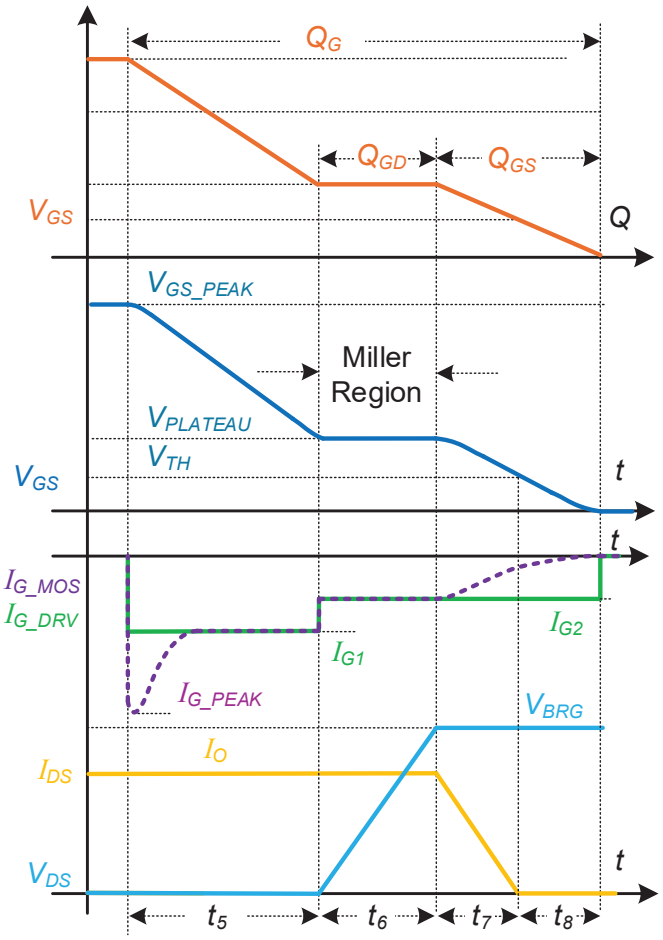

Figure 5: Turn-Off Characteristic of MOSFET using a Smart Gate Driver

IMPACT OF GATE DRIVER PEAK CURRENT

This section discusses the adverse impact of the peak gate current (I_{G_PEAK}) due to gate-driver limitation and its effect on the overall switching characteristics, as shown in Figure 6.

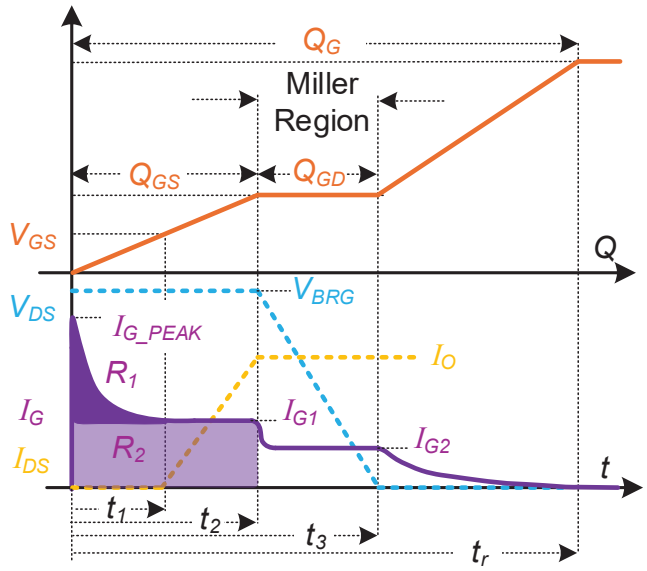

Figure 6: Gate Charge and Gate Current

Typically, the total charge demanded by the MOSFET for MOSFET turn-on is supplied by the gate driver. The total charge required is:

Equation 6:

$$Q_G = \int_0^{t_r} (I_G)\, dt$$

where Q_{GS} is the charge required to reach the Miller plateau, and Q_{GD} is the charge required to complete the transition.

Therefore, the charge required to reach the Miller plateau equals the charge that the gate driver needs to inject as the Q_{GS}, expressed as:

Equation 7:

$$Q_{GS} = \int_0^{t_1} (I_G)\, dt + \int_{t_1}^{t_2} (I_G)\, dt$$

In this equation, the first term contributes to the charge required to reach the threshold voltage, and the second term corresponds to the rate of change of current, $d(I_{DSX})/dt$.

For the Miller region, the charge required, Q_{GD}, is similarly given as:

Equation 8:

$$Q_{GD} = \int_{t_2}^{t_3} (I_G)\, dt$$

This equation contributes to the charge requirement for the switching-node slew-rate control ($d(V_{DSX})/dt$). Therefore, to reach the plateau, the gate driver must provide the charge Q_{GS}, as well as control of $d(I_{DSX})/dt$. This must be followed by the charge Q_{GD} in the Miller region to control the slew rate ($d(V_{DSX})/dt$) of the switching node.

In a smart gate driver, I_{G1} controls Q_{GS}, and I_{G2} controls Q_{GD}. However, due to the additional peak current (I_{G_PEAK}), the overall delivery of charge ($R_1 + R_2$) from the gate driver is higher. This can have an impact on the overall switching characteristics, as explained below. This additional charge due to peak gate current should be optimized by the configurable gate current and timings.

In the ideal gate-control scenario, the charge delivered by the gate driver equals the charge demanded by the MOSFET; however, as explained previously, there are two other possible scenarios: 1) $Q_{GS\_DRV} > Q_{GS\_MOS}$; and 2) $Q_{GS\_DRV} < Q_{GS\_MOS}$, described next.

Scenario 1: $Q_{GS\_DRV} > Q_{GS\_MOS}$

If the supplied charge (Q_{GS_DRV}) from the gate driver exceeds the demand charge (Q_{GS_MOS}), the overall switching rate increases, as shown in Figure 7. In this scenario, the gate-driver current applied ($I_{G1'}$) exceeds the ideal gate-driver current (I_{G1}). As shown in Figure 7, because $I_{G1'} > I_{G1}$, $d(I_{DSX})/dt$ and $d(V_{DSX})/dt$ are effectively increased. Moreover, because the $d(V_{DSX})/dt$ is now controlled by two different gate currents, i.e., $I_{G1'}$ and I_{G2}, a dual slope of $d(V_{DSX})/dt$ is observed.

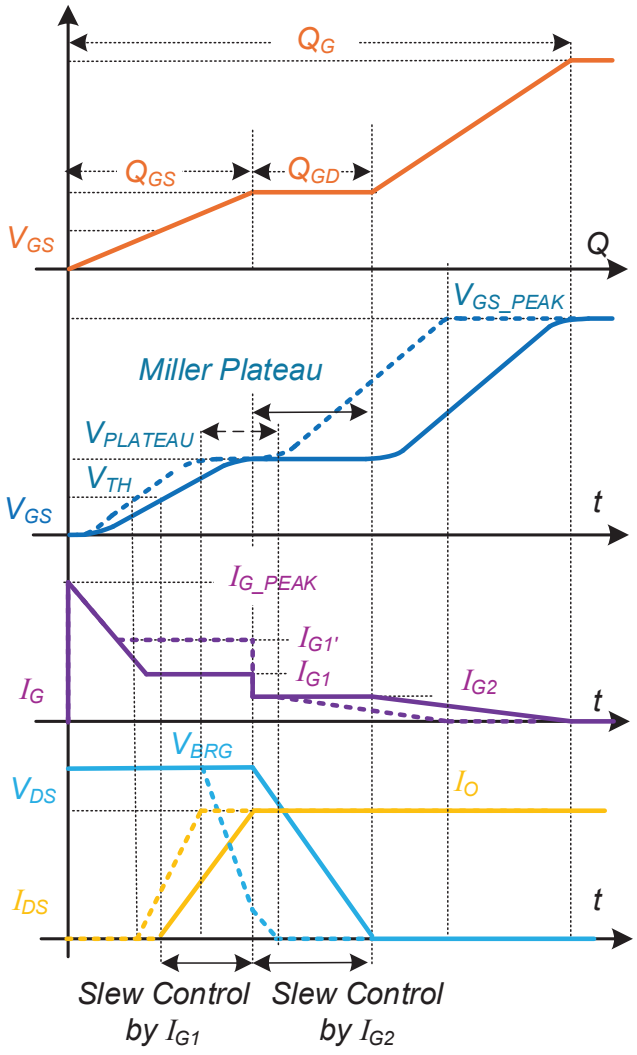

Figure 7: Impact of $Q_{GS\_DRV} > Q_{GS\_MOS}$

Scenario 2: $Q_{GS\_DRV} < Q_{GS\_MOS}$

If the supplied charge (Q_{GS_DRV}) from the gate driver is less than the demand charge (Q_{GS_MOS}), the overall switching rate decreases, as shown in Figure 8. In this scenario, a gate-driver current ($I_{G1'}$) less than the ideal gate-driver current (I_{G1}) is applied. As shown in Figure 8, $I_{G1'}$ is less than I_{G1}, so $d(I_{DSX})/dt$ increases, but $d(V_{DSX})/dt$ remains the same as in the ideal case because it is still charged by I_{G2}. However, because $d(I_{DSX})/dt$ is controlled by two gate currents, $I_{G1'}$ and I_{G2}, a dual slope of $d(I_{DSX})/dt$ is observed in Figure 8.

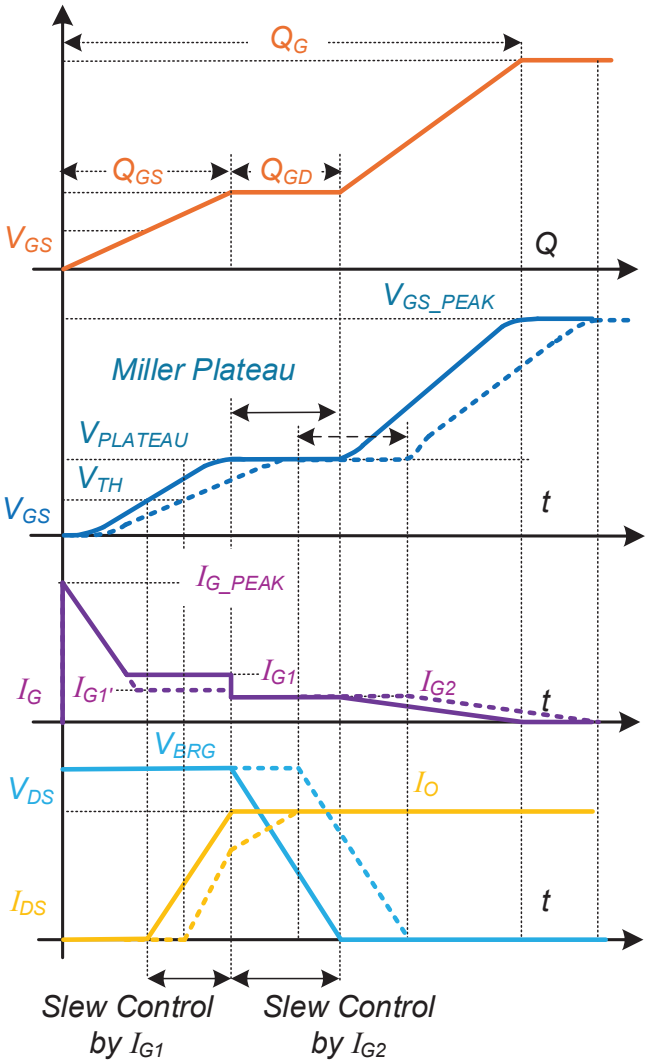

Figure 8: Impact of $Q_{GS\_DRV} < Q_{GS\_MOS}$

The experimental results of a tuned smart gate driver (using AMT49100) are shown in Figure 9, where the smart GDU provides sufficient Q_{GS} charge [driven by ILR1 (I_{G1}) and TLR1] for the MOSFET; i.e., $Q_{GS\_DRV} = Q_{GS\_MOS}$ and the slew rate is only controlled by ILR2 current (I_{G2}).

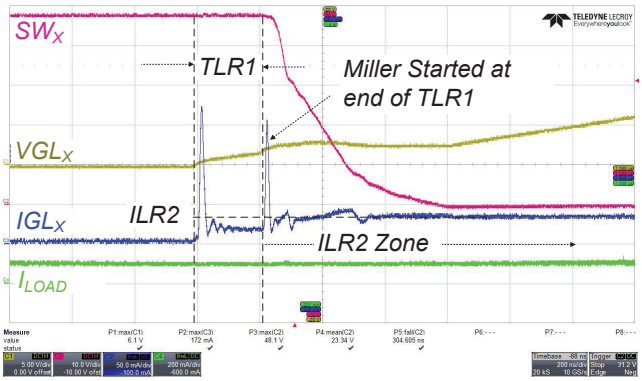

Figure 9: Experimental Waveforms Showing $Q_{GS\_DRV} = Q_{GS\_MOS}$

The experimental results of a case where the smart GDU overdrives the Q_{GS} charge, i.e., $Q_{GS\_DRV} > Q_{GS\_MOS}$, and effectively controls the Miller region with ILR1 current is shown in Figure 10. In this case, ILR1 and TLR are set to exceed the required Q_{GS}, and the driver is allowed to overdrive, such that the driver controls the slew rate with ILR1 instead of ILR2.

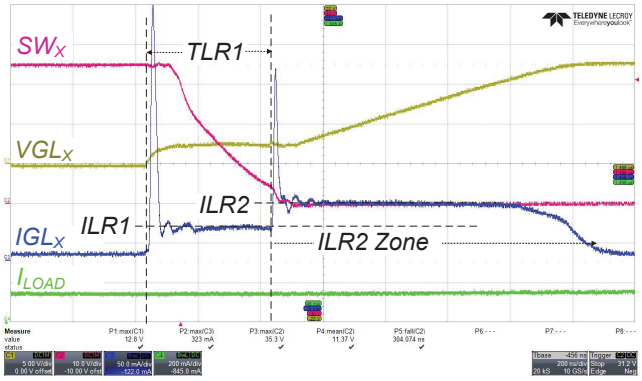

Figure 10: Experimental Waveforms Showing $Q_{GS\_DRV} > Q_{GS\_MOS}$

The experimental results of a smart GDU (AMT49100) where the charge provided by the driver (Q_{GS_DRV}) is less than the demand charge (Q_{GS_MOS}), i.e., $Q_{GS\_DRV} < Q_{GS\_MOS}$, is shown in Figure 11. As can be observed, the TLR1 time completes before the Miller region arrives, and ILR2 provides the rest of the Q_{GS} charge.

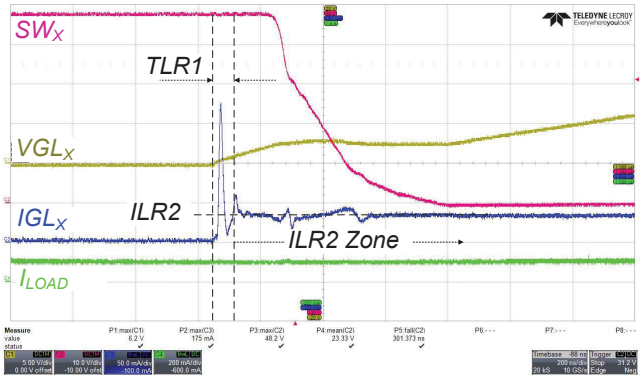

Figure 11: Experimental Waveforms Showing $Q_{GS\_DRV} < Q_{GS\_MOS}$

NONLINEAR C_{GD} VARIATION

The nonlinear variation of gate-drain capacitance (C_{GD}) presents significant challenges in MOSFET gate-drive design. C_{GD} is not a constant value; it varies significantly with the drain-source voltage (V_{DS}). This nonlinear relationship is inherent to the physical MOSFET structure and becomes more pronounced in modern, high-voltage devices optimized for low on-state drain-source resistance (R_{DS_ON}).

During switching transitions, the effective input capacitance witnessed by the gate driver is amplified by the Miller effect. This amplified capacitance (C_{Miller}) is proportional to C_{GD} and MOSFET gain. Because C_{GD} varies with V_{DS}, C_{Miller} also becomes dynamic and changes throughout the switching event. These changes make it difficult to predict and control the gate-drive current required for optimal switching.

An example of the gate-drain capacitance ($C_{rss} = C_{GD}$) of a 100 V, 2.8 mΩ, 180 A, N-channel MOSFET [2] is shown in Figure 12. As shown, when V_{DS} is 0 V, C_{GD} is 1100 pF; and, when V_{DS} is ~48 V, C_{GD} reduces to 18 pF. This ratio is almost 61×, and it increases further for higher V_{DS} voltages.

The varying C_{GD} makes it difficult to achieve a consistent slew rate ($d(V_{DSX})/dt$). As C_{GD} changes, the gate-current (I_G) required to maintain a specific slew rate also changes: At lower V_{DS} voltages, this can lead to a switching transition that is slower than desired; at higher V_{DS} voltages this can lead to a switching transition that is faster than desired.

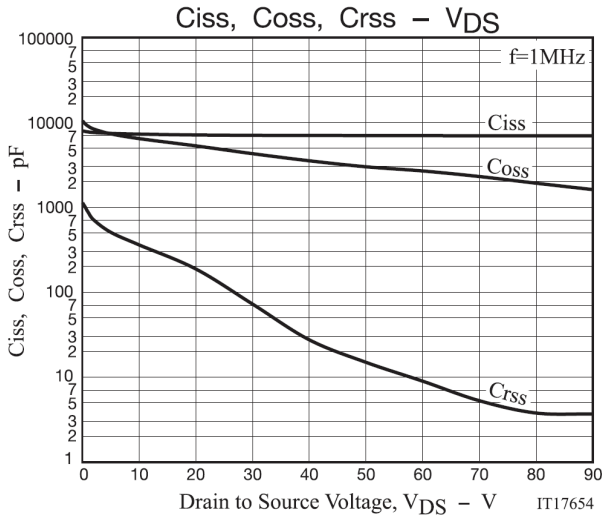

Figure 12: Variation of C_{iss}, C_{oss}, and C_{rss} with V_{DS} for an NDBA180N10B MOSFET [2]

IMPACT OF NONLINEAR C_{GD} VARIATION ON TURN-ON CHARACTERISTICS

The turn-on characteristics of the MOSFET with the nonlinear variation of C_{GD} is shown in Figure 13. During MOSFET turn-on, the initial V_{DS} is held at the supply voltage, i.e., V_{BRG}. Therefore, the value of C_{GD} is much lower (~18 pF). However, once V_{DS} begins to decrease, C_{GD} beings to increase nonlinearly, as shown in Figure 13. Due to this variation, the falling slope of V_{DS} is much steeper at the start of the voltage plateau and flattens at the end of the voltage plateau. The expected and measured slew rates are highlighted in Figure 13. This lower C_{GD} can lead to a higher slew rate (>1 kV/µs) at the start of plateau region, which can potentially cause a malfunction in the gate-driver operation.

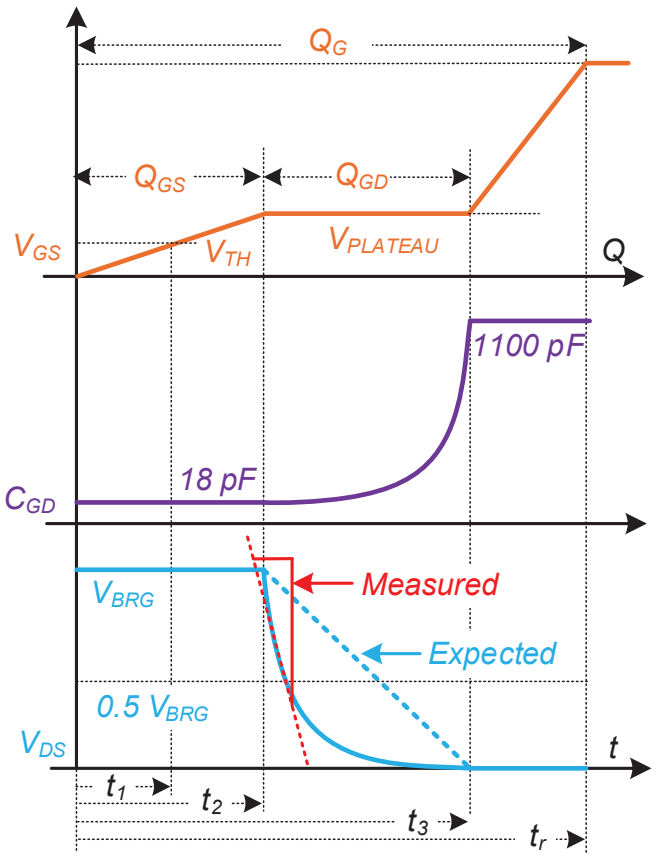

Figure 13: Impact of Nonlinear C_{GD} on Turn-On Slew Rate

[2] NDBA180N10B, 100 V, 2.8 mΩ, 180 A, N-channel MOSFET, On Semiconductor, Rev. 4, Jan 2016.

IMPACT OF NONLINEAR C_{GD} VARIATION ON TURN-OFF CHARACTERISTICS

Behavior similar to turn-on is observed during MOSFET turn-off. Due to the nonlinear behavior of C_{GD}, the turn-off slew rate changes as shown in Figure 14. During MOSFET turn-off, the initial V_{DS} is held close to V_{DS_ON} (very close to 0 V, due to lower R_{DS_ON}). Therefore, the value of C_{GD} is much higher (~1100 pF). However, once V_{DS} starts to increase, C_{GD} starts to decrease nonlinearly. Due to this variation, the rising slope of V_{DS} is much flatter at the start of the voltage plateau and steeper at the end of the voltage plateau. The expected and measured slew rates are highlighted in Figure 14. This shows a lower slew rate at the start of the plateau region and a very high slew rate at the end of the plateau region. This high slew rate can exceed the 1 kV/µs limit and trigger a malfunction in the gate-driver operation.

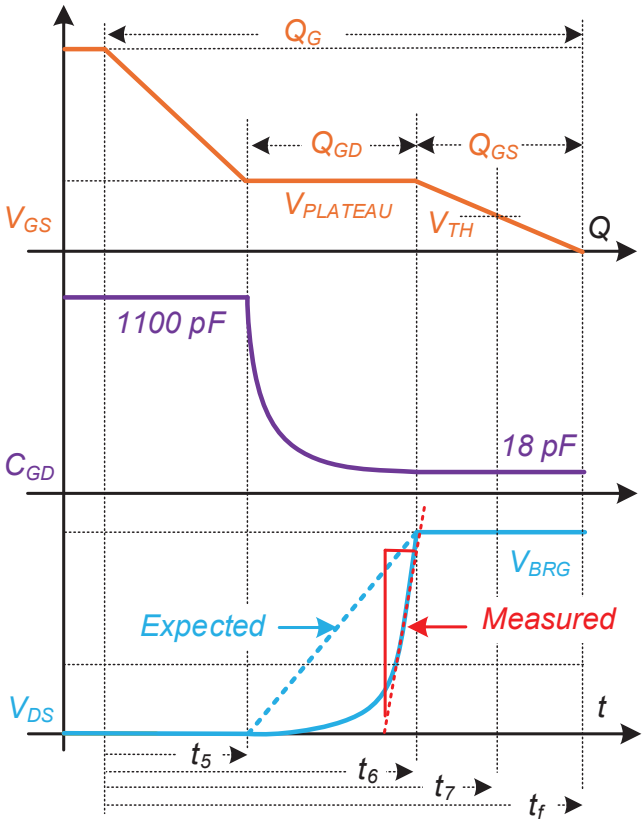

Figure 14: Impact of Nonlinear C_{GD} on Turn-Off Slew Rate

COMPENSATION OF NONLINEAR C_{GD} VARIATION

To effectively add capacitance in parallel with the intrinsic C_{GD} of the device, external gate-drain capacitance (C_{GD_EXT}) can be added between the gate and drain of a MOSFET, as shown in Figure 15. During switching transitions, this external capacitance increases the total gate charge (Q_G) that the gate driver must supply or remove. This, in turn, slows the rate of change of $d(V_{DSX})/dt$, which limits the slew rate.

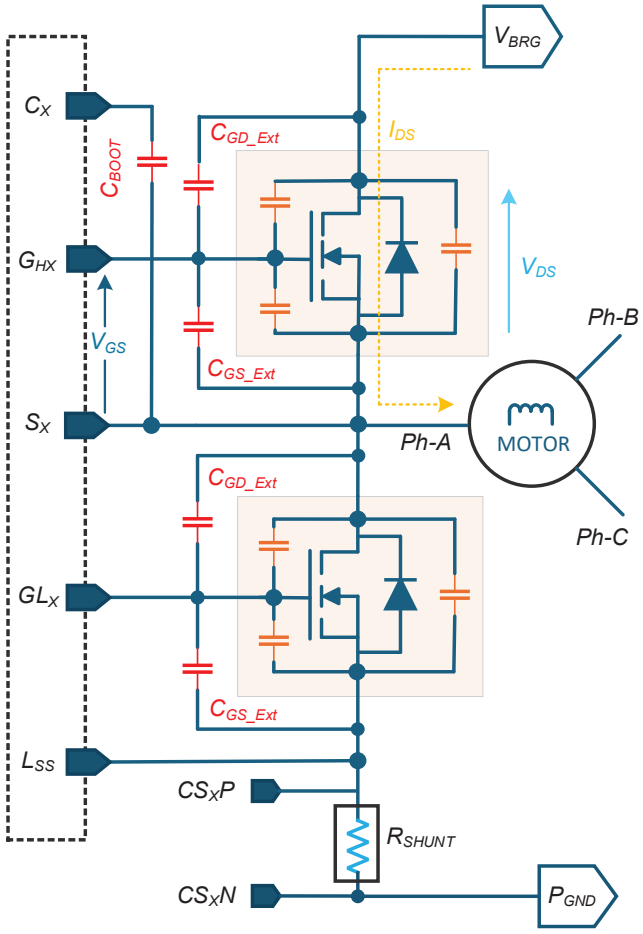

Figure 15: External C_{GS} and C_{GD} for Compensating Nonlinearity in MOSFET C_{GD}

During MOSFET turn-on and turn-off, the external capacitor (C_{GD_EXT}) dominates because its value exceeds C_{GD} at higher V_{DS}. Therefore, the effective capacitance is:

Equation 9:

$$C_{GD\_EFF} = C_{GD} + C_{GD\_EXT}$$

Considering the 100 V, 2.8 mΩ, 180 A, N-channel MOSFET [2] and a 220 pF/100 V SMD capacitor, [3] the effective gate-drain capacitance (C_{GD_EFF}) range increases from 18 pF/1100 pF (minimum/maximum) to 238 pF/1320 pF.

The impact to the turn-on and turn-off slew rate of the MOSFET with this additional C_{GD_EXT} capacitor is shown in Figure 16 and Figure 17. As shown, with this external capacitance, the slew rate can be limited to the desired value. However, the addition of external capacitors increases the Miller current, I_{GD}. The increased I_{GD} current leads to internal gate resistance (R_{G_INT}) that causes a voltage drop at the gate node of the MOSFET. The voltage on the gate of the low-side MOSFET observed during the switching node transition V_{GS_SLEW}, is:

Equation 10:

$$V_{GS\_SLEW} = C_{GD} \times \frac{d}{dt}(V_{DSX}) \times R_{G\_INT}$$

$$= I_{GD} \times R_{G\_INT}$$

To limit any shoot-through event, the V_{GS_SLEW} voltage must be maintained at less than the threshold voltage (V_{TH}) of the MOSFET. Therefore, an additional gate-source capacitor (C_{GS_EXT}) can be added to limit the impact of V_{GS_SLEW}. This additional C_{GS_EXT} capacitance should be added such that it does not affect the overall gate capacitance ratio:

Equation 11:

$$\frac{C_{GD}}{(C_{GS} + C_{GD})} = \frac{C_{GD\_EFF}}{(C_{GS\_EFF} + C_{GD\_EFF})}$$

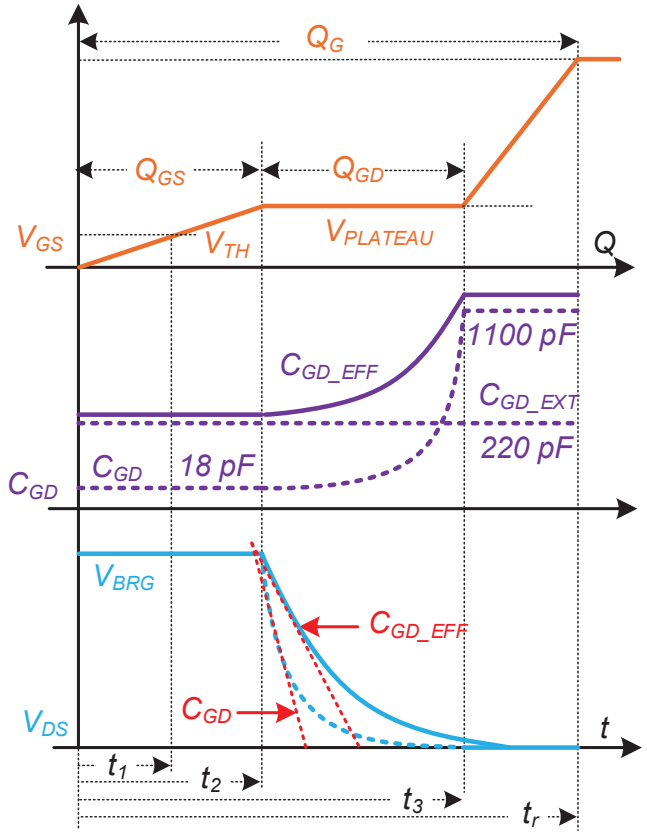

Figure 16: Impact on Turn-On Slew Rate with External C_{GD_EXT} Capacitor

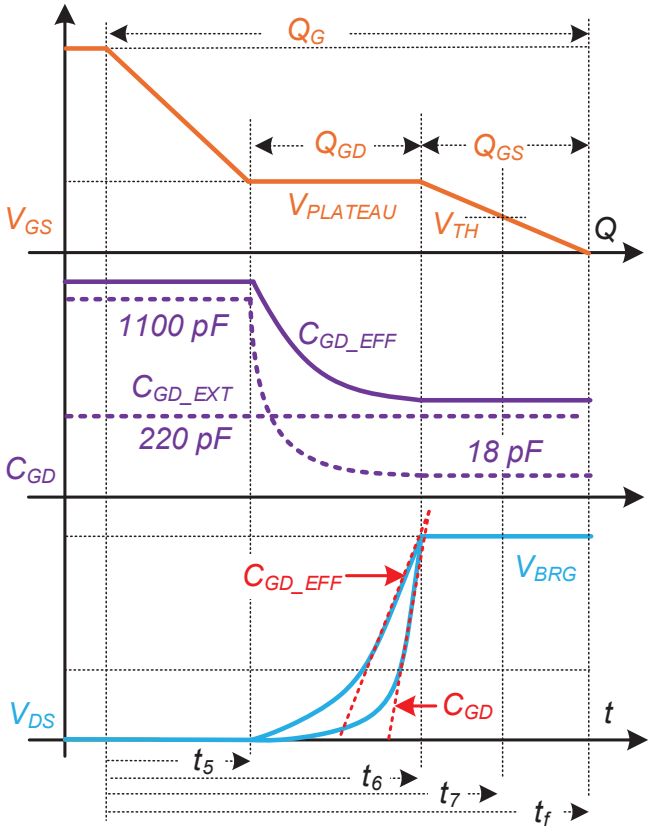

Figure 17: Impact on Turn-Off Slew Rate with External C_{GD_EXT} Capacitor

[3] 220 pF, 100 V, SMD Capacitor, VJ HIFREQ High Temperature (HT) Series, Vishay, April 2024.

The experimental data from the Allegro smart gate-driver AMT49100 is shown in Figure 18 and Figure 19 without and with external components, respectively.

As shown in Figure 18, C_{GD} nonlinearity with respect to V_{DS} clearly impacts the slew rate of the switching node. Without any external component, the initial slew rate is 0.45 kV/µs; and, once V_{DS} reduces to less than 18 V, the slew rate slows to 0.175 kV/µs.

To minimize C_{GD} nonlinearity and to reduce the initial slew rate, two external capacitors can be added: an external capacitor of 33 pF (C_{GD_EXT}) across the gate-to-drain terminal and an external capacitor of 47 pF (C_{GS_EXT}) across the gate-to-source terminal. These additional external components change the initial slew rate from 0.45 kV/µs to 0.3 kV/µs, nearly a 33% impact, as shown in Figure 19.

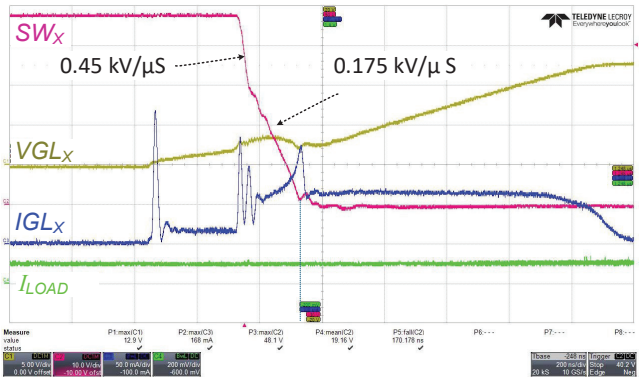

Figure 18: Slew Rate without External C_{GD} and C_{GS}

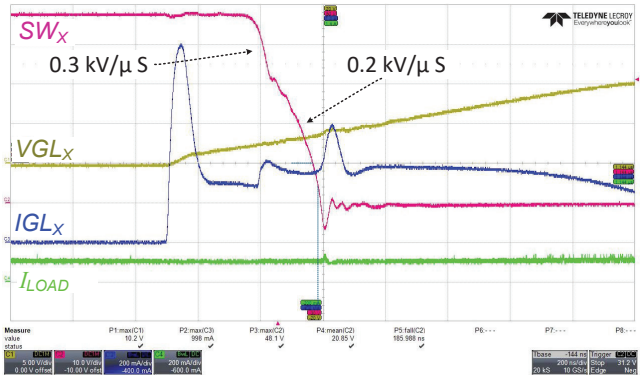

Figure 19: Slew Rate with External C_{GD} = 33 pF and C_{GS} = 47 nF

CROSS-CONDUCTION DUE TO INSUFFICIENT DEAD TIME

Dead time is the short interval intentionally inserted between the turn-off of one MOSFET and the turn-on of the complementary MOSFET in a half-bridge or full-bridge configuration. The purpose of dead time is to prevent simultaneous conduction of the MOSFETs, which would otherwise create a short circuit across the DC bus.

If the dead time in a MOSFET switching circuit is less than the discharge time of the gate-source capacitance (C_{GS}), shoot-through or cross-conduction can occur. This serious issue can damage the MOSFETs and reduce the efficiency of the circuit.

The C_{GS} discharge time is the time it takes for the gate-source voltage (V_{GS}) to reduce to less than the threshold voltage (V_{TH}) during MOSFET turn-off. This discharge is controlled by the gate-driver circuit and is influenced by the gate resistor (R_{G_EXT}), external gate capacitance (C_{GS_EXT}), and gate-driver sink-current capability.

When the dead time is equal to (t_{DEAD}) or greater than (t_{DEADH}) the C_{GS} discharge time, the high-side MOSFET completely discharges and the V_{GS} voltage reduces to less than V_{TH} before the low-side MOSFET turn-on. This safe zone of MOSFET operation protects the MOSFET from shoot-through, as shown in Figure 20.

If the dead-time is less than the time required to fully discharge C_{GS}, the gate driver initiates a high-side MOSFET turn-off, and the high-side V_{GS} begins to fall. Before the high-side MOSFET V_{GS} reduces to less than V_{TH}, the dead time (t_{DEADL}) ends and the gate driver begins to turn on the low-side MOSFET. Because the high-side MOSFET is not yet fully turned-off, but turn-on of the low-side MOSFET is in progress, both MOSFETs conduct simultaneously. This creates a low-impedance path between the V_{BRG} and P_{GND} bus rails, which results in a large current spike (shoot-through current).

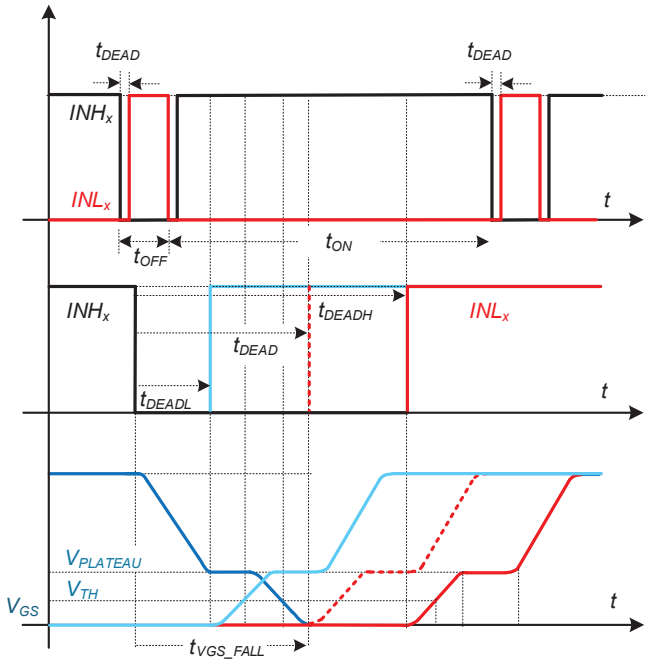

Figure 20: Cross-Conduction at Varying Dead Time

TUNING OF SMART GATE DRIVER

The Allegro smart gate driver (AMT49100) can be easily tuned to control the slew rate of the switching node to meet application requirements. The smart GDU ensures that MOSFET operation does not exceed the maximum slew rate and protects the device from permanent damage. The smart GDU can be easily tuned via the SPI register, where the gate current and time are configured based on the external MOSFET gate-charge requirements. This section details how to use the AMT49100 waveforms to tune an example MOSFET: a 100 V, 130 A, N-Channel MOSFET. [4]

Initially, the ILR1 current and the TLR1 time are set to the lowest setting, and the ILR2 current is set to exceed ILR1, such that the occurrence of current can be observed with respect to the slew rate. The transition of the ILR2 current occurs a significant duration before the SWX node starts to fall. As a result, the ILR1 current is not enough to charge the C_{GS}, as shown in Figure 21, where TLR1 time is set to 60 nS, ILR1 current is set to 16 mA, ILR2 current is set to 32 mA, and the observed slew rate is 0.128 kV/µs.

Next, the Q_{GS} demanded by the MOSFET requires an increase in either the ILR1 current or the TLR1 time. In this exercise, the TLR1 time is increased to allow clear observation of the current and the Miller plateau. However, to achieve the desired Q_{GS}, the user has the flexibility to change ILR1, TLR1, or both. To reach the Miller plateau at the end of TLR1, in this example, the TLR1 time is increased from 60 ns to 284 ns (and ILR1 remains at 16 mA), as shown in Figure 22. As evident in the figure, as soon as the Miller plateau is reached, the gate drivers transition the current from ILR1 to ILR2. Upon this transition, the smart gate driver can effectively control the slew rate with ILR2. Because gate-driver current does not change during the Miller region, the observed slew rate remains at 0.128 kV/µs.

At this point, the driver has been tuned at the optimal setting for Q_{GS} charging and the ILR2 can be controlled to adjust the slew rate. Operation at ILR1 = 16 mA and TLR1 = 284 ns is shown in Figure 23 through Figure 27 for ILR2 configurations of 48 mA, 64 mA, 96 mA, 128 mA, and 240 mA, respectively. As shown in these figures, the slew rate increases as the ILR2 is increased.

The variation of slew rate (kV/µs) with ILR2 current is summarized in Table 1 and plotted in Figure 28. As shown, once the driver is tuned for the initial Q_{GS}, the slew rate is easily controlled via ILR2.

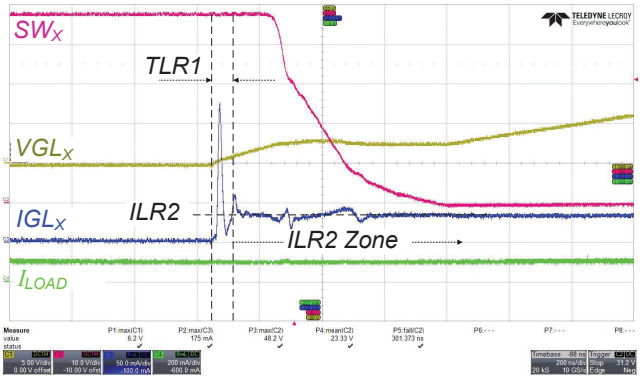

Figure 21: Tuning of AMT49100 for Slew-Rate Control ($Q_{GS\_DRV} < Q_{GS\_MOS}$)

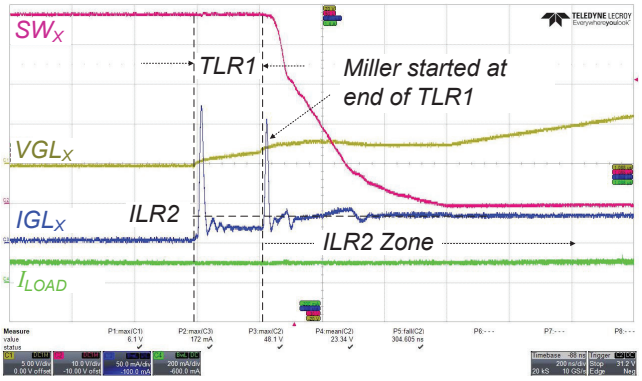

Figure 22: Tuning of AMT49100 for Slew-Rate Control ($Q_{GS\_DRV} = Q_{GS\_MOS}$)

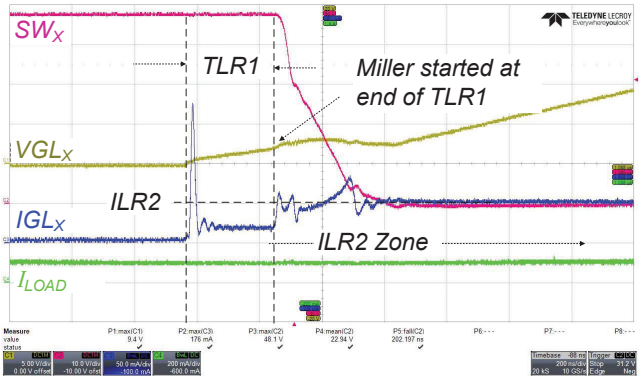

Figure 23: Tuning of AMT49100 for Slew-Rate Control (ILR2 set as 48 mA)

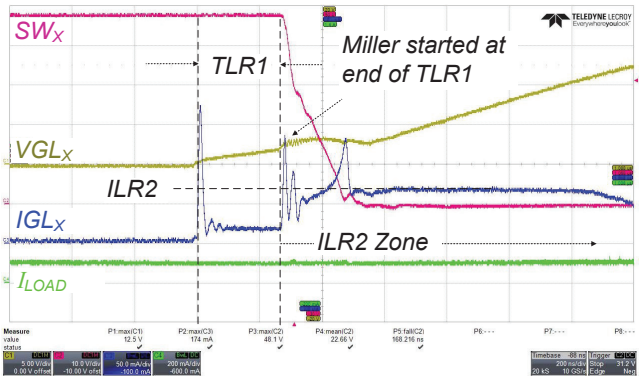

Figure 24: Tuning of AMT49100 for Slew-Rate Control (ILR2 set as 64 mA)

[4] MCB130N10Y, 100 V, 130 A, N-Channel MOSFET, MCC, Rev. 3.5, 2022.

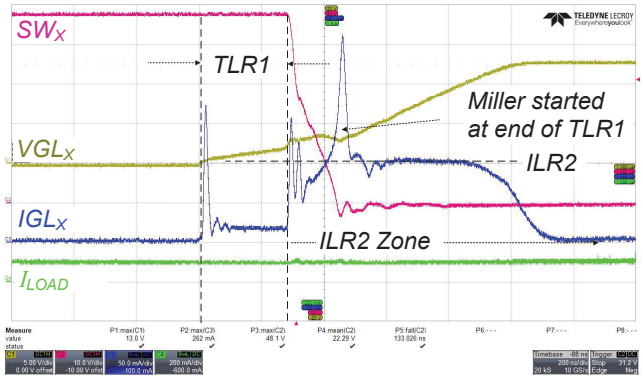

Figure 25: Tuning of AMT49100 for Slew-Rate Control (ILR2 set as 96 mA)

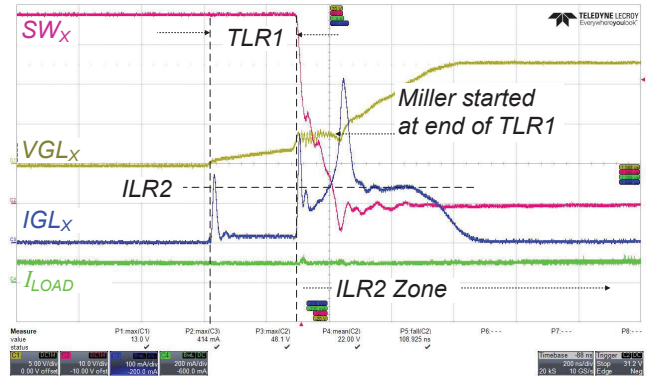

Figure 26: Tuning of AMT49100 for Slew-Rate Control (ILR2 set as 128 mA)

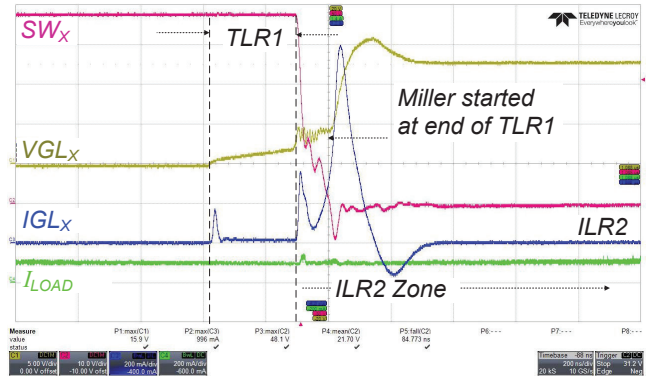

Figure 27: Tuning of AMT49100 for Slew-Rate Control (ILR2 set as 240 mA)

Table 1: AMT49100 Setting for Slew-Rate Control

TLR1 (ns)	ILR1 (mA)	ILR2 (mA)	Slew Time (ns)	Slew Rate (kV/µs)
284	16	32	300	0.128
284	16	48	202	0.191
284	16	64	168	0.228
284	16	96	133	0.288
284	16	128	108	0.356
284	16	240	84.7	0.453

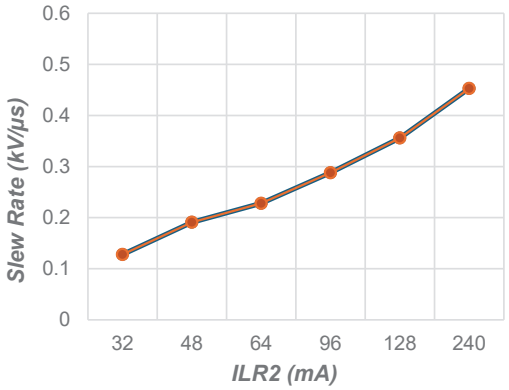

Figure 28: Variation of Slew Rate with ILR2

CONCLUSION

This application note has explored the critical role of smart gate drivers in the optimization of MOSFET slew-rate control for 48 V applications. By providing gate-current control, smart gate drivers enable designers to minimize switching losses, mitigate EMI, and ensure robust system reliability.

Effective slew-rate control is achieved through careful selection of gate-drive parameters, such as gate current and timing. The C_{GD} nonlinearity, and its dependence on drain-source voltage (V_{DS}), significantly impacts the overall switching behavior, leading to slew-rate variations across different operating conditions. This effect is successfully mitigated with the addition of external gate capacitors, as described and verified in this application note.

Use of effective gate-current control in a smart GDU can help a designer achieve optimal MOSFET switching performance, leading to more-efficient, reliable, and robust power electronic systems.

Revision History

Number	Date	Description	Responsibility
–	April 22, 2025	Initial release	V. Bist

955 PERIMETER ROAD • MANCHESTER, NH 03103 • USA
+1-603-626-2300 • FAX: +1-603-641-5336 • ALLEGROMICRO.COM