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DOUBLER CHARGE-PUMP SCHEME FOR GATE DRIVERS IN AUTOMOTIVE APPLICATIONS

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ABSTRACT

Most Allegro gate drivers are powered by a programmable-voltage internal regulator that limits the supply to the drivers and therefore limits the maximum gate-to-source voltage. In an automotive application, such as electric power steering, during low-supply-voltage events, such as cold-crank and warm-crank conditions, the regulated supply is maintained by a unique charge-pump boost converter that functions as a voltage doubler that requires a pump capacitor and a storage capacitor. This application note discusses the main advantages of the charge pump employed in the Allegro A89199 gate driver. Full operation of the doubler charge pump, requirements, and best practices for selection of both the pump and the storage capacitors are discussed.

INTRODUCTION

Many systems integrated in automotive applications require support for low-voltage operation. Low-voltage operation, as presented in the automotive standards ISO16750-2 and ISO7637-2, occurs during a cold-crank or warm-crank event. A charge pump is frequently used to support this low-voltage operation.

In an automotive environment, during a cold-crank or warm-crank event, the battery is subjected to transients. During these transient events, the system must operate at voltages as low as 4.5 V. To meet this requirement, the Allegro gate driver includes a regulated doubler charge-pump scheme to create sufficient gate-to-source, V_{GS}, voltage to drive standard MOSFETs during low-voltage-transient conditions. This scheme is ideally suited for applications that must remain fully functional during input-voltage dropouts, such as are typical during automotive cold-crank and warm-crank events. To ensure the safety of the driver and passengers, automotive electronic components must be extremely reliable and stable in severe weather conditions.

This application note describes the main advantages of the Allegro doubler charge pump when used in automotive applications that operate at low battery-supply voltage. Different load conditions and test parameters of the A89199 gate driver are considered.

The A89199 gate driver is supplied by programmable-voltage internal regulator VREG, which provides the current for the low-side gate-driver circuits and the charging current for the bootstrap capacitors. At low battery voltage, the regulated supply is maintained by a charge pump that generally requires a pump capacitor connected between A89199 charge-pump terminals CP1 and CP2. The regulated voltage, V_{REG}, available on the VREG terminal is programmable to 8 V or 11 V, selected by the value of the VRG bit in configuration register 6 of the A89199 gate driver:

- When the VRG bit is set to 1, V_{REG} is set to 11 V.
- When the VRG bit is set to 0, V_{REG} is set to 8 V.

This regulator uses a charge-pump scheme with a nominal switching frequency of 62.5 kHz. The charge pump operates as a regulator doubler or a linear step-down regulator, depending on the input voltage at supply terminal VBB. Regulator operation requires two external capacitors: one pump capacitor and one storage capacitor:

- Pump capacitor CP is connected as close as practicable between terminals CP1 and CP2.
- Storage capacitor CREG is connected as close as practicable between gate-driver terminals VREG and GND. The value of storage capacitor CREG typically depends on the size of the bootstrap capacitors and the total gate charge of the employed external power MOSFETs.

BATTERY CRANKING

Typical automotive gate drivers are powered by the battery system of the vehicle. During an engine cold-crank or warm-crank event, the supply voltage can reduce to a very low level for a short period of time. The Allegro A89199 gate driver is designed to handle these transient conditions down to 4.5 V.

A cold-crank event typically occurs when a vehicle starts when the vehicle battery and engine are both subjected to cold temperature. In this condition, the starter draws a high current from the battery to start the engine, which causes the battery voltage to reduce to an extremely low level, as shown in Figure 1.

A warm-crank event typically occurs when a vehicle starts during a warm condition in which the starter draws current from the battery to start the engine, and the battery voltage reduces, as shown in Figure 2. Warm-crank pulses typically are not as severe as cold-crank pulses, and voltage typically does not reduce as much as in a cold-crank event.

If the battery voltage reduces during a cold-crank or warm-crank condition, automotive electronic components connected to the battery supply must be able to operate without interruption. Many automotive manufacturers use similar profiles for both cold-crank and warm-crank events. Variations are typically within specific voltage levels and timings.

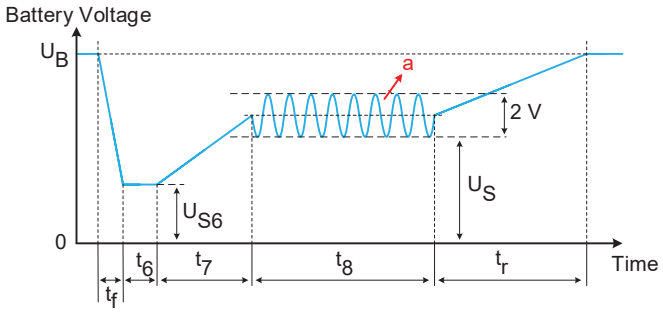

Figure 1: Typical Cold-Crank Profile

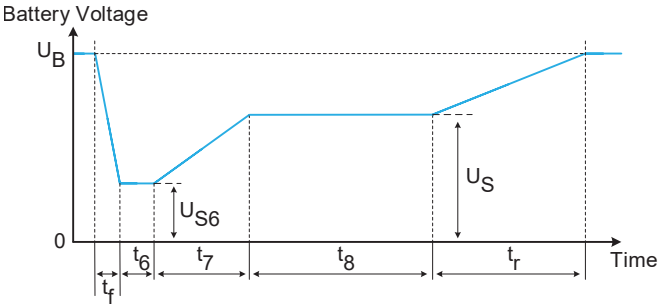

Figure 2: Typical Warm-Crank Profile

The two most commonly used standards providing profile specifications for both cold-crank and warm-cranking conditions in automotive applications are ISO16750-2 and ISO7637-2. Both sets of standards define different pulse profiles for both 12 V and 24 V vehicle systems. Each pulse profile contains specific voltage levels, pulse durations, and other timing information specific to common cold-crank and warm-crank conditions as presented in Figure 1 and Figure 2.

Many automotive original equipment manufacturers (OEMs) design products using specifications that typically refer to one or both of these two standards. These OEM specifications can also provide slight variations from the standards. These variations relate to the unique requirements of the OEM. In the worst-case cold-crank condition, the battery voltage can reduce to less than 3 V for 15 ms, as shown in Figure 1. After a duration of t_6, the battery voltage increases to approximately 7.5 V, where it oscillates between 6.5 V and 8.5 V for a duration of t_8 (typically, a few seconds), then returns to the nominal voltage within a rising time of t_r (typically of few milliseconds). A low-frequency sinusoidal signal, a, is added to the profile shown in Figure 1. The sinusoidal signal of 2 Hz frequency represents the alternator noise during crank. During a warm crank, the battery voltage can reduce to 5 V or 6 V as shown in Figure 2, and voltage duration time t_6 is often shorter than it is for a cold crank, as shown in Table 1. After a short duration of t_6 (approximately 5 ms), the battery voltage increases to approximately 8 V. The battery voltage remains at this level for less than a second, then it returns to the nominal battery voltage. Although a warm-crank profile is similar to a cold-crank profile, the voltage reductions and shortened pulse durations are typically less severe, as presented in Table 1, which presents typical voltage levels and pulse durations for both cold-crank and warm-crank conditions. It can be observed that the warm-crank condition is similar to the cold-crank condition; however, the voltage reduction and duration pulse times are not as extreme due to the warm engine.

Table 1: Typical Cold-Crank and Warm-Crank Parameters

Parameter	Symbol	Cold Crank	Warm Crank
Battery Voltage	U_B	12 V	12 V
Supply Voltage	U_{S6} at t_6	3 V	5 V or 6 V
	U_S at t_8	6.5 V	8 V
Falling Slope Time	t_f	5 ms	5 ms
Duration Time	t_6	15 ms	5 ms
	t_7	50 ms	50 ms
	t_8	10 s	700 ms
	t_r	100 ms	100 ms
Sinusoidal Signal	a	2 Hz, 2 V	–

DOUBLER CHARGE PUMP OPERATION

The charge pump is intended to supply the bridge driver at low-supply battery voltage. A simplified block diagram of the doubler charge pump and its external components, pump capacitor CP and storage capacitor CREG, is shown in Figure 3. The charge-pump input voltage is V_{BB}, and the charge-pump output voltage is V_{REG}. The regulator voltage, V_{REG}, is generated by a one-stage charge pump, as a multiplying effect of the input voltage, V_{BB}, using pump capacitor CP. Ideally, if losses are not present in the system, the charge pump can provide a voltage increase equal to the input supply voltage, V_{BB}.

An internal clock with a nominal switching frequency, f_{PUMP}, of 62.5 kHz (derived from the Allegro A89199 reference clock frequency of 2 MHz) drives internal MOSFET switches SWA, SWB, SWC, SWD, and SWE of the pump circuit, as shown in Figure 3. the switching frequency it can be expressed as:

$$f_{PUMP} = 2\ MHz/32 = 62.5\ kHz$$

The doubler charge-pump circuit shown in Figure 3 has two operating states: charging and pumping. Diode D1 is an on-chip diode. In linear step-down operating mode or buck mode, when supply voltage V_{BB} is greater than approximately 13 V, diode D1 is forward-conducting, and all other diodes in Figure 3 are internal MOSFET-switching body diodes.

The doubler charge-pump circuit functions as follows:

- When external capacitor CP (connected between terminals CP1 and CP2) is charging, MOSFET switches SWA, SWB, and SWC are turned on, and MOSFET switches SWD and SWE are opened.
- When the charge is transferring from pumping capacitor CP to storage capacitor CREG, MOSFET switches SWA, SWD, and SWE are turned on, and MOSFET switches SWB and SWC are opened.
- The voltage across storage capacitor CREG is regulated by internal monitoring of the voltage on the VREG terminal. When the VREG terminal reaches a nominal voltage of approximately 13 V, MOSFET switches SWA, SWD, and SWE are opened.
- The charging current of pump capacitor CP is controlled by a nominal active current limit of 100 mA.
- During the charging cycle, the voltage on terminal CP2 is limited by the value of the pump capacitor, the charging current, the switching frequency, and the duty cycle of the charge-pump regulator oscillator.
- The discharge current of pump capacitor CP or the charging current of storage capacitor CREG is limited by a nominal active current limit of 100 mA.

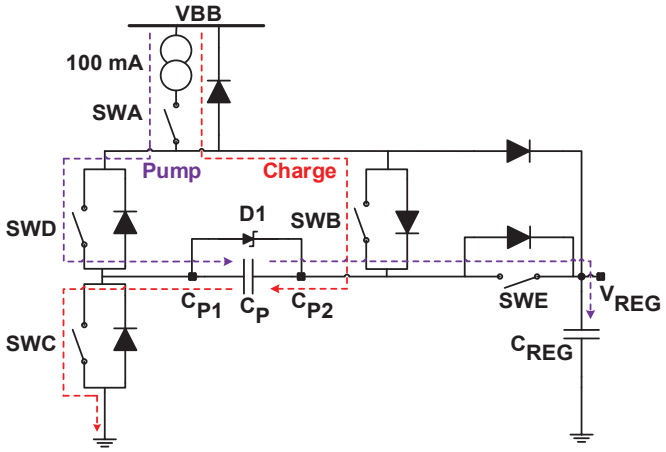

Figure 3: Simplified Charge-Pump Circuit, A89199

COMPONENT SELECTIONS

To generate the output voltage, V_{REG}, pump capacitor CP boosts the supply voltage, V_{BB}, while output capacitor CREG acts as a storage capacitor. The selection of the value and type of capacitor for pump capacitor CP should include consideration for: regulator voltage, V_{REG}; regulator current, I_{REG}; charge pump switching frequency, f_{PUMP}; capacitor voltage ripple, V_{RIPPLE}; dynamic response; and losses due to the equivalent series resistance of the capacitor.

When the value of pump capacitor CP increases, the start-up time and the time to respond to load change both lengthen, and the equivalent series resistance (ESR) increases. This results in losses. In a ceramic capacitor, when the applied voltage increases, capacitance reduces. Thus, the voltage rating of ceramic pump capacitor CP should be adequately selected.

For a typical application, a capacitor rated to at least 25 V with a minimum capacitance value of 470 nF is recommended. For stable operation in the A89199 gate driver, this capacitor should be connected between terminals CP1 and CP2.

The voltage ripple, V_{RIPPLE}, of pump capacitor CP can be estimated by considering the minimum pump capacitor value of 470 nF, the regulator current of 15 mA at low supply voltage, V_{BB}, of 5 V, and the charge-pump switching frequency of 62.5 kHz. The voltage ripple of pump capacitor CP can be expressed as follows:

$$V_{RIPPLE} = \frac{I_{REG}}{f_{PUMP} \times C_P} = \frac{15\ mA}{62.5\ kHz \times 470\ nF} = 0.5\ V$$

Use of capacitor with a value greater than 470 nF can reduce this voltage ripple. However, any increase to the value of pump capacitor CP slows the speed of both start-up and response to a load change during operation.

The regulator voltage, V_{REG}, supplies current for the low-side gate-drive circuits and the charging current for the bootstrap capacitors. This means that the value of storage capacitor CREG, located between gate-driver terminals VREG and GND, should be high enough to minimize the transient voltage reduction on terminal VREG for the combination of a low-side MOSFET turn-on and a bootstrap capacitor recharge.

- For block commutation control—also known as trapezoidal drive, where only one high side and one low side switch during each pulse-width modulation (PWM) period—a minimum value of 20 times bootstrap capacitor CBOOT is reasonable.
- For sinusoidal control schemes, a minimum value of 40 times bootstrap capacitor CBOOT is recommended.

Because the maximum working voltage of capacitor CREG never exceeds the maximum V_{REG} voltage of 11.7 V for the A89199 gate driver, the voltage rating of capacitor CREG can be as low as 15 V. However, to reduce any impact that the operating voltage might have on the capacitance value, a capacitor rated to at least twice the maximum working voltage, V_{REG}, is recommended. To optimize performance, a ceramic-type capacitor (not electrolytic) rated to at least 25 V is recommended for capacitor CREG.

EXPERIMENTAL RESULTS

The performance of the doubler charge-pump circuit, as experimentally verified on the bench, is presented in Figure 3.

Several experimental tests were performed on the bench using the A89199 gate driver, which has an internal designed regulator charge pump. The test bench contains a DC power supply, a 1 GHz Tektronix scope, and the A89199 soldered to a two-layer Allegro demonstration board.

In the experimental tests, a low constant-voltage level of 5 V was applied to supply terminal VBB of the A89199 gate driver under test, and the performance of the charge-pump circuit was observed by monitoring voltages V_{BB}, V_{REG},V_{CP1}, and V_{CP2}, as presented in Figure 4, Figure 5, and Figure 6.

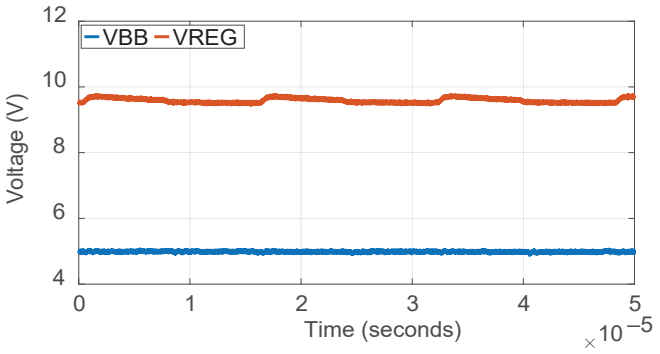

Figure 4: V_{BB} and V_{REG} with Regulator Current, I_{REG} ≈ 15 mA

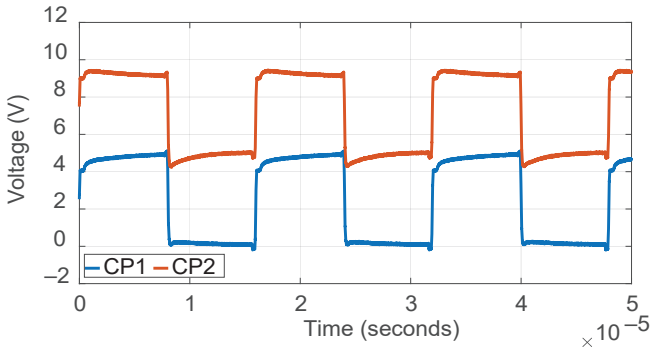

Figure 5: CP1 and CP2 with Regulator Current, I_{REG} ≈ 15 mA

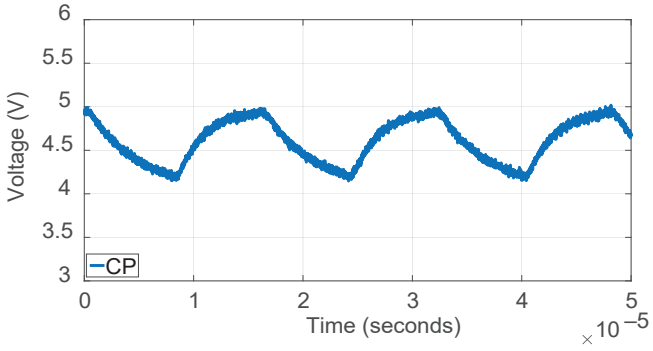

Figure 6: Pump Capacitor, C_P, with Regulator Current, I_{REG} ≈ 15 mA

For V_{BB} voltage set to 5 V, the measured regulator voltage, V_{REG}, is approximately 9.75 V, as shown in Figure 4. For V_{BB} set to 5 V and regulator load current, I_{REG}, of approximately 15 mA, the performance of a 470 nF capacitor demonstrated as pump capacitor CP, charged through terminal CP2, pumping 22 µF storage capacitor CREG through terminal CP1, is shown in Figure 5 and Figure 6.

Charge-pump load regulation measurements for two V_{REG} settings, 8 V and 11 V, of the A89199 gate driver are presented in Figure 7 and Figure 8. The VRG bit in configuration register 6 of the A89199 gate driver was used to set V_{REG}. The collected data are consistent with the V_{REG} output voltage limits presented in the A89199 datasheet.

The load regulation data presented in Figure 7 and Figure 8 were obtained at room temperature for different supply voltage levels varying from V_{BB} = 5 V, to V_{BB} = 50 V.

Results for the regulator voltage set to V_{REG} = 8 V (by programming the VRG bit in configuration register 6 to 0) are shown in Figure 7:

- For supply voltage, V_{BB}, greater than 4.5 V and less than or equal to 6 V, the measured regulator voltage, V_{REG}, is approximately 8.2 V with loading current up to 15 mA.
- For supply voltage, V_{BB}, greater than 6 V and less than or equal to 50 V, the measured regulator voltage, V_{REG}, is approximately 8.15 V with loading current up to 50 mA.

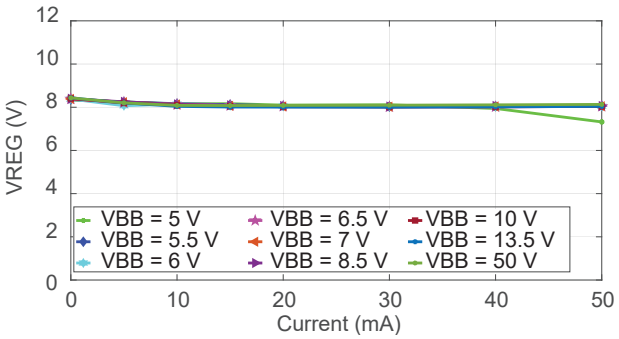

Figure 7: Measured Load Regulation with V_{REG} set to 8 V

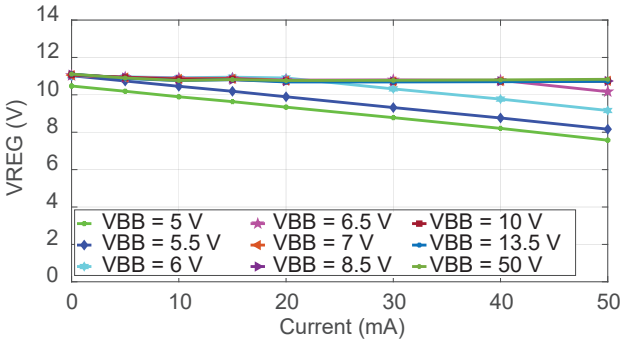

Figure 8: Measured Load Regulation with V_{REG} set to 11 V

Results for the regulator voltage, V_{REG}, set to 11 V (by setting the VRG bit in the configuration register 6 to 1) are shown in Figure 8:

- For supply voltage V_{BB} greater than 4.5 V and less than or equal to 6 V, the measured regulator voltage, V_{REG}, is approximately 9.75 V with loading current up to 15 mA.
- For supply voltage, V_{BB}, greater than 6 V and less than or equal to 50 V, the measured regulator voltage, V_{REG}, is approximately 10.85 V with loading current up to 50 mA.

The bench test results presented in Figure 7 and Figure 8 show that the charge-pump regulator provides the supply of the A89199 gate driver for battery voltage, V_{BB}, down to 5 V and allows the A89199 gate driver to operate with a reduced supply voltage, V_{BB}, down to 5 V. The self-running doubler charge pump of the A89199 gate driver is able to charge a 470 nF capacitor in approximately 8 µs, as shown in Figure 6, with a measured ripple voltage, V_{RIPPLE}, of approximately 0.6 V. This allows the A89199 to have a rapid response time and to drive the external MOSFETs very quickly, allowing fast switch-on and switch-off of the load in both cold-crank and warm-crank conditions.

The performance of the doubler charge pump of the A89199 gate driver was furthermore investigated by estimating the total power dissipation of the A89199 gate driver. The total power dissipation of the A89199 gate driver can be estimated as the sum of the charge pump power, P_{CPUMP}, the switching power, P_{SW}, and the bias power, P_{BIAS}, and it can be expressed as follows:

$$P_{TOTAL}=P_{BIAS} \times P_{CPUMP} \times P_{SW}$$

$$P_{BIAS} = V_{BB} \times I_{BB}$$

$$For\ V_{BB} < 13\ V: P_{CPUMP} = [(2 \times V_{BB}) - V_{REG}] \times I_{AV}$$

$$For\ V_{BB} \geq 13\ V: P_{CPUMP} = [V_{BB} - V_{REG}] \times I_{AV}$$

$$P_{SW} = Q_{GATE} \times V_{REG} \times N \times f_{PWM} \times Ratio$$

$$I_{AV} = Q_{GATE} \times N \times f_{PWM}$$

$$Ratio = 10/(R_{GATE} \times 10)$$

where N represents the number of MOSFETs switching during a PWM cycle.

The simplified block diagram of the charge-pump circuit shown in Figure 3 offers the basic switching elements required to implement a doubler charge pump, when combined with external capacitors for enhanced low supply voltage, V_{BB}, operation. The regulation set point for the linear step-down regulator is nominally set at 13 V, as illustrated in the estimated current and power data in Figure 9. The estimated current and power results in Figure 9 were calculated by taking into consideration the required application parameters presented in Table 2. As long as the supply battery voltage, V_{BB}, is greater than 13 V, MOSFET switches SWA, SWD, and SWE (presented in the simplified charge pump circuit in Figure 3) are opened; and the charge pump oscillator shuts down. In this state, on-chip diode D1 is forward-conducting in the linear step-down regulator. The obtained results shown in Figure 9 also demonstrate that, at less than approximately 13 V, the doubler charge pump actively regulates, and the maximum current that the doubler charge pump can supply typically depends on the value of pump capacitor CP, the quality of pump capacitor CP, and the charge-pump switching frequency of 62.5 kHz.

NOTE: The estimated power in Figure 9 is greater than the actual power dissipated by the A89199 device.

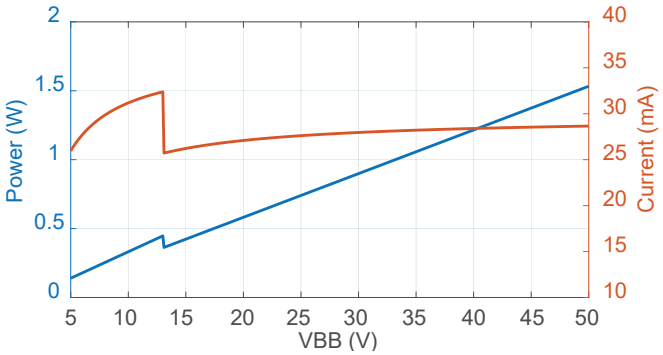

Figure 9: Estimated Power and Current, A89199

Table 2: Application Parameters

Required Parameters			
Description	**Symbol**	**Value**	**Unit**
PWM Frequency	f_{PWM}	20	kHz
Total Gate Charge	Q_{GATE}	140	nC
Gate Resistance	R_{GATE}	33	Ω
Regulator Voltage	V_{REG}	11	V
Supply Battery Voltage	V_{BB}	5 to 50	V

SUMMARY

This application note has presented the functionality, performance, and component selection of the doubler charge pump employed in the A89199 gate driver. The obtained results demonstrate that, at low supply voltage, V_{BB}, events such as cold-crank and warm-crank conditions in automotive applications—for example, in an electric power steering (EPS) system—the regulated voltage, V_{REG}, is maintained by a charge-pump boost converter. The charge pump described in this paper has similar performance to the charge pump currently used in the A4911, A4913, A4916 and A4918 devices from Allegro.

Revision History

Number	Date	Description	Responsibility
–	February 20, 2026	Initial release	K. Tshiloz

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