A1337

Precision, Hall-Effect Angle Sensor IC with SPI and SENT Outputs

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position and rotation direction measurement
  - □ Circular vertical Hall (CVH) technology provides a single-channel sensor system, with air gap independence
- 12-bit resolution possible in low-RPM mode, 10-bit resolution in high-RPM mode
- Angle refresh rate (output rate) configurable between 25 and 3200 µs through EEPROM programming
  - □ Capable of sensing magnetic rotational speeds up to 7600 rpm, and up to 30,000 rpm with reduced accuracy
- Serial peripheral interface (SPI; mode 3) and single-edge nibble transmission (SENT) [1]

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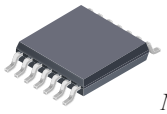
PACKAGES:

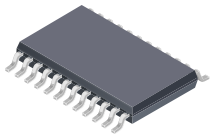
14-pin TSSOP (Suffix LE)



Single SoC

Not to scale

24-pin TSSOP (Suffix LE)



Dual Independent SoCs

DESCRIPTION

The A1337 is a 0° to 360° angle sensor IC that provides contactless high-resolution angular position data based on magnetic circular vertical Hall (CVH) technology. It has a system-on-chip (SoC) architecture that includes: a CVH front end, digital signal processing, digital SPI, and SENT outputs. It also includes on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration and configuration parameters. The A1337 is ideal for automotive applications requiring 0° to 360° angle measurements, such as electronic power steering (EPS), seatbelt motor position systems, rotary PRNDLs, and throttle systems.

The A1337 was designed with safety-critical application requirements in mind. It includes user-controlled, on-chip logic built-in self-test (LBIST) and full signal path diagnostics to enable customers to determine if the IC is operating in a proper manner.

The A1337 includes integrated turns-counter and low-power mode functions. The low-power mode enables the device to be connected directly to the vehicle battery and minimizes power consumption when the vehicle is in the key-off state. The turns-counter function allows the device to keep track of

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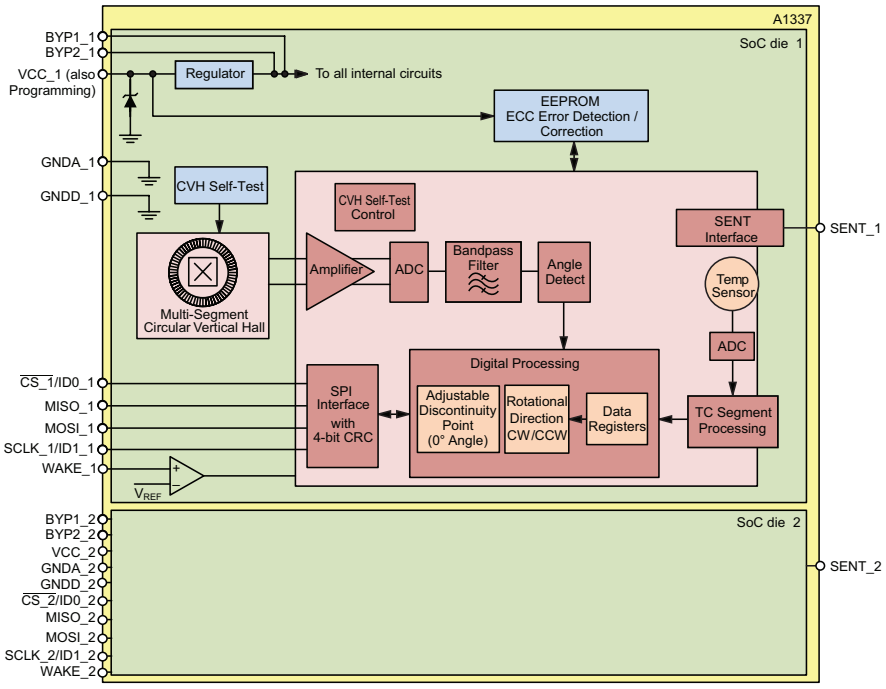

Figure 1: A1337 Magnetic Circuit and IC Diagram

FEATURES AND BENEFITS (continued)

- □ SPI interface provides a robust communication protocol for fast angle readings [1]
- □ SENT output supports four modes: SAEJ2716 (JAN2010) and Allegro proprietary options of triggered SENT (TSENT), sequential SENT (SSENT), and addressable SENT (ASENT) [1]
- □ Programmable via Manchester encoding on the VCC line, reducing external wiring [1]
- □ SPI and SENT interfaces allow use of multiple independent sensors for applications that require redundancy [1]

• Advanced diagnostics to support safety-critical applications, including:
- □ On-chip, user-controlled logic built-in self-test (LBIST) and signal path diagnostics
- □ 4-bit CRC on SPI messages
- □ User-programmable missing magnet error flag for notifying controller of low magnetic field level

• Diagnostics are initiated over the SPI or SENT interface and can directly test proper operation of the IC in safety-critical applications

• Integrated turns counter tracks magnet rotation in CW/CCW direction from –1280 to +1280 counts, even when vehicle is in key-off state
- □ Count updates are user-selectable to be every 180° or every 45° degree of magnet rotation
- □ WAKE pin for external wake-up trigger can be used to automatically detect motion > 100 rpm

• Low-power mode enables direct connection to vehicle battery
- □ User-programmable duty cycle optimizes low-power mode current consumption (typically 85 µA per die)
- □ Ultralow-power transport mode

• EEPROM with error correction control (ECC) configuration, sensor calibration including end-of-line adjustments like programmable angle reference (0°) position and rotation direction (CW or CCW)

• Available in both single-die and dual-die configurations
- □ Dual-die devices contain two independent dies housed within a single package

• Absolute maximum V_{CC} of 26.5 V for increased robustness and direct connection to automotive vehicle battery

[1] For more details, see the Selection Guide table.

DESCRIPTION (continued)

either 45° or 180° turns of the motor when the part is in low-power mode, monitoring the motor position even when the vehicle is in the key-off state.

The A1337 supports a low-RPM mode for slower-rate applications and a high-RPM mode for high-speed applications. The high-RPM mode is for applications that require higher refresh rates to minimize error due to latency. Low-RPM mode is for applications that require higher resolution operating at lower angular velocities.

The A1337 is available in a single-die 14-pin TSSOP and a dual-die 24-pin TSSOP. Both packages are lead (Pb) free with 100% matte tin leadframe plating.

SELECTION GUIDE

Part Number	System Die	Output Protocols	Package	Packing [1]
A1337LLETR-DD-T	Dual	SPI and SENT	24-pin TSSOP	4000 pieces per 13-in. reel
A1337LLETR-T	Single	SPI and SENT	14-pin TSSOP	4000 pieces per 13-in. reel

[1] Contact Allegro for additional packing options.

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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	26.5	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
Forward WAKE Pin Voltage [1]	$V_{WAKEmax}$	Maintain nominal WAKE pin threshold levels ($V_{WAKE(LOTH)}$ and $V_{WAKE(HITH)}$)	2.0	V
All Other Pins Forward Voltage	V_{IN}		5.5	V
All Other Pins Reverse Voltage	V_R		0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

[1] Sustained high-temperature exposure of the WAKE pin to large voltages may result in downward shifts of $V_{WAKE(LOTH)}$ and $V_{WAKE(HITH)}$. Restricting voltages from exceeding $V_{WAKEmax}$ minimizes the likelihood of such shifts. Operation with WAKE voltages below 0.55 V prevents all occurrences. Short duration exposure to voltages between 0.55 V and $V_{WAKEmax}$ do not result in significant shifts.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see the Application Information section

Characteristic	Symbol	Test Conditions [2]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-24 package	117	°C/W
		LE-14 package	82	°C/W

[2] Additional thermal information available on the Allegro website.

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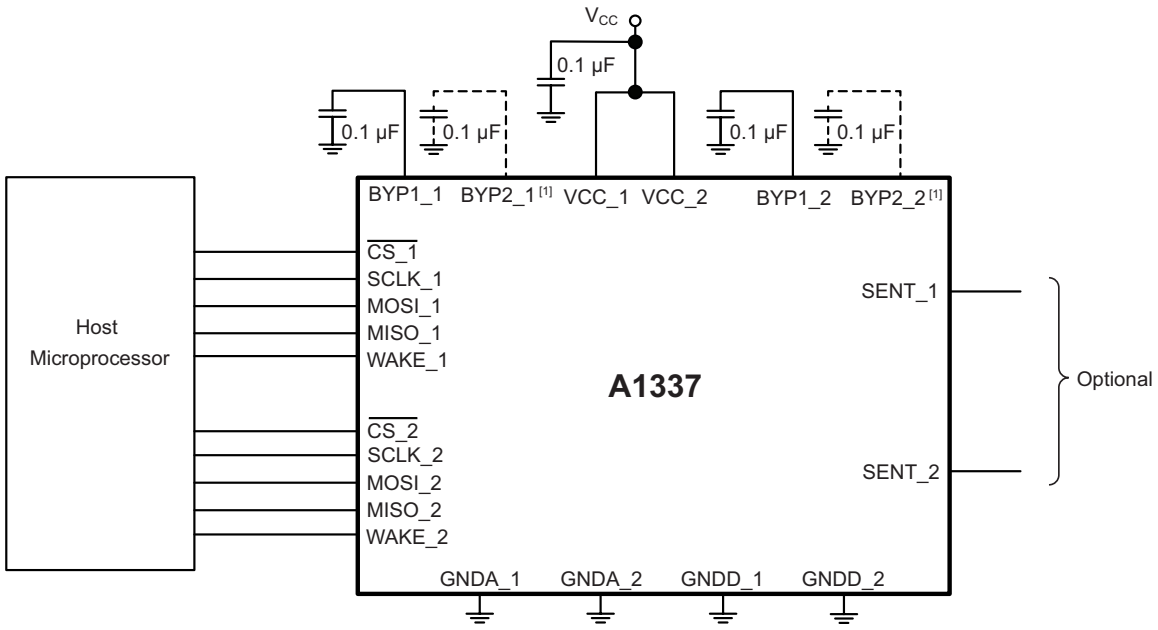
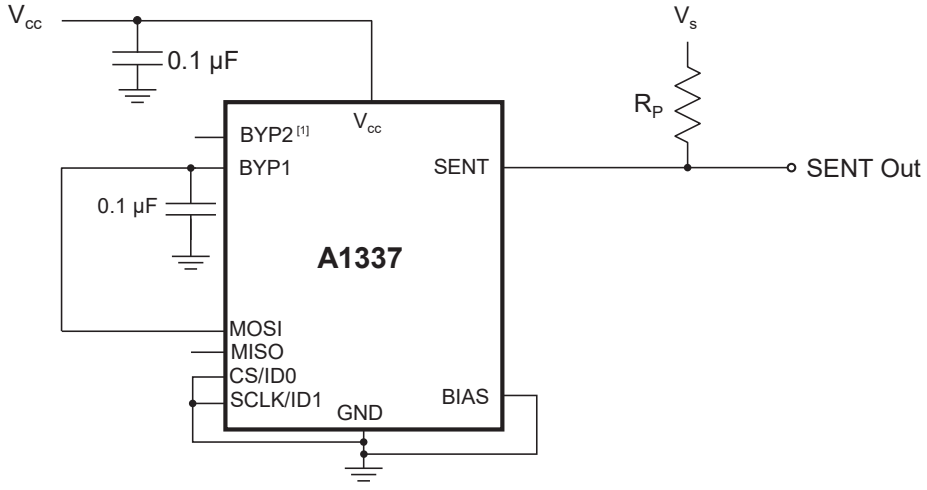


Either or both internal SoCs can be operated simultaneously.
(For application circuits that require a higher level of EMC immunity, see the EMC Reduction section.)
[1] Secondary bypass capacitors only required when using elevated SPI output voltage. For availability, contact Allegro.

Figure 2: Typical A1337 Configuration Using SPI Interface



ID0/ID1 brought to BYP or GND to configure Manchester address.
When configuring an IC for address 00_2, MOSI should be tied to BYP.
[1] Secondary bypass capacitors only required when using elevated SPI output voltage. For availability, contact Allegro.

Figure 3: Typical A1337 Configuration Using SENT Output with ID Value of 00_2

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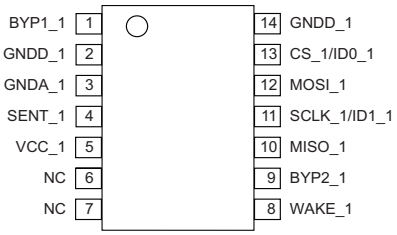
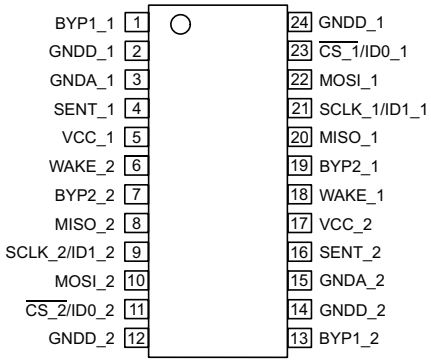
PINOUT DIAGRAMS AND TERMINAL LIST



14-Pin TSSOP LE Package Pinouts



24-Pin TSSOP LE Package Pinouts

Terminal List Table

Pin Name	Pin Number		Function
	LE-14	LE-24	
BYP1_1	1	1	External bypass capacitor terminal for internal regulator (die 1)
BYP2_1	9	19	External bypass capacitor terminal for internal regulator (die 1)
BYP1_2	–	13	External bypass capacitor terminal for internal regulator (die 2)
BYP2_2	–	7	External bypass capacitor terminal for internal regulator (die 2)
$\overline{\text{CS}}$_1/ID0_1	13	23	Option 1: SPI chip-select terminal, active low input (die 1)
			Option 2: ID0 bit to indicate peripheral address for SSENT or ASENT communication modes only (die 1)
$\overline{\text{CS}}$_2/ID0_2	–	11	Option 1: SPI chip-select terminal, active low input (die 2)
			Option 2: ID0 bit to indicate peripheral address for SSENT or ASENT communication modes only (die 2)
GNDA_1	3	3	Device analog ground terminal (die 1)
GNDA_2	–	15	Device analog ground terminal (die 2)
GNDD_1	2, 14	2, 24	Device digital ground terminal (die 1)
GNDD_2	–	12, 14	Device digital ground terminal (die 2)
MISO_1	10	20	SPI controller input/peripheral output (die 1)
MISO_2	–	8	SPI controller input/peripheral output (die 2)
MOSI_1	12	22	SPI controller output/peripheral input (die 1)
MOSI_2	–	10	SPI controller output/peripheral input (die 2)
SLCK_1/ID1_1	11	21	Option 1: SPI clock terminal (die 1)
			Option 2: ID1 bit to indicate peripheral address for SSENT or ASENT communication modes only (die 1)
SCLK_2/ID1_2	–	9	Option 1: SPI clock terminal (die 2)
			Option 2: ID1 bit to indicate peripheral address for SSENT or ASENT communication modes only (die 2)
SENT_1	4	4	SENT output (die 1); SENT for A1337LLETR-DD-T, A1337LLETR-T
SENT_2	–	16	SENT output (die 2); SENT for A1337LLETR-DD-T, A1337LLETR-T
WAKE_1	8	18	External wake-up signal input (die 1)
VCC_1	5	5	Power supply (die 1); also used for EEPROM programming
VCC_2	–	17	Power supply (die 2); also used for EEPROM programming
WAKE_2	–	6	External wake-up signal input (die 2)
NC	6, 7	–	Not internally connected; tie to GNDD

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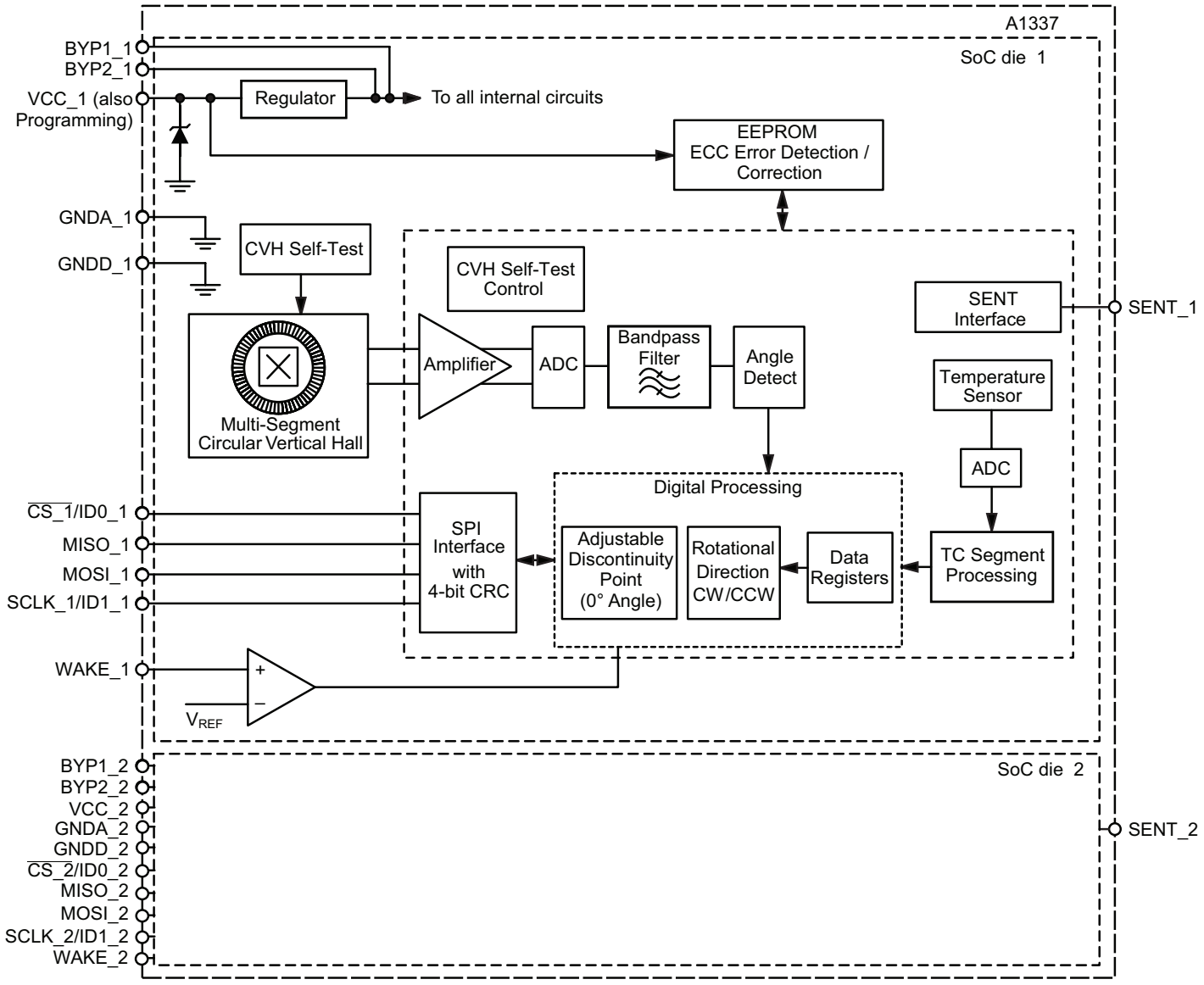

Figure 4: Functional Block Diagram

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OPERATING CHARACTERISTICS: Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}		3.7	–	16	V
Full-Power Mode Supply Current	$I_{CC(AWAKE)}$	Each die, T_A = 150°C	–	8.25	10	mA
Low-Power Mode Average Supply Current	$I_{CC(LP)}$	Each die, target RPM = 0, T_A = 25°C, 98 ms sleep time	–	55	–	µA
		Each die, A1337 in Transport Mode, T_A = 150°C	–	30	–	µA
Undervoltage Lockout Threshold Voltage [3]	V_{UVLOHI}	Maximum V_{CC}, dV/dt = 1 V/ms, T_A = 25°C	–	–	3.6	V
	$V_{UVLOLOW}$	Maximum V_{CC}, dV/dt = 1 V/ms, T_A = 25°C	2.9	–	–	V
VCC Low Flag Threshold [4]	V_{UVLOTH}		3.5	–	3.9	V
Supply Zener Clamp Voltage	V_{ZSUP}	I_{CC} = $I_{CC(AWAKE)}$ + 3 mA, T_A = 25°C	26.5	40	–	V
Reverse-Battery Current	I_{RCC}	V_{RCC} = –18 V, T_A = 25°C	–5	–	0	mA
Power-On Time [5]	t_{PO}		–	300	–	µs
Bypass1 Pin Output Voltage [6]	V_{BYP1}	T_A = 25°C, C_{BYP} = 0.1 µF	2.5	2.7	2.9	V
Bypass2 Pin Output Voltage [6] (Elevated SPI Output Mode)	V_{BYP2}	T_A = 25°C, C_{BYP2} = 0.1 µF; For availability, contact Allegro	2.9	3.1	3.3	V
WAKEx INPUT SPECIFICATIONS						
WAKE Enable High Threshold Voltage	$V_{WAKE(HITH)}$		–	215	–	mV
WAKE Enable Low Threshold Voltage	$V_{WAKE(LOTH)}$		–	115	–	mV
WAKE Input Resistance	R_{WAKE}		–	1	–	MΩ
SPI INTERFACE SPECIFICATIONS						
Digital Input High Voltage	V_{IH}	MOSIx, SCLKx, $\overline{CS}$x pins	2.4	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSIx, SCLKx, $\overline{CS}$x pins	–	–	0.5	V
CSx Pin Input Bias Current	I_{BIAS}	V_{CSx} = 3.3 V	–	15	–	µA
SPI Output High Level	V_{OH1}	MISOx pins, C_L = 20 pF, C_{BYP1} = 0.1 µF, C_{BYP2} grounded	2.5	2.7	2.9	V
SPI Output High Level (Elevated SPI Output Mode)	V_{OH2}	MISOx pins, C_L = 20 pF, C_{BYP1} = 0.1 µF, C_{BYP2} = 0.1 µF; for availability, contact Allegro	2.9	3.1	3.3	V
SPI Output Low Voltage	V_{OL}	MISOx pins, C_L = 20 pF	–	0.3	–	V
SPI Clock Frequency [7]	f_{SCLK}	MISOx pins, C_L = 20 pF	0.1	–	10	MHz
SPI Clock Duty Cycle [7]	D_{fSCLK}	$SPICLK_{DC}$, 5 V compliant	40	-	60	%
SPI Frame Rate [7]	t_{SPI}	5 V compliant	5.8	–	588	kHz
Chip-Select to First SCLK Edge [7]	t_{CS}	Time from $\overline{CS}$x going low to SCLKx falling edge	50	–	–	ns
Data Output Valid Time [7]	t_{DAV}	Data output valid after SCLKx falling edge	–	–	40	ns
MOSI Setup Time [7]	t_{SU}	Input setup time before SCLKx rising edge	25	–	–	ns
MOSI Hold Time [7]	t_{HD}	Input hold time after SCLKx rising edge	40	–	–	ns
SCLK to CS Hold Time [7]	t_{CHD}	Hold SCLKx high time before $\overline{CS}$x rising edge	5	–	–	ns
Capacitive Load [8]	C_L	Loading on digital output (MISOx) pin with SPI clock frequency = 10 MHz	–	–	20	pF

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions		Min.	Typ. [1]	Max.	Unit [2]
SENT PROTOCOL SPECIFICATIONS (A1337LLETR-DD-T and A1337LLETR-T variants only)							
SENT Message Duration	t_{SENT}	Tick time = 3 µs		–	–	1	ms
Minimum Programmable SENT Message Duration	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks		–	96	–	µs
SENT Output Signal	$V_{SENT(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ		–	–	0.2	V
		2 kΩ ≤ R_{pullup} < 5 kΩ		–	–	0.4	V
	$V_{SENT(H)}$	Minimum R_{pullup} = 2 kΩ		0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ		0.7 × V_S	–	–	V
SENT Output Trigger Signal	$V_{SENTtrig(L)}$			–	–	1.4	V
	$V_{SENTtrig(H)}$			2.8	–	–	V
Minimum Time Frame for SENT Trigger Signal	$t_{SENTMIN}$	Tick time = 0.5 µs, 3 data nibbles, SCN, and CRC, nibble length = 27 ticks		2	–	–	µs
Triggered Delay Time	t_{dSENT}	From end of trigger pulse to beginning of SENT message frame TSENT (SENT_MODE 3 and SENT_MODE 4)		–	7	–	tick
Maximum Sink Current	I_{LIMIT}	Output FET on, T_A = 25°C		–	30	–	mA
DIAGNOSTIC SPECIFICATIONS							
CVH Self-Test Time	t_{CVHST}			–	23	–	ms
Logic BIST Coverage versus Time	$t_{LBISTXX}$	70% coverage		–	10	–	ms
EEPROM PROGRAMMING PULSES							
Pulse High Time	$t_{PULSE(H)}$	Time above minimum pulse voltage		8	10	11	ms
Rise Time	t_r	10% to 90% of minimum pulse level		300	–	–	µs
Fall Time	t_f	10% to 90% of minimum pulse level		60	–	–	µs
Pulse Voltage	V_{PULSE}	Applied on VCC line		18	19	19.5	V
Separation Time	$t_{PULSE(f-r)}$	Timing between first pulse dropping below 6 V and second pulse rising above 6 V		0.002	–	50	ms
MAGNETIC CHARACTERISTICS							
Magnetic Field	B	Range of input field		–	–	1500	G_{pp}
TURNS COUNTER CHARACTERISTICS							
Sleep State Period [7]	t_{SLEEP}	Default value is 98 ms Programmable from 2 to 512 ms via EEPROM selection.		2	–	512	ms
Awake State Period	t_{AWAKE}			–	260	–	µs
Awake State Threshold Acceleration [9]	$\varepsilon_{AWAKE(TH)}$	Low-power mode		–	–	6000	°/s²
Awake State Threshold Speed [10]	$S_{AWAKE(TH)}$			–	100	–	rpm
Wake-Up Delay [11][12]	t_{dWAKE}	Measured from V_{WAKEx} > $V_{WAKE(HITH)}$, V_{WAKEx} rising, to beginning of sampling for turns counting	Low-RPM mode	–	500	–	µs
			High-RPM mode	–	300	–	µs
Counter Range [13]	RANGE	Stored as two's complement		–1280	–	1280	count

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OPERATING CHARACTERISTICS (continued): Valid over the full operating voltage and ambient temperature ranges, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ. [1]	Max.	Unit [2]
ANGLE CHARACTERISTICS						
Digital Output Word Length [8]	RES_{ANGLE}		–	12	–	bit
Effective Resolution [14]		B = 300 G, T_A = 25°C, ORATE = 0	–	11.59	–	bit
Angle Refresh Rate [15]	t_{ANG}	High-RPM mode	–	25	–	µs
		Low-RPM mode, AVG = 011 (varies with AVG mode, refer to the Programming Manual available on the Allegro software portal)	–	200	–	µs
Response Time	$t_{RESPONSE}$	Low-RPM mode (see Figure 5)	–	60	–	µs
Angle Error	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, B = 300 G, target rpm = 0	–	0.5	–	degrees
		T_A = 150°C, ideal magnet alignment, B = 300 G, target rpm = 0	–1.3	–	1.3	degrees
Angle Noise	N_{ANG}	T_A = 25°C, B = 300 G, 3-sigma noise, no internal filtering	–	0.35	–	degrees
		T_A = 150°C, no internal filtering, B = 300 G, 3-sigma noise, target rpm = 0	–	0.55	–	degrees
Temperature Drift	$ANGLE_{DRIFT}$	T_A = 150°C, B = 300 G	–1.4	–	1.4	degrees
		T_A = –40°C, B = 300 G	–	±1	–	degrees
Angle Drift Over Lifetime	$ANGLE_{DRIFT-LIFE}$	B = 300 G, typical maximum drift observed after AEC-Q100 qualification testing	–	±0.5	–	degrees

[1] Typical data is at T_A = 25°C and V_{CC} = 5 V, and it is for design estimates only.
[2] 1 G (gauss) = 0.1 mT (millitesla).
[3] At power-on, a die does not respond to commands until V_{CC} rises above V_{UVLOHI}. After that, the die performs and responds, typically until V_{CC} drops below $V_{UVLOLOW}$.
[4] VCC low threshold flag is sent via the SPI interface as part of the angle measurement.
[5] During the power-on time period, the A1337 SPI transactions are not guaranteed.
[6] The output voltage and current specifications are to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during full-power operation.
[7] Parameter is not guaranteed at final test. Determined by design.
[8] RES_{ANGLE} represents the number of bits of data available for reading from the die registers.
[9] In low-power mode, acceleration greater than $\varepsilon_{AWAKE(TH)}$ may result in missed 180° crossings. To capture greater rates of acceleration, the WAKE pin should be asserted.
[10] When the die logic determines the velocity of the magnet is greater than $S_{AWAKE(TH)}$, the die remains in the awake state.
[11] Measured from $V_{WAKEx} > V_{WAKE(HITH)}$, V_{WAKEx} rising, to beginning of sampling for turns counting. Alternative conditions for wake-up are:
- $V_{WAKEx} > V_{WAKE(HITH)}$, V_{IH}.
- Host removes sleep condition by means of the SPI lines.
- $S_{AWAKE} > 100$ rpm.

[12] To calculate low-RPM mode, time = 300 µs + 25 × 2^{AVG}. Given AVG = 011 = 3 (decimal), $2^3 = 8$.
[13] Turns-counter step size can be selected between 45 degrees and 180 degrees, by setting an EEPROM bit.
[14] Effective resolution is calculated using:

$$log_2(360) - log_2\left(\frac{1}{n}\sum_{i=1}^{n}\sigma_i\right)$$

[15] The rate at which a new angle reading becomes ready.

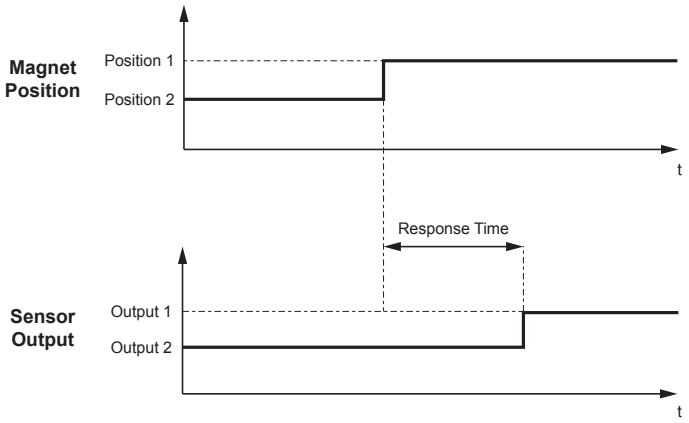

Figure 5: Definition of Response Time

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FUNCTIONAL DESCRIPTION

Overview

The A1337 is a rotary position Hall-sensor-based device. It incorporates up to two electrically independent Hall-based sensor dies in the same surface-mount package to provide solid-state consistency and reliability and to support a wide variety of automotive applications. Each Hall-sensor-based die measures the direction of the magnetic field vector through 360° in the x-y plane (parallel to the branded face of the device) and computes an angle measurement based on the actual physical reading, as well as any internal configuration parameters that have been set by the user. The output of each die is used by the host microcontroller to provide a single channel of target data.

This device is an advanced, programmable system-on-chip (SoC). Each integrated circuit includes a circular vertical Hall (CVH) analog front end, a high-speed sampling analog-to-digital converter, digital filtering, digital signal processing, and an SPI/SENT output.

Angle Measurement

The A1337 can monitor the angular position of a rotating magnet at speeds ranging from 0 to more than 7,600 rpm. At lower rotational speeds, the A1337 is able to measure angle data with minimal angular latency between the actual magnet and sensor output. As the rpm increases, the angular latency between the magnet and sensor output also increases. Above 7,600 rpm, the A1337 continues to provide angle data; however, the accuracy is proportionally reduced.

The A1337 can be configured to operate in two angular measurement modes of operation: low-RPM mode and high-RPM mode. Low-RPM mode allows a programmable number of internal angle samples to be accumulated and averaged, providing greater resolution while reducing the update rate. This is suitable for lower-RPM applications (0 to ≈500 rpm). For high-speed applications, the averaging function may be bypassed by operating in high-RPM mode.

The actual update rate of low-RPM mode can be changed by setting the AVERAGING bits in the EEPROM (for details, see the Programming Manual available on the Allegro software portal). The different levels of averaging available in low-RPM mode are described in Table 1. A setting of 0002 is equivalent to high-RPM mode.

Table 1: Refresh Rate Based on Quantity of Samples Averaged

AVG [2:0]	Quantity of Samples Averaged	Refresh Rate (µs)
000	1	25
001	2	50
010	4	100
011	8	200
100	16	400
101	32	800
110	64	1600
111	128	3200

The A1337 has a typical output bandwidth of 40 kHz (25 µs refresh rate) in high-RPM mode. In high-RPM mode, a new angle measurement is available at the internal angle output register to be transmitted over the SPI/SENT output ports every 25 µs. There is a latency of 60 µs from when there is a change in the position of the target magnet field to when the new representative angle is updated in the internal angle output register. This latency effectively represents the age of the angle measurement.

Impact of High-Speed Sensing

Due to signal path latency, the angle data is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e., a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm) and is referred to as angular lag.

The lag is directly proportional to rpm, and may be compensated for externally, if the velocity is known.

Angular lag can be expressed using:

Equation 1:

$$Angle_{Lag} = (rpm \times 6) / (1^6 \times t_{RESPONSE})$$

where rpm represents the rotational velocity of the magnet, $Angle_{Lag}$ is expressed in degrees, and $t_{RESPONSE}$ is in µs.

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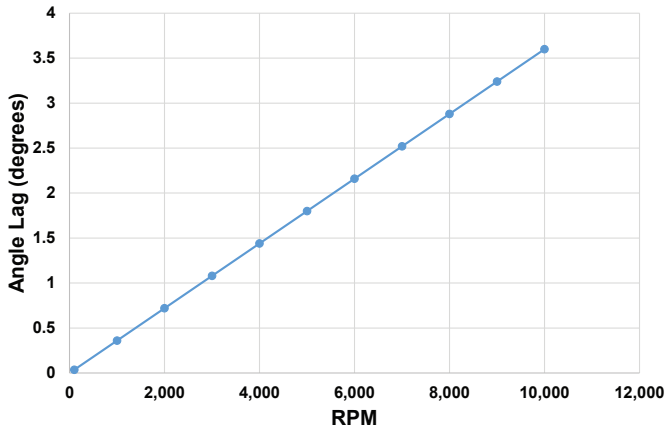

Figure 6: Angle Lag versus RPM, 60 µs Response Time

Angle Resolution and Representation

In addition to using the internal averaging of the sensor, angle resolution is also dependent on the intensity (B, in gauss) of the applied magnetic field from the target. At lower intensities, a reduced signal-to-noise ratio causes one or two LSBs to change state randomly due to noise. These factors work together:

- In high-RPM mode, the effective range of resolution is 8 to 10 bits (from lower to higher field intensities), dependent on field strength and AVG selection.
- In low-RPM mode, the effective range is 11 to 12 bits, dependent on field strength and AVG selection.

Regardless of the field intensity and mode selection, the transmission protocol and number formatting remains the same. The MSB is always transmitted first. The entire number should be read.

The output angle is always calculated at maximum resolution. To be more explicit, when reading the digital angle value:

Equation 2:

$$Angle_{OUT} = 360\ (°) \times D[12:0] / (2^{13})$$

This formula is always true, regardless of the applied field intensity. What changes with the field and speed setting is how "quiet" the LSBs of the measurement data (D 12:*x*) are.

It should be noted that the secondary die (E2) is rotated 180° relative to the primary die (E1). This results in a difference in measurement of approximately 180° between the two dies, given perfect alignment of each die to the target magnet.

This phenomenon can be counteracted by subtracting the offset using a microprocessor. Alternatively, compensation for the difference between the two dies can be made using the EEPROM for setting the reference angle.

Programing Modes

The EEPROM can be programmed through the dedicated SPI pins or via Manchester encoding on the VCC pin, which allows process coefficients to be entered and options to be selected.

NOTE: EEPROM programming also requires the VCC line to be pulsed, which could adversely affect other devices if powered from the same line. The EEPROM provides persistent storage of final parameters at the end of the line.

SPI System-Level Timing

The A1337 outputs a new angle measurement every t_{ANG} µs. In high-RPM mode, the A1337 outputs a new angle measurement every t_{ANG} µs, with an effective resolution of 10 bits. There is, however, a latency of t_{LAT}, from when the rotating magnet is sampled by the CVH to when the sampled data has been completely transmitted over the SPI interface. Because an SPI interface read command is not synchronous with the CVH timing, but is polled by the external host microcontroller, the latency can vary. For single back-to-back SPI transactions (where the first transaction is sending the read register 0x0 command and the second is retrieving the angle data), the following scenarios are possible:

- Worst case: 2 CVH cycles + 2 SPI cycles
- Best case: 1.5 SPI cycles; 2 µs, assuming a 10 MHz SPI clock

Power-Up

Upon applying power to the A1337, the device automatically runs through an initialization routine. The purpose of this initialization is to ensure that the device comes up in the same predictable operating condition every power cycle. This initialization routine takes a finite amount of time to complete, which is referred to as power-on time, t_{PO}.

The A1337 wakes up in a default state that sets all SPI registers to their default value. It is important to note that, regardless of the state of the device before a power cycle, the device repowers with the default values. For example, on every power-up, the device powers up in the mode set in the EEPROM bit RPM. The state of the EEPROM is unchanged.

Full-Power Mode

In full-power mode, the IC draws maximum current (nominally 8.25 mA; for more details, refer to the full-power mode supply current specification) to operate its full feature set, and updates the angle output register at the fastest rate, as selected by RPM mode and AVG settings (for more details, refer to the Programming Manual available on the Allegro software portal).

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Low-Power Mode

Low-power mode is useful for battery-powered applications where the task of tracking the target rotation can be delineated into one of two mission modes—The first mission mode is similar to an angle-tracking mode, where the sensor tracks the output at full bandwidth and provides its measure of the angular output at full resolution. The second mission mode can be considered as a turns-tracking mode. In this mode, the sensor does not need to track the angle at full resolution—It is sufficient to track the turns-count value of the target. The size of one turns-count unit can be preselected via EEPROM setting in the A1337 to be either 180 degrees or 45 degrees. The A1337 tracks ±1280 turns in both directions. In low-power mode, the A1337 is mostly held in a lower-quiescent-current consumption state. The IC does not provide typical angle readings over the SPI or SENT interfaces, but wakes up periodically to check for the occurrence of turns counts. The off-time of the low-power mode operation can be adjusted by the user based on the application, by programming on-chip EEPROM memory. Average I_{CC} in µA versus the programmable off-time t_{OFF} is shown in Figure 7.

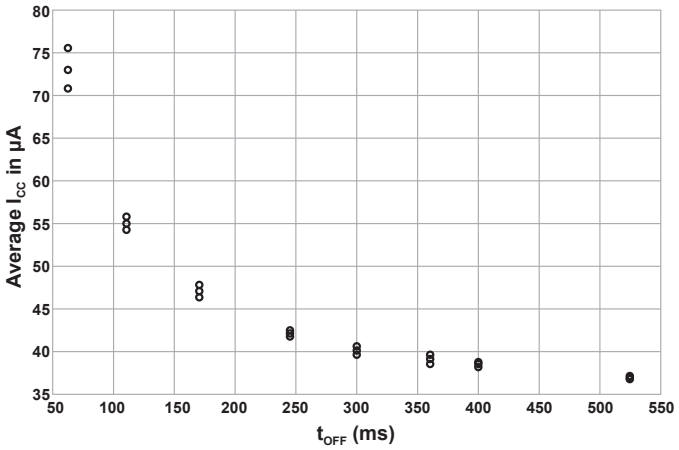

Figure 7: A1337 Average I_{CC} vs. t_{OFF}, Measured at 150°C

Transport Mode

Certain battery-powered applications require especially low power consumption from the IC during long-term storage and/or transportation (for example, when a new car is being transported from the assembly line to the dealer). To meet this need, the A1337 features an ultralow-power mode called transport mode. Transport mode is used to put the A1337 into a deep-sleep state for ultralow power consumption. When in this mode, the sensor IC does not track angle or turns counts. Typically, the IC consumes 30 µA of current per die when in transport mode.

WAKE Pin

The A1337 also offers a WAKE input pin. This pin is intended to wake up the device from low-power mode in special cases where the motor acceleration is too high and the system cannot afford to wait for the entire low-power sleep time to expire before the next periodic wakeup. When the voltage threshold on the WAKE pin exceeds $V_{WAKE(HITH)}$, the IC wakes up from low-power mode and begins to track turns as it would in full-power mode. This pin is usually connected to a filtered version of the back-EMF voltage signal from the motor being used. This allows fast feedback from the motor to the turns-count circuit in the case of high-acceleration events.

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Transitioning Between Modes

The A1337 is designed so that it can transition between full-power mode (FPM), low-power mode (LPM), and transport mode (TM) based on either a command from the system microcontroller, by magnetic target rotation, or by exceeding the WAKE pin threshold, $V_{WAKE(HITH)}$. This dual scheme ensures that valuable turns-count (TC) data is not lost due to the target rotating too quickly while the sensor is in low-power mode.

To better understand this, consider a few scenarios based on the state diagram shown in Figure 8, as well as the information shown in Table 2. If the sensor is powered up and in FPM, it is able to provide all the functionality described under the FPM column in Table 2. If the controller then determines that, to save power, it should enter LPM, all the conditions outlined in branch A of Figure 8 must be satisfied before it can enter LPM. In other words, the A1337 SPI lines must be held low for >50 µs, the WAKE pin voltage on the A1337 IC must be lower than the threshold $V_{WAKE(LOTH)}$, and the target rpm of the magnet must be lower than an average speed $S_{AWAKE(TH)}$. If all these conditions are met, the IC transitions into LPM. While in LPM, the IC is able to support the TC tracking functionality described in Table 2.

If the system needs to wake up from LPM and reenter FPM, it must then satisfy any one of the conditions outlined in branch B of Figure 8—in other words, it must initiate activity on the SPI pins, rotate the target faster than $S_{AWAKE(TH)}$, or apply a voltage higher than $V_{WAKE(LOTH)}$ on the WAKE pin.

In a similar manner, the system can navigate between FPM, LPM, and TM, by meeting the appropriate conditions specified by branches A, B, C, or D of the state diagram.

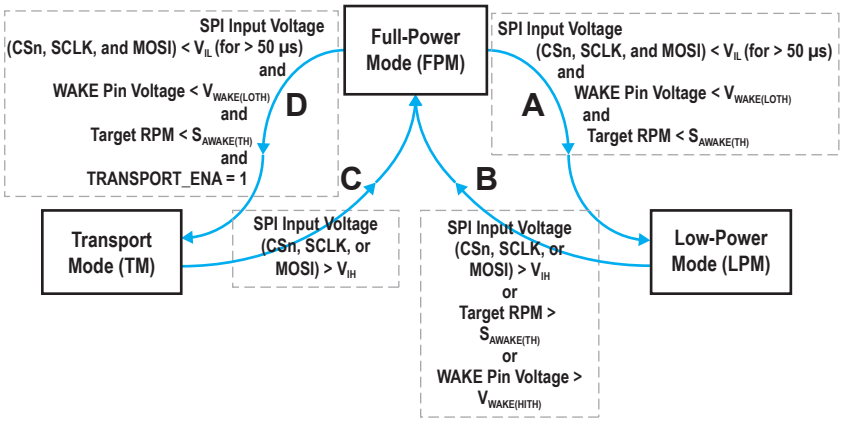

Figure 8: Operating Mode State Diagram

Table 2: Mode States

	Full-Power Mode (FPM)	Low-Power Mode (LPM)	Transport Mode (TM)
Angle Sensor Functionality	Available communication protocols: • **SPI 4-wire** • **SENT** • **Manchester code**	Available communication protocols: • **Not applicable**	Available communication protocols: • **Not applicable**
	Available angle output data: • **12-bit absolute angle value** • **Turns-count (TC)**	Available angle output data: • **Turns-count (TC)** [1]	Available angle output data: • **Not applicable**
Current Consumption	8.5 mA nominal per die	55 µA nominal per die **100× power savings**	30 µA nominal per die **280× power savings**

[1] During LPM, TC values are tracked. Upon exiting LPM, TC values become read-only.

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User-Programmable Features for Low-Power Mode and Turns Counting

The A1337 allows programmability of its LPM function. For instance, the IC provides the ability to select the size of its turns-count. Two choices are available: 180° or 45°. This feature is selectable via the TC1 bit in EEPROM address 0x15, bit 18. In a similar manner, other functions of the LPM operation can also be programmed in EEPROM. These features and the default values are summarized in Table 3.

Table 3: User-Programmable Features

Field	EEPROM Address	Size (bits)	Default [1] (Binary, Decimal)	Value	Function
TC1	0x15, bit 18	1	$(0)_2$	0	180-degree turns-count.
				1	45-degree turns-count.
LOW_POWER_OFF_TIMER	0x15, bit 17:10	8	$(00110000)_2$, $(48)_{10}$	–	Sets LPM off-time from ~2 ms to ~500 ms, in 2 ms steps.
NORMAL_POWER_SPEED_TIMER	0x15, bit 9:0	9	$(0010011101)_2$, $(157)_{10}$	–	Sets the time interval over which the angular velocity of the target is measured. To ensure proper operation as specified in the datasheet, the default value is the recommended setting for this parameter.
NORMAL_POWER_ANGLE_THRESHOLD	0x16, bit 22:12	11	$(00000011010)_2$, $(26)_{10}$	–	Sets the maximum allowable angle displacement over the time set by NP_SPEED_TIMER. To ensure proper operation as specified in the datasheet, the default value is the recommended setting for this parameter.
LOW_POWER_ANGLE_THRESHOLD	0x16, bit 10:0	11	$(01010101010)_2$, $(682)_{10}$	–	Sets the maximum allowable angle displacement over the time set by LP_OFF_TIMER. To ensure proper operation as specified in the datasheet, the default value is the recommended setting for this parameter.

[1] Default values for LP_OFF_TIMER, NP_SPEED_TIMER, NP_ANGLE_THRESHOLD, and LP_ANGLE_THRESHOLD are for angular motion with constant acceleration (max acceleration 6000°/s^2) and t_{OFF} = 98 ms.

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MANCHESTER SERIAL INTERFACE

To facilitate addressable device programming when using the unidirectional SENT output mode with no need for additional wiring, the A1337 incorporates a serial interface on the VCC line.

NOTE: The A1337 may be programmed via the SPI interface, with additional wiring connections. For detailed information about part programming, refer to the A1337 Programming Manual available on the Allegro software portal.

This interface allows an external controller to read and write registers in the A1337 EEPROM and volatile memory. The device uses a point-to-point communication protocol, based on Manchester encoding per G.E. Thomas (a rising edge indicates a 0 and a falling edge indicates a 1), with address and data transmitted MSB first. The addressable Manchester code implementation uses the logic states of the SA0 (SPI $\overline{CS}$ pin)/SA1 (SPI SCLK pin) to set address values for each die. In this way, individual communication with up to four A1337 dies is possible.

To prevent any undesired programming of the A1337, the serial interface can be disabled by setting the disable Manchester bit (0x19, bit 18) to a 1. With this bit set, the A1337 ignores any Manchester input on VCC.

Entering Manchester Communication Mode

Provided the disable Manchester bit is not set in EEPROM, the A1337 continuously monitors the VCC line for valid Manchester commands. The part takes no action until a valid Manchester access code is received.

There are two special Manchester code commands used to activate or deactivate the serial interface and specify the output format used during read operations:

1. **Manchester Access Code:** Enters Manchester communication mode; Manchester code output on the SENT pin.
2. **Manchester Exit Code:** Returns the SENT pin to typical (angle data) output format.

Once the Manchester communication mode is entered, the SENT output pin ceases to provide angle data, which interrupts any data transmission in progress.

Transaction Types

The A1337 receives all commands via the VCC pin and responds to read commands via the SENT pin, as shown in Figure 9.This implementation of Manchester encoding requires the communication pulses to be within a high ($V_{MAN(H)}$) and low ($V_{MAN(L)}$) range of voltages on the VCC line. Writing to EEPROM is supported by two high-voltage pulses on the VCC line.

Each transaction is initiated by a command from the controller; the A1337 does not initiate any transactions. Two commands are recognized by the A1337: write and read.

Writing to EEPROM

When a write command requires writing to nonvolatile EEPROM, after the write command, the controller must also send two programming pulses—high-voltage strobes—via the VCC pin. These strobes are detected internally, allowing the A1337 to boost the voltage on the EEPROM gates. For specific details about sensor programming and protocols, refer to the Programming Manual available on the Allegro software portal.

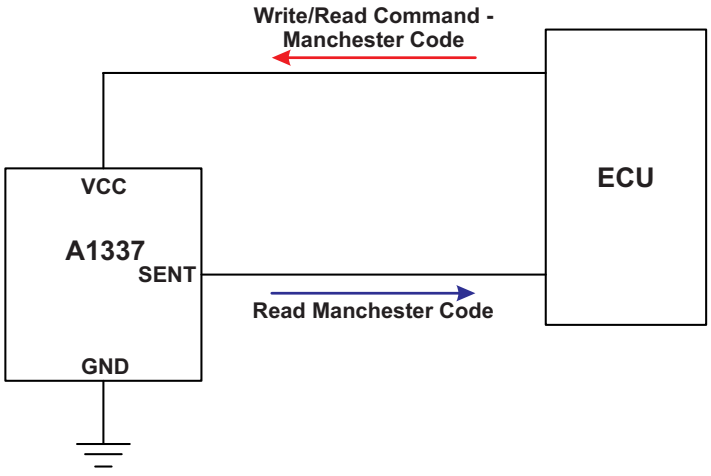

Figure 9: Top-Level Programming Interface

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Manchester Interface Reference

Table 4: Manchester Interface Protocol Characteristics [1]

Characteristics	Symbol	Note	Min.	Typ.	Max.	Unit
INPUT/OUTPUT SIGNAL TIMING						
Bit Rate		Defined by the input message bit rate sent from the external controller	4	–	50	kbps
Bit Time	t_{BIT}	Data bit pulse width at 4 kbps	243	250	257	µs
		Data bit pulse width at 100 kbps	9.5	10	10.5	µs
Bit Time Error	err_{TBIT}	Deviation in t_{BIT} during one command frame	–11	–	+11	%
Write Delay	$t_{WRITE(E)}$	Required delay from the end of the second EEPROM program pulse to the leading edge of a following command frame	V_{CC} < 6.0 V	–	–	–
Read Delay	t_{START_READ}	Delay from the trailing edge of a read command frame to the leading edge of the read acknowledge frame	¼ × t_{bit}	–	¾ × t_{bit}	µs
EEPROM PROGRAMMING PULSE						
EEPROM Programming Pulse Setup Time	$t_{sPULSE(E)}$	Delay from last bit cell of write command to start of EEPROM programming pulse	40	–	–	µs
Pulse High Time	$t_{PULSE(H)}$	Time above minimum pulse voltage	8	10	11	ms
Rise Time	t_r	10% to 90% of minimum pulse level	300	–	–	µs
Fall Time	t_f	10% to 90% of minimum pulse level	60	–	–	µs
Pulse Voltage	V_{PULSE}	Applied on VCC Line	18	19	19.5	V
Separation Time	$t_{PULSE(f-r)}$	Timing between first pulse dropping below 6 V and second pulse rising above 6 V	0.002	–	50	ms
INPUT SIGNAL VOLTAGE						
Manchester Code High Voltage	$V_{MAN(H)}$	Applied to VCC line	7.8	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	Applied to VCC line	–	–	6.3	V
OUTPUT SIGNAL VOLTAGE (Applied on SENT Line)						
Manchester Code High Voltage	$V_{MAN(H)}$	Minimum R_{pullup} = 5 kΩ	0.9 × V_S	–	–	V
		Maximum R_{pullup} = 50 kΩ	0.7 × V_S	–	–	V
Manchester Code Low Voltage	$V_{MAN(L)}$	5 kΩ ≤ R_{pullup} ≤ 50 kΩ	–	–	0.2	V

[1] Determined by design.

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SENT Output Mode

(A1337LLETR-DD-T, A1337LLETR-T options)

The SENT output converts the measured magnetic field angle to a binary value mapped to the full-scale output (FSO) range of 0 to 4095, shown in Figure 10. This data is inserted into a binary pulse message, referred to as a frame, that conforms to the SENT data transmission specification (SAE J2716 JAN2010).

The SENT frame may be configured via EEPROM. The A1337 may operate in one of three broadly defined SENT modes (for details on SENT modes and settings, see the A1337/8 Programming Manual).

- SAE J2716 SENT: Free-streaming SENT frame in accordance with industry specification.
- Triggered SENT (TSENT): User-defined sampling and retrieval.
- Shared SENT: Allows multiple devices to share a common SENT line. Devices may either be directly addressed (addressable SENT or ASENT) or sequentially polled (sequential SENT or SSENT).

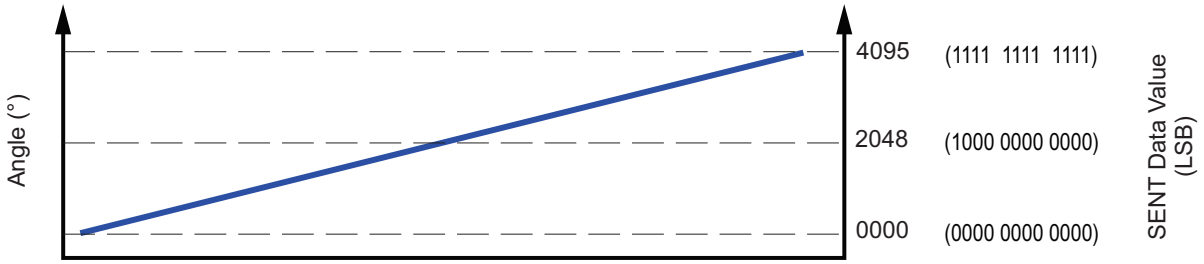

Figure 10: Angle is Represented as a 12-Bit Digital Value

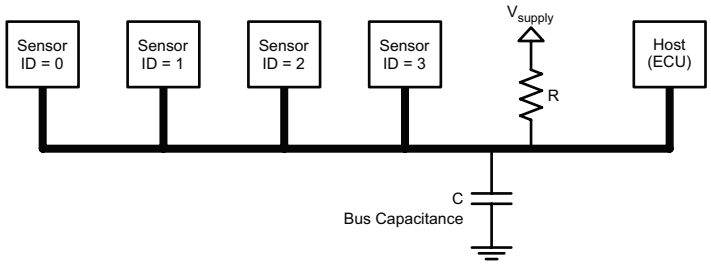

Figure 11: Allegro-Proprietary SENT Protocol Allows Multiple Parts to Share One Common Output Bus

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SENT MESSAGE STRUCTURE

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at 5 ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the falling edge may be adjusted using the C_SENT_DRIVE parameter.

The duration of a nibble is denominated in ticks. The period of a tick is set by the C_TICK_TIME parameter. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence (see Figure 13):

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides A1337 status and the optional serial data determined by the setting of the SENT_SERIAL parameter.
3. **Data:** Angle data and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

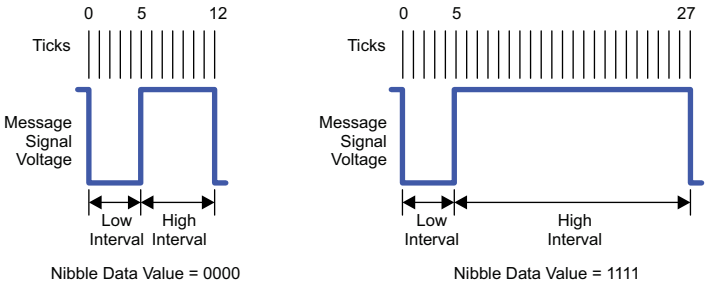

Figure 12: General Value Formation for SENT

0000 (left), 1111 (right)

Table 5: Nibble Composition and Value

Quantity of Ticks			Binary (4-Bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0002	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

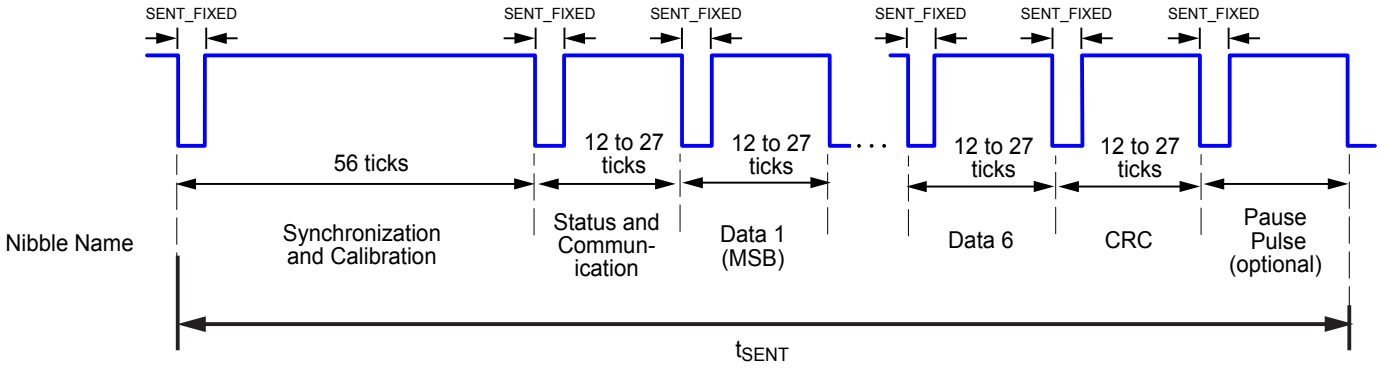

Figure 13: General Format for SENT Message Frame

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Table 6: EEPROM Registers Map (Factory Reserved Registers Not Shown)

EADR	State	Bits																							
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x15	LP_CFG1	RES					TC1	LOW_POWER_OFF_TIMER								NORMAL_POWER_SPEED_TIMER									
0x16	LP_CFG2	RES	NORMAL_POWER_ANGLE_THRESHOLD											RES	LOW_POWER_ANGLE_THRESHOLD										
0x17	SENT_CFG	ZS	SS	SM	PO	IS	RES	SCN_MODE			DATA_MODE			SENT_MODE		TICK_TIME							SENT_DRIVE		
0x18	CUST_CFG1	RES			CIS	DA	MAXID		NS	FA	U_INIT_ST		PW_UP_ST	MISSING_MAG_THRESHOLD											
0x19	CUST_CFG2	LOCK	RES				MAND	SCRC	RPMD	AVERAGE			POL	ANGLE_OFFSET											
0x1E	ERM	RES									MAN2	MAN	UV	LBST	CVHST	GOVF	AH	AL	EU	ES	TR	TRNO	IE	MAGM	BATD
0x1F	CUST2	CUST_EEP																							

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Diagnostics

The A1337 was designed with ISO 26262 requirements in mind and supports a number of on-chip self diagnostics to enable the host microcontroller to assess the operational status of each die. For example, each die can be user-configured for logic built-in self-test (LBIST) evaluation to ensure the digital circuits are operational. Upon completion of an LBIST operation, the A1337 sets a pass/fail LBIST status flag in the device error (ERR) register.

Each A1337 die also supports several diagnostic features and status flags, accessible via a SPI read of the ERR register, to let the user know if any issues are present with the A1337 or associated magnetic system, as shown in Table 7.

In addition, each die on the A1337 supports an on-chip user-initiated diagnostic (CVH self-test) mode that tests the entire signal path, including the front end CVH sensing circuitry.

USER-INITIATED DIAGNOSTICS

Each die on the A1337 can be independently controlled by a microcontroller to enter its CVH self-test mode via SPI or SENT.

When a CVH self-test mode operation is requested by the microcontroller, the respective die initiates a test mode sequence whereby it sequentially applies an internal constant bias current to every contact element in the CVH ring. As each element in the CVH ring is sequentially biased, an angle measurement is calculated.

The time to complete one revolution around the CVH ring and calculate and store incremental angle measurements is t_{CVHST}.

Table 7: Diagnostic Capabilities

Diagnostic/ Protection	Description	Output State
Loss of V_{CC}	Determine if battery power was lost.	BATD error flag is set; see the ERR (Error) Register section.
Reverse V_{CC} Condition	Current limiting (VCCx pin).	Output below GND.
MISO/SENT Short to VCC	Current limiting (MISOx pin).	MISO/SENT line: Pulled up to V_{pullup}. Should not be tied to VCC if V_{CC} > 5.5 V.
MISO/SENT Short to Ground	Current limiting (MISOx pin).	MISO/SENT line: Pulled up to GND.
Logic Built-In Self-Test (LBIST)	70% coverage for 10 ms BIST of all digital circuitry.	Error flags set in SPI message when errors are detected; see the ERR2 (Error2) Register section.
Signal Path Diagnostics	User-controlled advanced CVH and full signal path diagnostics.	Error flags set in SPI message when errors are detected; see the ERR2 (Error2) Register section.
Internal Error	Monitors digital logic for proper function.	IERR error flag is set; see the ERR (Error) Register section.
Missing Magnet	Monitors magnet field level in case of mechanical failure.	MAGM error flag is set; see the ERR (Error) Register section.
EEPROM Error Detection and Correction	Detection of single- and dual-bit error, and correction of single-bit error.	Error flags set in SPI message when errors are detected or corrected; see the ERR (Error) Register section.
V_{CC} Low Flag	Asserted when $V_{CC} < V_{UVLOTH}$.	Bit 2 of SPI output on MISO is set high. For more details, see the Programming Manual.
Temperature Out of Range	Die temperature has exceeded acceptable range.	For more details, see the ERR (Error) Register section.
Redundancy	Dual-die version of the A1337 provides redundant sensors in the same package.	

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SERIAL INTERFACE STRUCTURE

The serial interface contains the primary serial interface (PSI) registers and the restricted extended addressing registers. The PSI fields are used by the host for routine communication with the A1337, such as retrieving current angle, turns-count, error, and status data, and managing certain configuration settings. For information on extended addressing and EEPROM access, see the A1337 Programming Manual available on the Allegro software portal.

Table 8: Primary Serial Interface Registers (Reserved Registers Not Shown)

Address (Hex)	Name (Symbol)	Usage
0x00	Angle Output (ANG)	Read out current angle (Note: 12-bit angle output located MSB first, in bits12:1; bit 0 is always 0)
0x02	Turns Count (TRN)	Read out current turns count (A1337 only); bits 11:0
0x04	Error (ERR1)	Read out error flags
0x05	Error (ERR2)	Read out error flags
0x08	Control (CTRL)	Read or write configuration commands
0x0F	Key Code (KEY)	Write the key code to enable access to extended addressing registers

Table 9: Primary Serial Interface Registers Bits Map (Reserved Registers Not Shown)

Serial Address	Register Symbol	Addressed Byte (MSB)												
		12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	ANG	ANGLE OUTPUT (12:1)												0
0x02	TRN	–	TURNS_COUNT											
0x04	ERR	–	–	–	–	–	–	EEP2	EEP1	TMP	TRNO	IERR	MAGM	BATD
0X05	ERR2	–	–	–	–	–	–	MANER	RES3	LBIST	CVHST	RES2	RES1	RES0
0x08	CTRL	–	–	–	–	–	–	–	–	STS	TRST	RPM	TEN	ERST
0x0F	KEY	–	–	–	–	–	KEY_CODE							

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ANG (Angle Output) Register
Address: 0x00

Address	0x00												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUTPUT												–
R/W	R	R	R	R	R	R	R	R	R	R	R	R	R
Value	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0

Stores data on current angle reading.

ANGLE_OUTPUT [12:1] Current Angle

Most recent angle reading. Value is unsigned, stored in bits 12:1 (bit 0 defaults to 0). As the target turns, the angle value increases or decreases according to the rotational polarity setting in EEPROM (CUST_CFG2 register, POL bit).

Bit	Value	Description
12:1	0/1	Current angle reading.

TRN (Turns Count) Register
Address: 0x02

Address	0x02												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	TURNS_COUNT											
R/W	–	R	R	R	R	R	R	R	R	R	R	R	R
Value	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0

Stores data on cumulative target full turns count.

TURNS_COUNT [11:0] Cumulative Turns Count

Most recent net accumulated turns count. A turn is counted at each crossing of: the zero-angle and 180-degree points, or the zero-angle and incremental 45-degree points. As the target turns, the count value increases or decreases according to the rotational polarity setting in EEPROM (CUST_CFG register, POL bit). Turns-count threshold can be set to either 45 degrees or 180 degrees, based on the setting of EEP 0x15, bit 18 (TC1, 1 = 45 degrees, 0 = 180 degrees).

Bit	Value	Angle Value (Absolute Degrees)		Description	
11:0	0/1	EEP 0x15, Bit 18, (TC1) = 0	EEP 0x15, Bit 18, (TC1) = 1	Two's complement current turns count, for example:	
				Turns Count	Field Bits Value
		0	0	0	0000 0000 0000
		180	45	+1	0000 0000 0001
		230400	57600	+1280	0101 0000 0000
		–180	–45	–1	1111 1111 1111
		–230400	–57600	–1280	1011 0000 0000

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ERR (Error) Register

Address: 0x04

Address	0x04												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	EEP2	EEP1	TMP	TRNO	IERR	MAGM	BATD
R/W	–	–	–	–	–	–	R	R	R	R	R	R	R
Value	X	X	X	X	X	X	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1

Error register. Indicates various current error conditions. When set, can only be cleared via the CTRL register ERST field, hard reset, or power-on reset (see BATD for exception). If any of the error bits are asserted, the error flag on the serial interface becomes asserted. Masking an error bit prevents the bit from asserting the serial interface error flag, but the error bit may still become asserted in this register.

EEP2 [6] EEPROM Error Flag 2

Uncorrectable dual-bit EEPROM error flag.

Bit	Value	Description
6	0	Error condition not present.
	1	Error condition present.

EEP1 [5] EEPROM Error Flag 1

Corrected single-bit EEPROM error flag.

Bit	Value	Description
5	0	Error condition not present.
	1	Error condition present.

TMP [4] Temperature Out of Range

This bit indicates an error condition when the die temperature has exceeded the acceptable range.

Bit	Value	Description
4	0	Error condition not present.
	1	Error condition present.

TRNO [3] Turns-Count Data Overflow

Indicates an overflow in the turns-count output data.

Bit	Value	Description
3	0	Error condition not present.
	1	Error condition present.

IERR [2] Internal Error

This bit is set to 1 if an internal logic error condition has been detected. When this bit is set to 1, a general reset is recommended.

Bit	Value	Description
2	0	No digital logic timer error has been detected.
	1	Digital logic timer error has been detected.

MAGM [1] Target Magnet Loss

Monitors target magnet field level to detect field loss due to mechanical failure in the application. Missing magnet field threshold can be customer programmed by writing to EEPROM address 0x18, bits 10:0 (MISSING_MAG_THRESHOLD). Allegro programs this to a default value of 100 G, but the customer can readjust this field if desired.

Bit	Value	Description
1	0	Error condition not present.
	1	Error condition present.

BATD [0] Power Supply Loss

Indicates if battery power (VCC supply) was lost. By default, also indicates at expected low-power events: start-up, power-on reset, and after exiting transport mode. Before commencing full-power operation, must be set to 0 by asserting the ERST bit of the CTRL register (unless field is masked in EEPROM by ERM register BATD field).

Bit	Value	Description
0	0	Error condition not present.
	1	Error condition present.

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ERR2 (Error2) Register

Address: 0x05

Address	0x05												
Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	MANER	RES3	LBIST	CVHST	RES2	RES1	RES0
R/W	–	–	–	–	–	–	R	–	R	R	–	R	R
Value	X	X	X	X	X	X	0/1	–	0/1	0/1	–	0/1	0/1
Reset	0	0	0	0	0	0	0	–	0	0	–	0	1

Error register. Indicates various current error conditions. When set, can only be cleared via the CTRL register ERST field, hard reset, or power-on reset (see BATD for exception). If any of the error bits are asserted, the error flag on the serial interface becomes asserted. Masking an error bit prevents the bit from asserting the serial interface error flag, but the error bit may still become asserted in this register.

MANER [6] Manchester/SENT Error Flag

Indicates Manchester/SENT Error.

Bit	Value	Description
6	0	Error condition not present.
	1	Error condition present.

RES3 [5] Factory Reserved Bit

LBIST [4] LBIST Error Flag

This bit indicates that the logic built-in self-test (LBIST) failed.

Bit	Value	Description
4	0	Error condition not present.
	1	Error condition present.

CVHST [3] Circular Vertical Hall Self-Test

This bit indicates that the CVH built-in self-test (CVHST) failed.

Bit	Value	Description
3	0	Error condition not present.
	1	Error condition present.

RES2 [2] Factory Reserved Bit

RES1 [1] Factory Reserved Bit

RES0 [0] Factory Reserved Bit

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CTRL (Control) Register

Address: 0x08

Address	0x08							
Bit	7	6	5	4	3	2	1	0
Name	–	–	–	STST	TRST	RPM	TEN	ERST
R/W	–	–	–	RW1C	RW1C	R/W	R/W	RW1C
Value	X	X	X	X	0/1	0/1	0/1	0/1
Reset	0	0	0	0	0	0	0	0

Initialization and operation configuration control command settings.
RW1C: When a 1 is written to the field, the command is immediately executed, and the value returns to zero. When reading the field, this type of field always reads back 0.

STS [4] Self-Test Start

Commands the A1337 to begin Self-Test(s).

Which self-test is run, is determined by the U_INIT_ST field within EEPROM. There are two self-tests:

- Logic Built-In Self-Test (LBIST): Verifies digital gate integrity. This is a modified version of digital scan testing. Requires approximately 10 ms to run, during which time no angle readings can occur.
- CVH Self-Test: Test of the front-end transducer and signal path. Requires approximately 40 ms to complete, during which time angle readings are not available.

Bit	Value	Description
4	0	Does not trigger self-test.
	1	Self-test is triggered based on preselected options in the U_INIT_ST field of EEPROM.

TRST [3] Turns Count Reset

Commands the A1337 to clear the value in the TRN register (0x02).

Bit	Value	Description
3	0	Turns counter reset.
	1	Turns counter not reset.

RPM [2] RPM Operating Mode (see Programming Manual)

This field is populated on power-up by the EEPROM field RPMD. This field can be written during operation to temporarily override the EEPROM. On the next power cycle, this field resets to the value determined by the EEPROM field RPMD. To enable internal averaging, this bit must be a 1.

Bit	Value	Description
2	0	Internal Averaging not allowed.
	1	Internal Averaging allowed.

TEN [1] Low Power Mode Select

Determines operational mode at power-on reset. Determines whether device enters the standard low-power mode or the transport mode on the next low-power-cycle request.

Bit	Value	Description
1	0	Low Power Mode.
	1	Transport Mode.

ERST [0] Error Flags Reset

A feature to clear the values in the ERR register (0x04).

Bit	Value	Description
0	0	ERR register not cleared.
	1	ERR register cleared.

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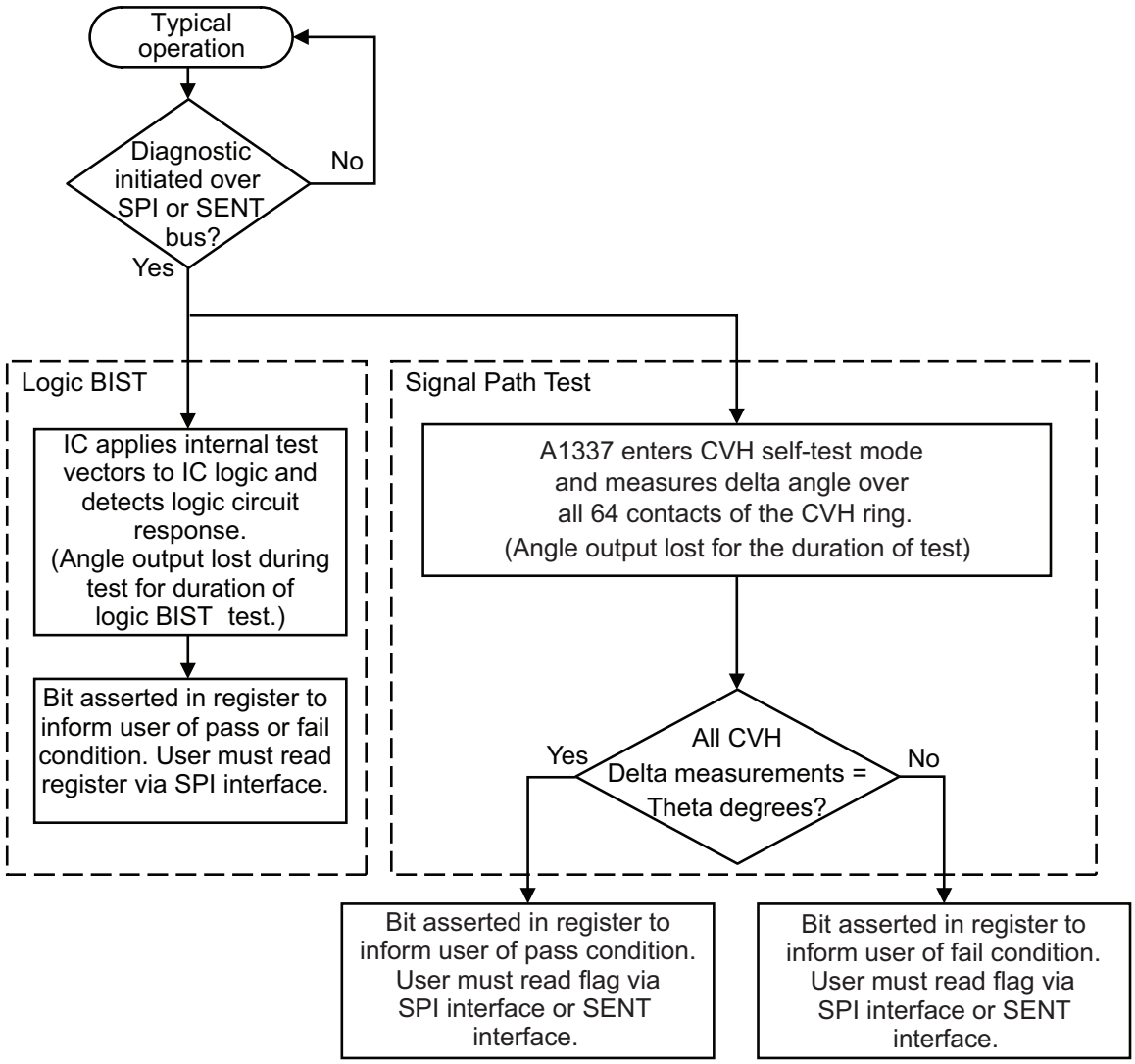

Figure 14: User-Interface Diagnostic Diagram

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APPLICATION INFORMATION

Serial Interface Description

The A1337 features SPI and SENT interfaces. The following figures show some typical application circuits for using the A1337 with these interfaces.

Calculating Target Zero-Degree Angle

When shipped from the factory, the default angle value when oriented as shown in Figure 15, is approximately 21° (201° on the second die). In some cases, the end user may want to program an angle offset in the A1337 to compensate for variation in magnetic assemblies or for applications that require absolute system-level readings.

The internal algorithm for computing the output angle is:

Equation 3:

$$Angle_{OUT} = Angle_{RAW} - Reference\ Angle\ .$$

The procedure to "zero out" the A1337 is quite simple. During final application calibration and programming, position the magnet above the A1337 in the required zero-degree position, and read the angle from the A1337 using the SPI interface ($Angle_{OUT}$). From this angle, the reference angle required to program the A1337 can be computed as:

Equation 4:

$$Reference\ Angle = Angle_{OUT}\ .$$

Bypass Pins Usage

The bypass pins are required for proper operation of the device. A 0.1 µF capacitor should be placed in very close proximity to each of the bypass pins.

When using the SPI communication protocol, the A1337 has the ability to support host microcontroller inputs with voltage input high (V_{IH}) thresholds of 2 V (minimum). This option only requires BYP1 to be populated with a 0.1 µF capacitor.

By using an optional second bypass capacitor on the BYP2 pins, the A1337 can also support host microcontroller inputs with voltage input high (V_{IH}) thresholds of 2.5 V (minimum). This option requires that both the BYP1 pin and the BYP2 pin be populated with 0.1 µF capacitors, and that the appropriate EEPROM con-

Target alignment for default angle setting
- Target rotation axis intersects primary die
  - Sets primary die 21° default point
  - Sets secondary die 201° default point

(Example shows element E1 as primary die and element E2 as secondary die)

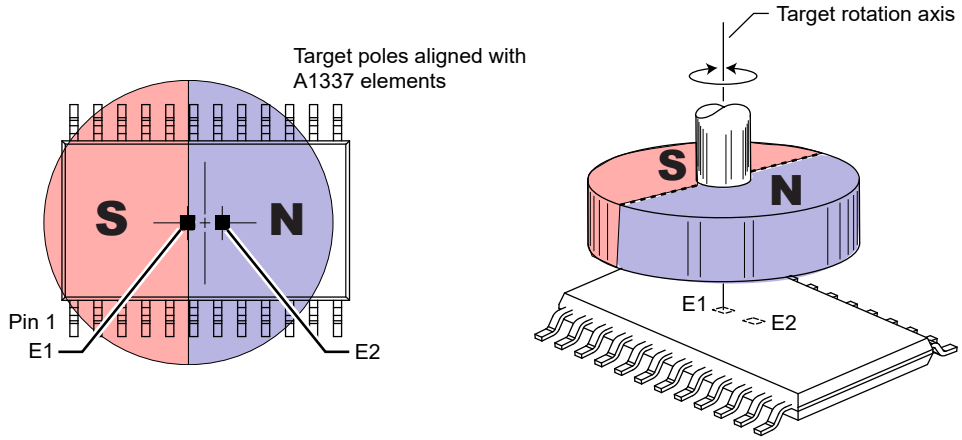

Figure 15: Orientation of Magnet Relative to Primary and Secondary Die

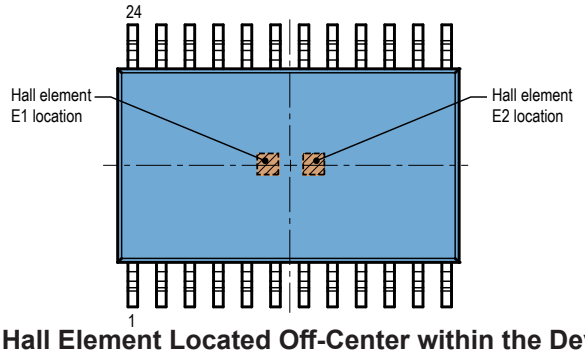

Figure 16: Hall Element Located Off-Center within the Device Body

(For reference dimensions, refer to the Package Outline Drawing.)

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figuration bit be enabled. For availability of parts with elevated SPI output levels, contact Allegro.

The bypass pins are not intended to be used to source external components. To assist with PCB layout, see the Operating Characteristics table for output voltage and current requirements.

Changing Sampling Modes

The A1337 features a high -RPM sampling mode and a low-RPM sampling mode. The default power-on state of the A1337 is loaded from EEPROM. To configure the A1337 to low-RPM mode, set the operating mode to low-RPM mode by writing a logic 1 to bit 2 (RPM) of the configuration commands (CTRL) register, via the SPI interface.

Magnetic Target Requirements

The A1337 is designed to operate with magnets constructed with a variety of magnetic materials, cylindrical geometries, and field strengths, as shown in Table 10. For more detailed information about magnet selection and theoretical error, contact Allegro.

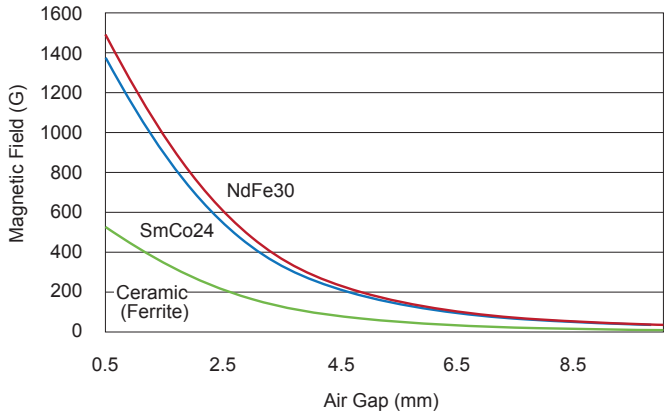
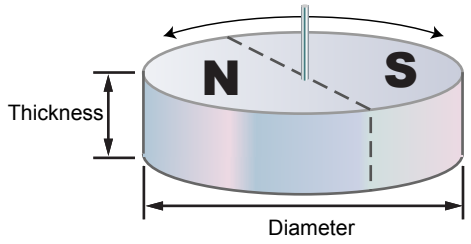


Figure 17: Magnetic Field versus Air Gap
For a magnet 6 mm in diameter and 2.5 mm thick

Allegro can provide similar curves for customer application magnets upon request. Larger magnets are recommended for applications that require optimized accuracy performance.

Table 10: Target Magnet Parameters

Magnetic Material	Diameter (mm)	Thickness (mm)
Neodymium (bonded)	15	4
Neodymium (sintered) [1]	10	2.5
Neodymium (sintered)	8	3
Neodymium / SmCo	6	2.5



[1] A sintered neodymium magnet with 10 mm (or greater) diameter and 2.5 mm thickness is the recommended magnet for redundant applications.

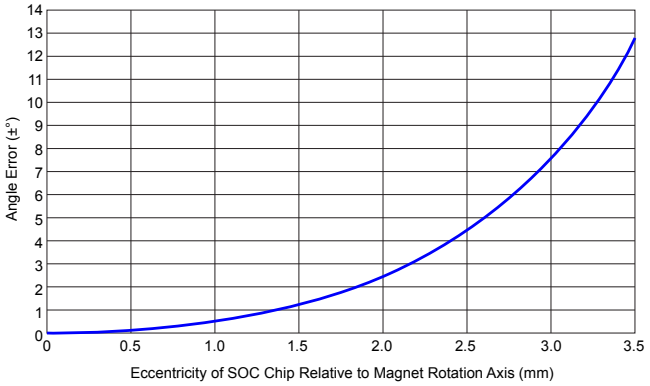


Figure 18: Angle Error versus Eccentricity

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Redundant Applications and Alignment Error

The A1337 is designed to be used in redundant, on-axis applications with a single magnet spinning over the two separate dies that are mounted side-by-side in the same package. One challenge with this configuration is correctly aligning the magnet with the device package, so it is important to be aware of the physical separation of the two dies.

The behavior of alignment error when using a Ø10 mm × 2.5 mm neodymium magnet located 2.7 mm above the branded face of the package is illustrated in Figure 19. The curve shows the relationship between absolute angle error present on the output of the die versus eccentricity of the die relative to the rotation axis of the magnet. The curve is the same for both dies in the package.

The curve provides guidance to determine what the optimal magnet placement should be for a given application. For example, given that the maximum spacing between the two dies is 1 mm, if the center of the magnet rotation is placed at the midpoint between the two dies, each die will have a maximum eccentricity of 0.5 mm.

For applications with reduced accuracy requirements, considering one die the primary and the other die the secondary, the magnet axis of rotation could be positioned directly above the primary die, and thus offset 1 mm from the secondary die, yielding zero alignment error on the primary die, and approximately ±1° of error on the secondary die, relative to the primary die, due to geometric mismatch.

System Timing and Error

The A1337 is a digital system and therefore takes angle samples at a fixed sampling rate. When using a sensing device with a fixed sampling rate to sample a continuously moving target, there will be error introduced that can be simply calculated with the sampling rate of the device and the speed at which the magnetic signal is changing. In the case of the A1337, the input signal is rotating at various speeds, and the sampling rate of the A1337 is fixed at ANG. The calculation would be:

Equation 5:

$$ANG\ (\mu s) \times angular\ velocity\ (^\circ/\mu s)\ .$$

So, the faster the magnetic object spins, the further behind in angle the output signal seems for a fixed sampling rate.

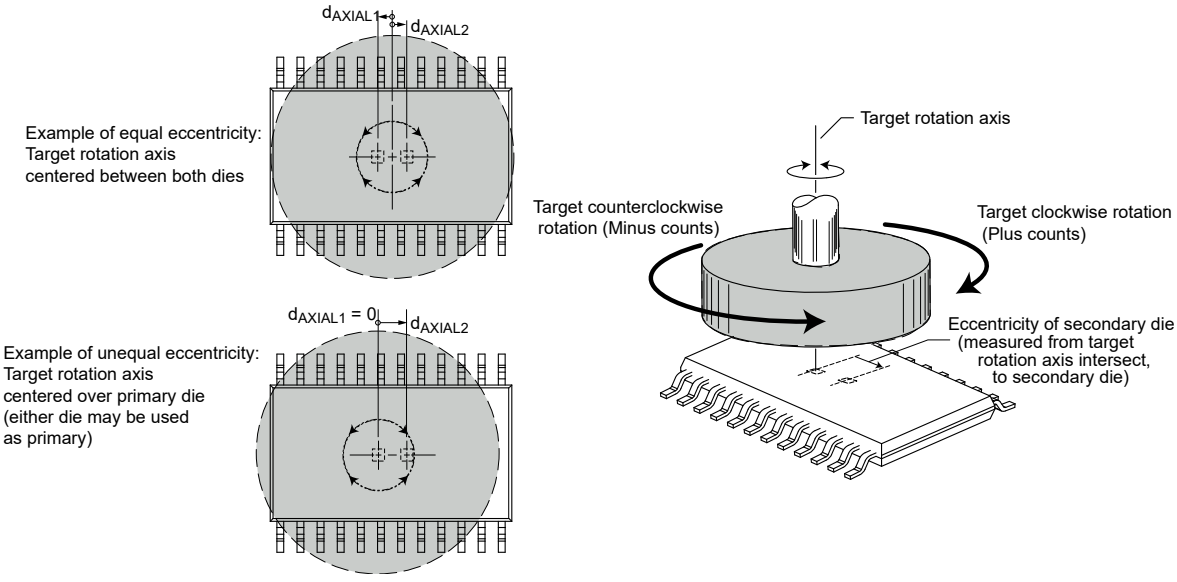

Figure 19: Demonstration of Magnet to Sensing Element Eccentricity

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CHARACTERISTIC PERFORMANCE DATA

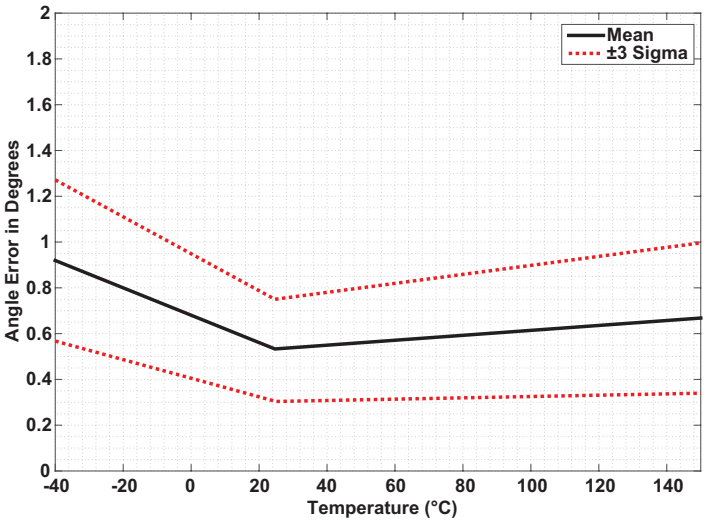

Figure 20: Angle Error over Temperature (300 G)

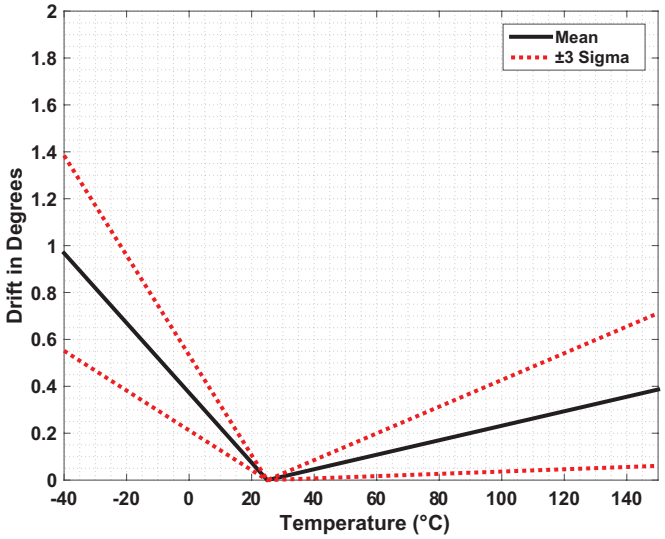

Figure 21: Angle Drift Relative to 25°C (300 G)

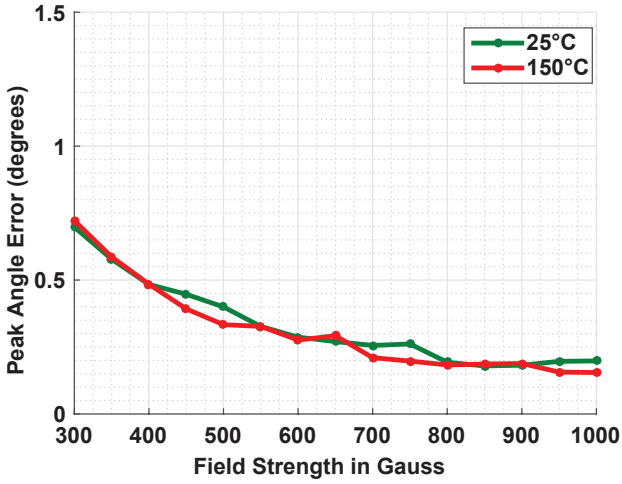

Figure 22: Angle Error over Field Strength

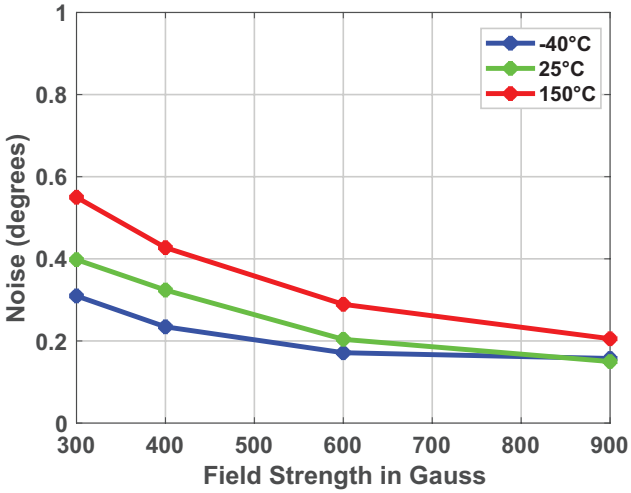

Figure 23: Typical Three-Sigma Angle Noise Over Field Strength

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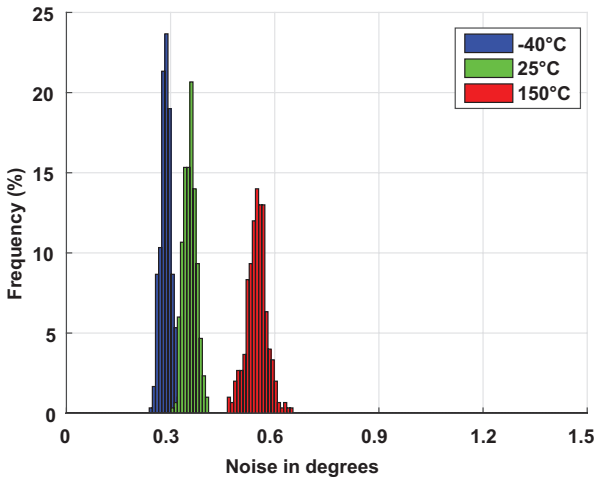

Figure 24: Noise Distribution over Temperature (3 σ, 300 G)

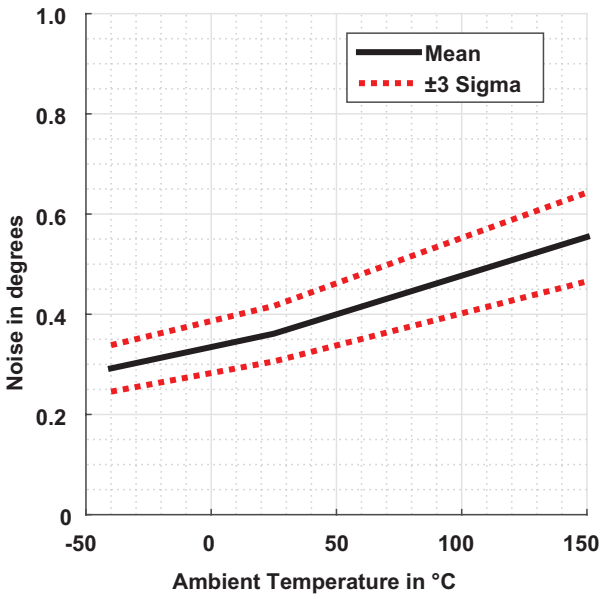

Figure 25: Noise Performance over Temperature (3 σ, 300 G)

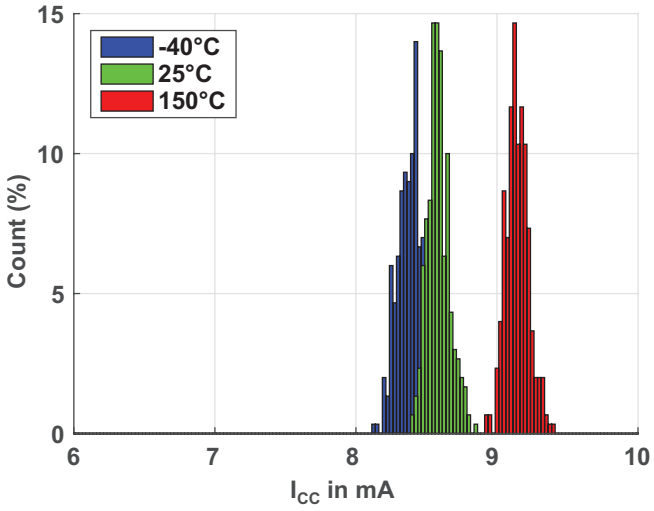

Figure 26: I_{CC} Distribution over Temperature (I_{CC} per die, V_{CC} = 3.7 V)

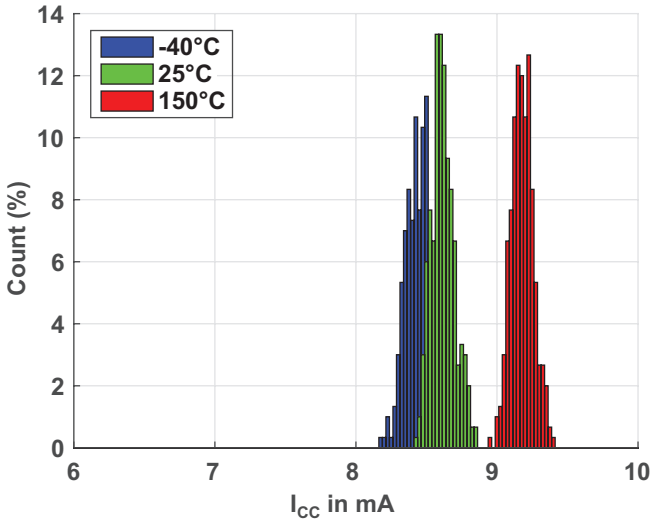

Figure 27: I_{CC} Distribution over Temperature (I_{CC} per die, V_{CC} = 16 V)

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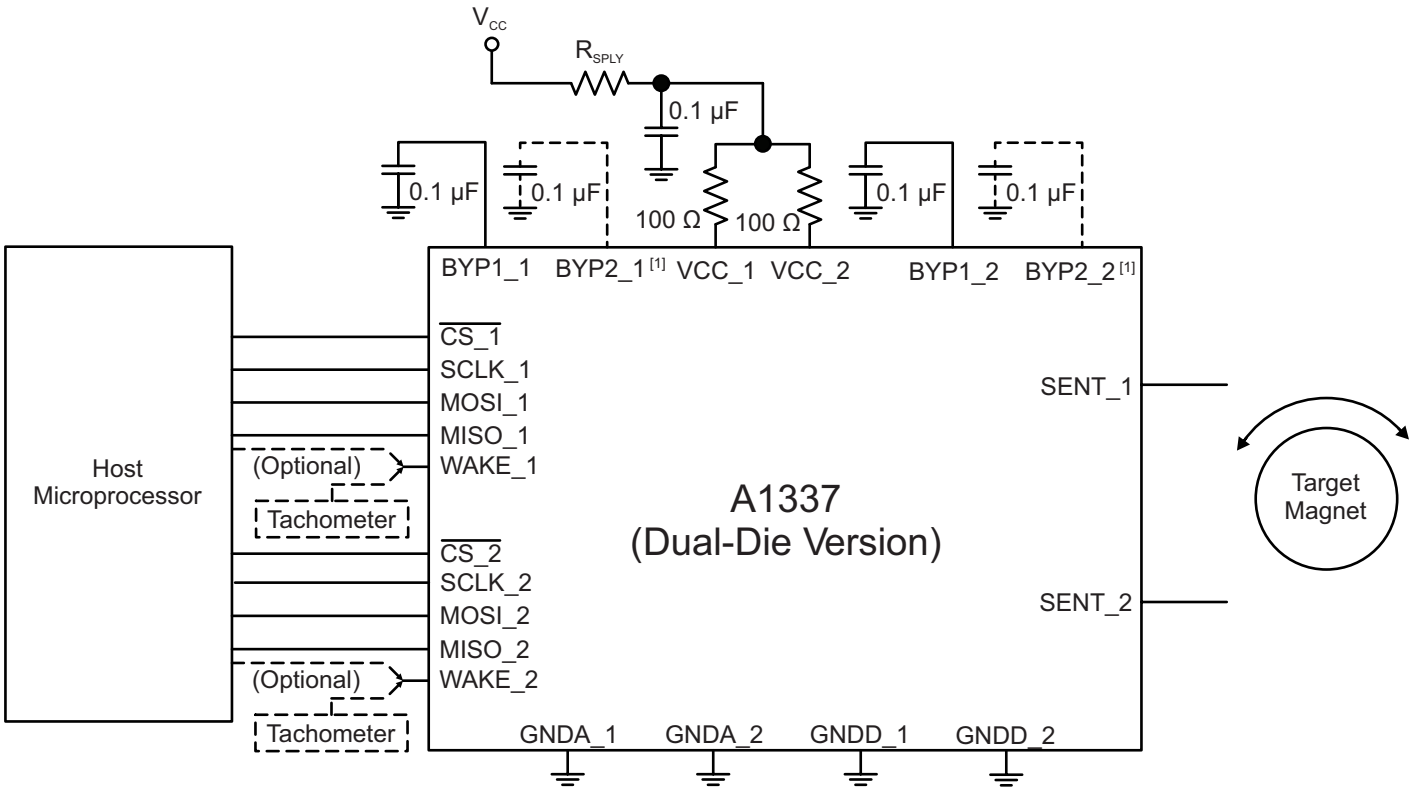
EMC Reduction

For applications with stringent EMC requirements, a 100 Ω resistance should be added to the supply for the device in order to suppress noise. A recommended circuit is shown in Figure 28.



[1] Secondary bypass capacitors only required when using elevated SPI output voltage. Contact Allegro for availability.

Figure 28: Typical Application Diagram (Dual-Die Version) with EMC Suppression Resistor, R_{SPLY}, on Supply Line

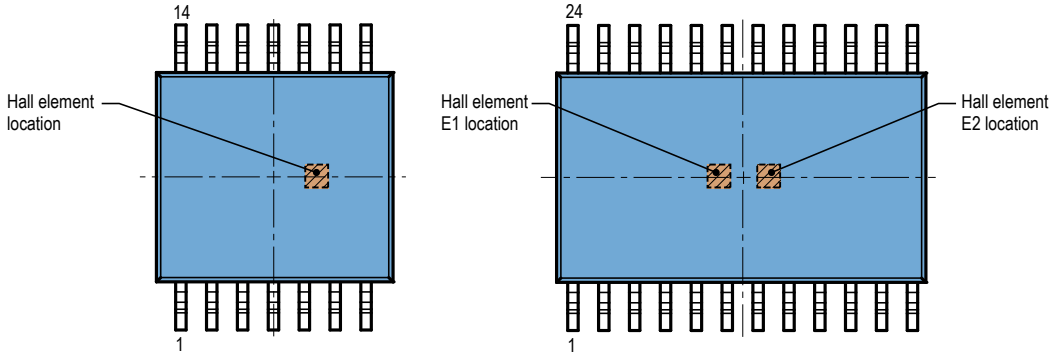


Figure 29: Hall Element Located Off-Center within Device Body
For reference dimensions, refer to the Package Outline Drawings.

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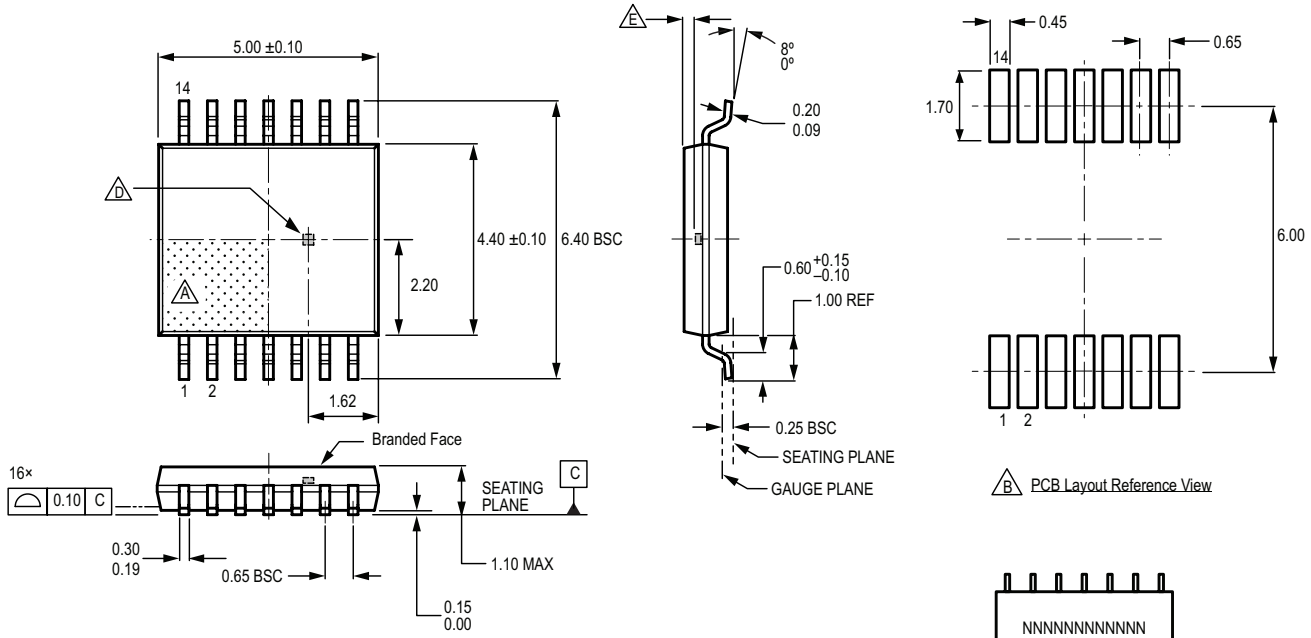
PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-14M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall element, not to scale

E Active Area Depth 0.36 mm REF

C Standard Branding Reference View

N = Device part number
= Supplier emblem
Y = Last two digits of year of manufacture
W = Week of manufacture
L = Lot number

Figure 30: Package LE, 14-Pin TSSOP

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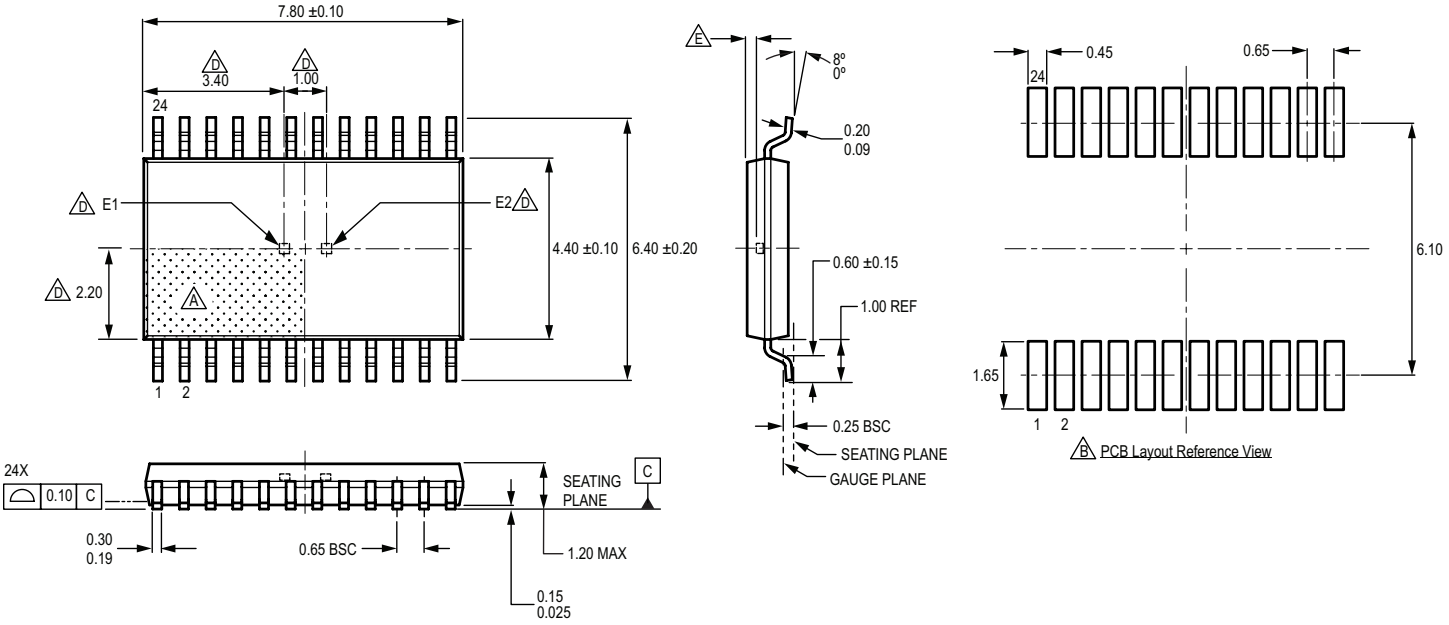
For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AD)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Hall elements (E1, E2), corresponding to respective die; not to scale

E Active Area Depth 0.36 mm REF

C Standard Branding Reference View

Lines 1, 2: Maximum 10 characters per line
Line 3: Maximum 8 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 31: Package LE, 24-Pin TSSOP

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Revision History

Number	Date	Description
–	November 18, 2016	Initial release
1	May 26, 2017	Overall editorial update
2	July 14, 2017	Updated Figure 14
3	January 24, 2018	Updated Typical Application Diagram (page 4); Low-Power Mode Average Supply Current test conditions and Bypass2 Pin Output Voltage characteristic and test conditions (page 7); PWM Carrier Frequency test conditions, Sent Output Signal maximum value, Logical BIST Coverage versus Time (page 8); Sleep State Period test conditions (page 9); Effective Resolution typical value, footnotes 8-15 (page 10); Overview, Angle Measurement sections (page 11-12); Table 2 (page 15); Manchester Code Low Voltage maximum value (page 18); Table 5 (page 21); Table 6 (page 22); CTRL Register, STS Self-Test Start (page 25); Calculating Target Zero-Degree Angle (page 27); and Figure 23 (page 32).
4	April 4, 2018	Updated PWM Interface Specifications (page 8); PWM Output section (page 16); EEPROM Registers Map Table (page 21); Serial Interface Structure (pages 23-27); Figures 20 and 22 (pages 32-33).
5	January 25, 2019	Minor editorial updates
6	March 6, 2020	Minor editorial updates
7	January 15, 2021	Updated Typical Applications (page 4), MOSI Hold Time value (page 7), Figure 19 (page 19), Table 6 (page 21), and Package Outline Drawing reference numbers (pages 35-36).
8	July 30, 2021	Removed references to PWM output from: Headings (all pages); Text on page 1; Selection Guide (page 2); Table of Contents (page 3); Pinout diagrams and tables (page 5); Operating characteristics (removed PWM interface specification, page 8); Text on page 10 (was page 11 in Rev. 7); Text on page 12 (was page 13 in Rev. 7); PWM section (removed page 16 of Rev. 7); Text on page 27 (was page 29 in Rev. 7); Removed Figure 14 and Figure 15 (as numbered in Rev. 7); and Modified Figures 1–4, Figure 14 (was Figure 16 in Rev. 7), Figure 28 (was Figure 30 in Rev. 7)), Table 2, Table 6, and Table 7.

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Revision History

Number	Date	Description
9	August 18, 2022	Removed date in association with ISO 26262 (page 20); and Updated Product Outline Drawing (page 34).
10	November 28, 2023	Changed archaic language (changed normal to typical or full-power, master to controller, and slave to peripheral), corrected response time figure reference (page 9), added hyperlinks to cross-referenced sections, changed many instances of title-case to lowercase font, rewrote sentences written in the future tense, changed footnote symbols to numbers, and made minor editorial corrections throughout (all pages).

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