A33022

Stray Field Immune, Hall-Effect Angle Sensor IC With SPI, PWM, and SENT Interfaces

FEATURES AND BENEFITS

- Contactless 0° to 360° angle sensor IC, for angular position, rotational speed, and direction measurement
  - Hall-effect technology
  - End of shaft
  - Stray field immune
- 11.2 bits noise-free resolution with 300 G field and 12.5 kHz bandwidth
- Default 25 µs latency with 12.5 kHz bandwidth (BW)
  - BW programmable from 3.125 kHz to 50 kHz
- Designed to meet ASIL D Top Level Safety Requirements in a single- or dual-die package, when used in conjunction with appropriate system-level control
- Wide operating voltage (3.7 V to 18 V) enables direct connection to vehicle battery
- Linearization to reduce error from misalignment between the sensor and target magnet
- SPI interface allows use of multiple independent sensors for applications requiring redundancy
- 5-bit cyclic redundancy check (CRC) on SPI messages
- SENT output is SAEJ716 JAN2016 compliant with Allegro proprietary enhancements
  - Customer programmable tick times down to 0.5 µs
  - Shared SENT allows multiple ICs to share a common SENT line
  - Configurable SENT output with 12-bit or 16-bit magnetic data
- EEPROM with error correction control (ECC) for trimming calibration
- EEPROM programmable angle reference (0°) position and rotation direction (clockwise or counterclockwise)
- AEC-Q100 Grade 0 qualified
- Wide operating temperature range: –40°C to 150°C

DESCRIPTION

The A33022 is a 360° angle sensor IC that provides contactless high-resolution angular position information based on magnetic sensing technology. The A33022 has a system-on-chip (SoC) architecture that includes angle sensing, digital signal processing, and various output options: serial peripheral interface (SPI), pulse width modulation (PWM), or single edge nibble transmission (SENT). Also integrated in the device is on-chip EEPROM technology capable of supporting a high number of read/write cycles, for flexible end-of-line programming of calibration parameters.

The low 25 µs latency of the A33022 makes it ideal for automotive applications requiring fast 0° to 360° angle measurements, such as electronic power steering (EPS), seatbelt motor systems, transmission actuators, shift-by-wire systems, electronic braking systems, and throttle systems.

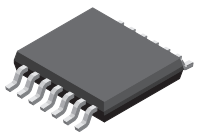
The A33022 is developed as a Safety Element out of Context (SEooC) in accordance with ISO 26262 requirements for hardware product development for use in safety-critical applications.

The A33022 also includes integrated linearization features. This allows the A33022 to correct for misalignment between the IC and the target magnet with minimal added latency.

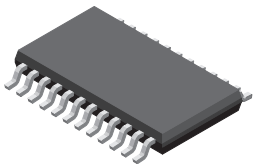
The A33022 is available in a single-die 14-pin TSSOP package and a dual-die 24-pin eTSSOP package. The packages are lead (Pb) free with 100% matte tin leadframe plating.

PACKAGES

Not to scale



14-pin TSSOP (Single Die, Suffix LE)



24-PIN eTSSOP with exposed pad (Dual Die, SUFFIX LP)

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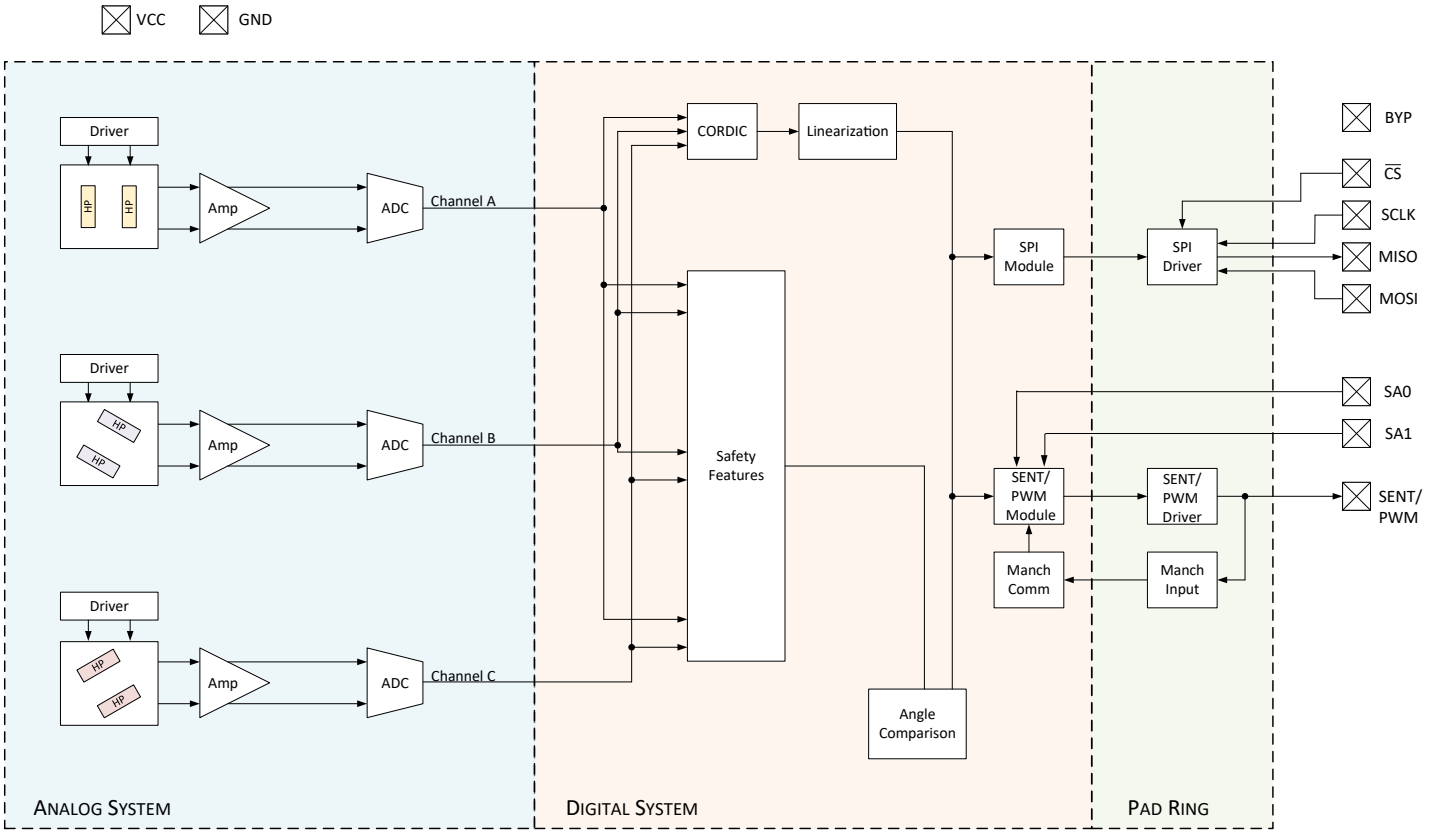

Figure 1: Functional Block Diagram

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SPECIFICATIONS

SELECTION GUIDE

Part Number	System Die	Nominal B_{IN}	Interface Voltage	Package	Packing
A33022LLEATR-300	Single	300 G	3.3 V	14-pin TSSOP	4000 pieces per 13-in reel
A33022LLEATR-600	Single	400 G	3.3 V	14-pin TSSOP	4000 pieces per 13-in reel
A33022LLEATR-300-5	Single	300 G	5 V	14-pin TSSOP	4000 pieces per 13-in reel
A33022LLEATR-600-5	Single	400 G	5 V	14-pin TSSOP	4000 pieces per 13-in reel
A33022LLPBTR-DD-300	Dual	300 G	3.3 V	24-pin eTSSOP	4000 pieces per 13-in reel
A33022LLPBTR-DD-600	Dual	400 G	3.3 V	24-pin eTSSOP	4000 pieces per 13-in reel
A33022LLPBTR-DD-300-5	Dual	300 G	5 V	24-pin eTSSOP	4000 pieces per 13-in reel
A33022LLPBTR-DD-600-5	Dual	400 G	5 V	24-pin eTSSOP	4000 pieces per 13-in reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Forward Supply Voltage	V_{CC}	Not sampling angles	38	V
Reverse Supply Voltage	V_{RCC}	Not sampling angles	–18	V
Digital I/O Forward Voltage (MOSI, MISO, SCLK, $\overline{CS}$, SA1, SA0, BYP)	V_{DIG}	3.3 or 5 V interface selected	5.65	V
Digital I/O Reverse Voltage	V_{RDIG}		–0.5	V
PWM/SENT Forward Voltage	V_{PWM}		18	V
PWM/SENT Reverse Voltage	V_{RPWM}		–0.5	V
Operating Ambient Temperature	T_A	L range	–40 to 150	°C
Maximum Junction Temperature	$T_{J(MAX)}$		165	°C
Storage Temperature	T_{STG}		–65 to 170	°C
ESD Rating	V_{ESD}	HBM testing per AEC-Q100; TSSOP-14 package	>4	kV
		HBM testing per AEC-Q100; eTSSOP-24 package	>4 [1]	kV

[1] All GND pins shorted together.

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see Operating Characteristics section.

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LE-14 package on 4-layer PCB based on JEDEC standard JESD51-7	82	°C/W
		LP-24 package on 4-layer PCB based on JEDEC standard JESD51-7	69	°C/W

[1] Additional thermal information available on the Allegro website.

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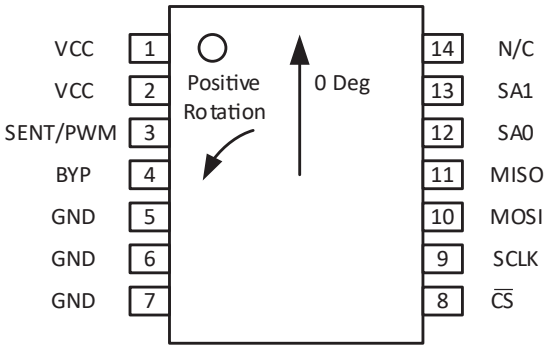
PINOUT DIAGRAMS AND TERMINAL LIST TABLES



Package LE 14-pin TSSOP Pinout Drawing

Terminal List Table

Number	Name	Function
1,2	VCC	Power supply
3	PWM/SENT	PWM or SENT angle output and Manchester communications
4	BYP	External bypass capacitor terminal for internal regulator
5, 6, 7	GND	Device ground terminal
8	$\overline{CS}$	SPI chip-select terminal (active low input)
9	SCLK	SPI clock terminal input
10	MOSI	SPI primary output/secondary input
11	MISO	SPI primary input/secondary output
12	SA0	SA0 (SENT addressing input)
13	SA1	SA1 (SENT addressing input)
14	No connect	Not connected; connect to ground in application

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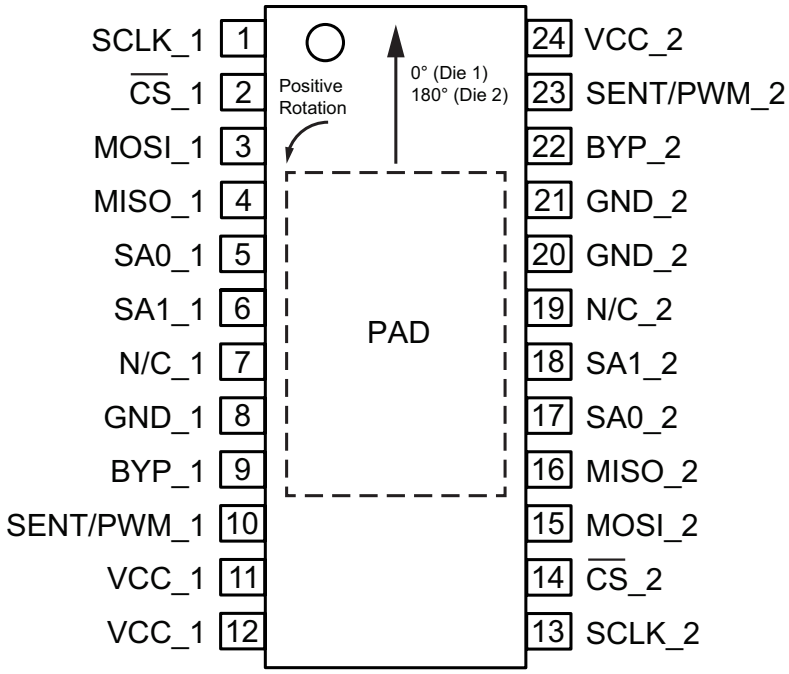

Package LP 24-pin eTSSOP Pinout Drawing

Terminal List Table

Die 1

Number	Name	Function
1	SCLK_1	SPI clock terminal input
2	$\overline{CS}$_1	SPI chip select terminal (active low input)
3	MOSI_1	SPI controller output/peripheral input
4	MISO_1	SPI controller input/peripheral output
5	SA0_1	SA0 SENT and Manchester addressing input Sets bit 0 of address field Tie to BYP for logic 1, GND for logic 0
6	SA1_1	SA1 SENT and Manchester addressing input Sets bit 1 of address field Tie to BYP for logic 1, GND for logic 0
7	NC	Not connected Connect to ground in application
8	GND_1	Device ground terminal
9	BYP_1	External bypass capacitor terminal for internal regulator
10	PWM/ SENT_1	PWM/SENT output and Manchester communication
11, 12	VCC_1	Power supply

Die 2

Number	Name	Function
13	SCLK_2	SPI clock terminal input
14	$\overline{CS}$_2	SPI chip select terminal (active low input)
15	MOSI_2	SPI controller output/peripheral input
16	MISO_2	SPI controller input/peripheral output
17	SA0_2	SA0 SENT and Manchester addressing input Sets bit 0 of address field Tie to BYP for logic 1, GND for logic 0
18	SA1_2	SA1 SENT and Manchester addressing input Sets bit 1 of address field Tie to BYP for logic 1, GND for logic 0
19	NC	Not connected Connect to ground in application
20, 21	GND_2	Device ground terminal
22	BYP_2	External bypass capacitor terminal for internal regulator
23	PWM/ SENT_2	PWM/SENT output and Manchester communication
24	VCC_2	Power supply

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CHARACTERISTIC PERFORMANCE

OPERATING CHARACTERISTICS: Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1] [2]	V_{CC}	3.3 V digital	3.7	–	18	V
		5 V digital with POK_EXT = 0	6	12	18	V
		5 V digital with POK_EXT = 1	4.5	12	18	V
		5 V digital pass-through mode with POK_EXT = 0	4.5	5	5.5	V
		5 V digital pass-through mode with POK_EXT = 1	3.7	5	5.5	V
Supply Current	I_{CC}	One die, sampling angles, $T_A \geq 25°C$	–	–	20	mA
		One die, sampling angles, $T_A < 25°C$	–	–	22	mA
Clock Frequency	f_{CLK}	Main oscillator, ADC signal processing oscillator	13.6	16	18.4	MHz
	f_{CLK_LF}	Low frequency oscillator	200	250	300	kHz
Undervoltage Flag Threshold	$V_{UVD(HIGH)}$	dV/dt = +1 V/ms, undervoltage flag clears	–	–	3.75	V
	$V_{UVD(LOW)}$	dV/dt = –1 V/ms, undervoltage flag asserts	3.35	–	–	V
Overvoltage Flag Threshold [3]	$V_{OVD(HIGH)}$	V_{CC} rising	21	22	–	V
	$V_{OVD(LOW)}$	V_{CC} falling	20	21	–	V
Forward Supply Zener Clamp Voltage	V_{ZUP}	$I_{CC} = I_{CC(max)} + 3$ mA	38	–	–	V
Reverse Supply Zener Clamp Voltage	V_{RZUP}	$I_{CC} = I_{RCC(min)}$	–	–	–18	V
Reverse Battery Current	I_{RCC}	$V_{CC} = –18$ V	–5	–	–	mA
Power-On Time [4][5]	t_{PO}		–	0.5	–	ms
Internal Bandwidth [5]	BW	IIR_BW_SEL = 000_2	2.5	3.125	3.75	kHz
		IIR_BW_SEL = 001_2	5	6.25	7.5	kHz
		IIR_BW_SEL = 010_2 (default)	10	12.5	15	kHz
		IIR_BW_SEL = 011_2	20	25	30	kHz
		IIR_BW_SEL = 100_2	40	50	60	kHz

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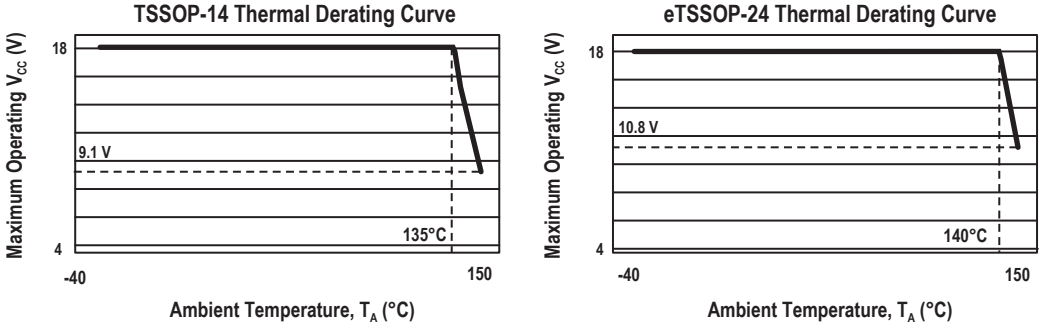
OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS (continued)						
Bypass Pin Output Voltage [6]	V_{BYP}	T_A = 25°C, C_{BYP} = 0.1 µF, 3.3 V interface voltage	2.97	3.3	3.63	V
		T_A = 25°C, C_{BYP} = 0.1 µF, 5 V interface voltage, V_{CC} ≥ 6 V	4.5	5	5.65	V

[1] Conditions of maximum supply voltage and ambient temperature must not exceed maximum junction temperature. At elevated ambient temperatures, the maximum operational voltage is reduced. See plot below. Plot is based on $R_{\theta JA}$, using a four-layer JEDEC standard PCB.



[2] Supply voltage ramp rate should be no slower than 25 V/ms when first energizing (0 to 5 V in 200 µs). Once device is powered on, the rate of change on V_{CC} must be limited to less than 1 V/µs for changes larger than 1 V in magnitude.
[3] Contact Allegro for additional OVD threshold options.
[4] SPI transactions will be valid within ≈ 500 µs of power on. Time for valid angle depends on filter bandwidth (typically 0.5 ms after power-on when using a 12.5 kHz bandwidth). Angle is considered valid once ANG_RDY (bit 0 of serial address 0xC) is set to 1, and no error flags are present.
[5] Parameter is not measured at final test. Determined by design.
[6] The output voltage specification is to aid in PCB design. The pin is not intended to drive any external circuitry. The specifications indicate the peak capacitor charging and discharging currents to be expected during normal operation. Parameter is not measured at finale test. Determined by design.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SPI GENERAL SPECIFICATIONS [1]						
Load Resistance	R_L		100	–	–	kΩ
Load Capacitance	C_L	Loading on digital output (MISO) pin with frequency up to 10 MHz	–	–	20	pF
		Loading on digital output (MISO) pin with frequency up to 1 MHz	–	–	50	pF
SPI Input Leakage Current	I_{L_SPI}	Leakage current into MOSI, SCLK, $\overline{CS}$ pins Bus voltage ≤ $V_{IH(MAX)}$	–	–	70	µA
SPI INTERFACE VOLTAGE SPECIFICATIONS (3.3 V DIGITAL)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins	2.8	–	3.63	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO pin, C_L = 50 pF, f_{SCLK} ≤ 1MHz	2.93	3.3	3.63	V
Digital Output Low Voltage	V_{OL}	MISO pin, C_L = 50 pF, f_{SCLK} ≤ 1MHz	–	0.3	0.5	V
SPI INTERFACE VOLTAGE SPECIFICATIONS (5 V DIGITAL)						
Digital Input High Voltage	V_{IH}	MOSI, SCLK, $\overline{CS}$ pins, V_{CC} ≥ 6 V	3.75	–	5.5	V
Digital Input Low Voltage	V_{IL}	MOSI, SCLK, $\overline{CS}$ pins, V_{CC} ≥ 6 V	–	–	0.5	V
Digital Output High Voltage	V_{OH}	MISO pin, C_L = 50 pF, f_{SCLK} ≤ 1 MHz, V_{CC} ≥ 6 V	4	5	5.5	V
Digital Output Low Voltage	V_{OL}	MISO pin, C_L = 50 pF, f_{SCLK} ≤ 1 MHz, V_{CC} ≥ 6 V	–	0.3	0.5	V
SPI INTERFACE TIMING SPECIFICATIONS [1]						
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	MISO pins, C_L ≤ 20 pF	0.1	–	10	MHz
		MISO pins, C_L ≤ 50 pF	0.1	–	1	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	f_{SPI}	SPI message is 32 bits	3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge, C_L = 20 pF	–	–	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to $\overline{CS}$ Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns

[1] Parameter is not measured at final test. Determined by design.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
PWM/SENT ELECTRICAL SPECIFICATIONS						
PWM/SENT Output Low Saturation Voltage	V_{SAT_LOW}	Sink current = 4.7 mA, V_{CC} = 5 V, output FET on	–	–	0.35	V
PWM/SENT Output High Saturation Voltage [1]	V_{SAT_HIGH}	Push-pull (3.3 V digital), I_{OUT} = 1 mA	2.85	–	–	V
		Push-pull (5 V digital), 6 V ≤ V_{CC} ≤ $V_{CC(MAX)}$, I_{OUT} = 1 mA	4.3	–	–	V
		Push-pull (pass-through mode), 4.5 V ≤ V_{CC} ≤ 5.5 V, I_{OUT} = 1 mA	0.85 × V_{CC}	–	–	V
Output Load Resistance [1]	$R_{L(PULLUP)}$	Pull-up resistor; push-pull, or open-drain mode	1.0	–	55	kΩ
	$R_{L(PULLDOWN)}$	Pull-down resistor; push-pull mode only	10	–	–	kΩ
Pull-Up Source Voltage [1]	V_{S_PWM}	Maximum pull-up source for PWM/SENT operation, open-drain output	–	–	5.65	V
		Maximum pull-up source for PWM/SENT operation, push-pull mode (3.3 V digital)	2.97	3.3	3.63	V
		Maximum pull-up source for PWM/SENT operation, push-pull mode (5.0 V digital)	4.35	5	5.65	V
PWM/SENT Load Capacitance [1]	C_{PWM_SENT}		–	–	4.7	nF
PWM/SENT Output Leakage Current	$I_{PWM\_leakage}$	Leakage into pin, FET off, V_{PWM} ≤ 5.5 V	–	–	20	µA
PWM/SENT Max Operational Current [1]	$I_{PWM\_MAX(SINK)}$	Maximum operating PWM/SENT sink current	–	–	20	mA
	$I_{PWM\_MAX(SOURCE)}$	Maximum operating PWM/SENT source current	–	–	2	mA
PWM/SENT Output Short-Circuit Current Limiter [1]	$I_{PWMSC(SINK)}$	Internally limited	20	–	50	mA
	$I_{PWMSC(SOURCE)}$	Internally limited	2	–	5	mA
PWM INTERFACE SPECIFICATIONS						
PWM Carrier Frequency [1]	f_{PWM}	PWM frequency minimum setting, T_A in specification	–	125	–	Hz
		PWM programmable options	–	16	–	steps
		PWM frequency maximum setting, T_A in specification	–	16	–	kHz
PWM Output Low Clamp [1]	$D_{PWM(MIN)}$	2% corresponds to PWM_PORCH_SEL set to 000_2 8% corresponds to PWM_PORCH_SEL set to 110_2	2	–	8	%
PWM Output High Clamp [1]	$D_{PWM(MAX)}$	92% corresponds to PWM_PORCH_SEL set to 110_2 98% corresponds to PWM_PORCH_SEL set to 000_2	92	–	98	%
PWM Output Clamp Step Size	$D_{PWM(step\_size)}$	PWM_PORCH_SEL EEPROM field	–	1	–	%

[1] Parameter is not measured at final test. Determined by design.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
SENT SPECIFICATIONS [1]						
SENT Tick Time	t_{TICK}	Programmable. All SENT Modes	0.5	–	7	µs
SENT Tick Time Tolerance	TOL_{tTICK}	All SENT Modes	–15	–	15	%
SENT Trigger Signal	$V_{SENTtrig(L)}$	SENT_HYST_CFG = 0, 2; falling edge threshold	1.48	–	1.79	V
	$V_{SENTtrig(H)}$	SENT_HYST_CFG = 0; rising edge threshold	2.21	–	2.49	V
		SENT_HYST_CFG = 2; rising edge threshold	1.92	–	2.19	V
SENT Trigger Threshold Hysteresis	$V_{SENTtrig(HYST)}$	SENT_HYST_CFG = 0	–	0.73	–	V
		SENT_HYST_CFG = 2	–	0.44	–	V
Minimum SENT Trigger Time	$t_{trig(MIN)}$	TRIGGER_CFG = 0	–	2.5	–	µs
		TRIGGER_CFG = 1	–	5	–	µs
		TRIGGER_CFG = 2	–	10	–	µs
		TRIGGER_CFG = 3	–	0.5	–	µs
SENT Output Trigger Edge Filter	$t_{SENTtrig(f)}$	Deglitch filter	–	0.375	–	µs
SENT Trigger Delay Time [2]	T_{dSENT}	Delay from end of trigger pulse to beginning of SENT message frame (for TSENT and shared SENT).	7	–	–	ticks
MANCHESTER SPECIFICATIONS [1]						
Bit Rate		Communication rate	4	–	100	kbps
Manchester Input Low Voltage	$V_{MAN(L)}$	SENT_HYST_CFG = 0,2; data pulses on SENT/PWM	1.48	–	1.76	V
Manchester Input High Voltage	$V_{MAN(H)}$	SENT_HYST_CFG = 0; data pulses on SENT/PWM	2.21	–	2.49	V
		SENT_HYST_CFG = 2; data pulses on SENT/PWM	1.92	–	2.19	V

[1] Parameter is not measured at final test. Determined by design.
[2] SENT output in open-drain configuration. Actual time includes a fixed 1.25 µs delay, independent of tick time. More precise definition: t_{dSENT} = 7 Ticks + 1.125 µs.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min	Typ	Max	Unit
MAGNETIC CHARACTERISTICS						
Input Magnetic Flux Density [1]	B_{IN}	For part numbers with suffix 300	–	300 [2]	400	G
		For part numbers with suffix 600	–	400 [2]	600	G
ANGLE CHARACTERISTICS						
Number of Angle Bits via SPI	N_{SPI}	Angle message length, SPI output	–	16	–	bits
Response Time [3][4]	$t_{RESPONSE}$	Angular latency, bandwidth = 3.125 kHz	–	90	–	µs
		Angular latency, bandwidth = 6.25 kHz	–	45	–	µs
		Angular latency, bandwidth = 12.5 kHz	–	25	–	µs
		Angular latency, bandwidth = 25 kHz	–	20	–	µs
		Angular latency, bandwidth = 50 kHz	–	15	–	µs
Refresh Rate [5]	t_{ANG}	Angle update	–	2	–	µs
Angle Error [6]	ERR_{ANG}	T_A = 25°C, ideal magnet alignment, target RPM = 0	–1.0	±0.5	1.0	degrees
		T_A = 150°C, ideal magnet alignment, target RPM = 0	–2.0	±0.9	+2.0	degrees
Angle Error Due to DC Stray Field [3]		T_A = 25°C, B_{stray} = 50G DC, B_{IN} = 300 G	–	±0.1	±0.4	degrees
Angle Error Due to AC Stray Field [3]		T_A = 25°C, AC stray field according to ISO11452-8 Test Level IV, B_{IN} = 300 G	–	±0.1	±0.4	degrees
Angle Drift Due to Temperature [6]	$ANGLE_{DRIFT}$	Change in angle from 25°C; T_A = 150°C, ideal magnet alignment, target RPM = 0	–1.2	±0.5	+1.2	degrees
		Change in angle from 25°C; T_A = –40°C, ideal magnet alignment, target RPM = 0	–	±0.5	–	degrees
Angle Drift Over Lifetime	$ANGLE_{DRIFT\_Life}$	B_{IN} = 300 G, average maximum drift observed following AEC-Q100 qualification testing	–	±0.5	–	degrees

[1] Input magnetic flux density, B_{IN}, is defined in the Input Magnetic Flux Density Definitions section.
[2] There is no strict minimum value for B_{IN}. However, because a low B_{IN} results in low angular resolution, operation is not recommended below 50 G for 300 G (typical) devices, or below 100 G for 400 G (typical) devices.
[3] Parameter is not measured at final test. Determined by design.
[4] Response time is measured at the time between the magnet crossing a given angle and the angle value updating within the IC. No communication delay is considered.
[5] Rate at which a new angle reading will be ready.
[6] Angle error and drift are inferred through channel characterization and signal path testing—not directly measured at final test.

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OPERATING CHARACTERISTICS (continued): Valid over operating voltage and temperatures, unless otherwise specified

Characteristics	Symbol	Test Conditions			Min	Typ	Max	Unit
ANGLE CHARACTERISTICS (continued)								
Angle Noise [1][2]	N_{ANG}	Target RPM = 0, 3 sigma; 300 G for 300 part variant; 400 G for 600 part variant	BW = 3.125 kHz	T_A = 25°C	–	0.040	–	degrees
				T_A = 150°C	–	0.080	–	degrees
			BW = 6.25 kHz	T_A = 25°C	–	0.050	–	degrees
				T_A = 150°C	–	0.110	–	degrees
			BW = 12.5 kHz	T_A = 25°C	–	0.075	–	degrees
				T_A = 150°C	–	0.160	–	degrees
			BW = 25 kHz	T_A = 25°C	–	0.085	–	degrees
				T_A = 150°C	–	0.210	–	degrees
			BW = 50 kHz	T_A = 25°C	–	0.110	–	degrees
				T_A = 150°C	–	0.260	–	degrees
Noise-Free Number of Bits [2][3]	b_{NOISE_FREE}	Target RPM = 0, 6 sigma; 300 G for 300 part variant; 400 G for 600 part variant	BW = 3.125 kHz	T_A = 25°C	–	12.1	–	bits
				T_A = 150°C	–	11.1	–	bits
			BW = 6.25 kHz	T_A = 25°C	–	11.8	–	bits
				T_A = 150°C	–	10.7	–	bits
			BW = 12.5 kHz	T_A = 25°C	–	11.2	–	bits
				T_A = 150°C	–	10.1	–	bits
			BW = 25 kHz	T_A = 25°C	–	11.0	–	bits
				T_A = 150°C	–	9.7	–	bits
			BW = 50 kHz	T_A = 25°C	–	10.7	–	bits
				T_A = 150°C	–	9.4	–	bits
Temperature Sensor [4]								
Temperature	$TEMP_{Bits}$	Main and redundant			–	12	–	bits
Temperature Resolution		1°C = 8 counts			–	0.125	–	°C
Overtemperature Threshold	OVT				–	170	–	°C
	UVT				–	–60	–	°C

[1] Value represents 3-sigma, or three times the standard deviation of the measured samples ($N_{ANG} = 3 \times \sigma$).
[2] Based on characterization data. Not measured at final test.
[3] Noise-free number of bits is defined as: $log_2 \left(\frac{360}{6 \times \sigma} \right)$, where σ is the rms angle noise.
[4] Parameter is not measured at final test. Determined by design.

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FUNCTIONAL DESCRIPTION

Overview

The A33022 is an automotive-qualified, four-channel, rotary position sensor. The four channels provide redundant angle sensing within a single monolithic surface-mount device.

This device is an advanced, programmable system-on-chip (SoC), incorporating six planar Hall-effect, analog signal conditioning, high-speed sampling analog-to-digital converters, digital filtering, digital signal processing (which includes two separate signal paths—primary and secondary), and multiple output options. Available outputs options include SPI, PWM, and SENT.

The primary (or main) channel comprises six planar Hall plates measuring the magnetic field perpendicular to the package. The three secondary channels are each a subset of four Hall plates out of the six from the main channel (for more details, refer to the Angle Measurements section). The information from each channel is processed in parallel to compute an angle measurement based on the input magnetic fields. The resulting angle information, primary and secondary, is passed through additional processing and made available as four independent outputs. In addition, the A33022 compares the primary angle to the secondary angles to monitor the integrity of the angle information.

Zero-angle, filtering, linearization, and diagnostic adjustment options are available in the A33022. These options are configurable in the onboard EEPROM, providing a wide range of sensing solutions in the same device.

Angle Measurements

The A33022 is capable of rejecting common-mode stray fields. It is based on the calculation of the equivalent “center of mass” of the measured magnetic fields. The center-of-mass analogy illustrates how the A33022 is a stray-field-immune sensor: If the same additional mass is applied to a group of weights, the angular position of the center of mass is unchanged. The A33022 has six planar Hall plates equally spaced in a 2 mm diameter circle (Figure 2, not to scale). The magnetic center is attracted toward a given Hall plate if it measures a positive magnetic field or repelled if it measures a negative magnetic field. While placed in front of the right rotating magnet, the magnetic center follows the same rotation as the magnet. The A33022 measures the position of this magnetic center and returns its angular position.

To evaluate the magnet angle position δ_{MAIN}, the A33022 realizes the following calculation:

$$\delta_{MAIN} = atan2\left(\frac{\frac{\sqrt{3}}{2}(CH_B + CH_C)}{CH_A + \frac{1}{2}(CH_B - CH_C)}\right)$$

Equation 1: Magnet angle position calculation

where:

- CH_A = HP1 – HP4,
- CH_B = HP2 – HP5, and
- CH_C = HP3 – HP6.

HPi is the magnetic field measured by Hall plate i along direction Z, perpendicular to the surface of the chip.

The A33022 also measures three redundant angles, using the functions f_1, f_2, and f_3:

- $\delta_{AB} = f_1(CH_A,CH_B)$
- $\delta_{BC} = f_2(CH_B,CH_C)$
- $\delta_{CA} = f_3(CH_C,CH_A)$

The A33022 compares the main and redundant angles at each clock cycle and switches to safe state if a sufficiently high mismatch is detected.

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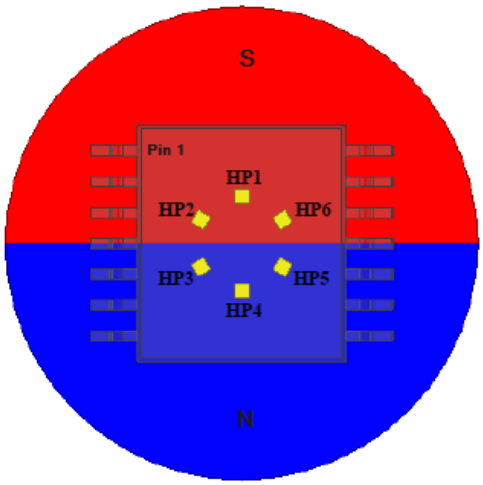

Figure 2: Axial view of the A33022 and the cylinder magnet with diametrical magnetization (showing default 0° position)

The A33022 is intended to work as an end-of-shaft angle sensor, in front of a rotating magnet. To achieve 360° absolute angle position, the magnet can be a:

- Two-pole ring, cylinder, or block magnet with diametrical magnetization (Figure 3). The typical magnetic field observed by these channels is presented in the Input Magnetic Flux Density Definitions section.
- Four-pole ring, cylinder, or block magnet with magnetization parallel to the axis of rotation (Figure 4).

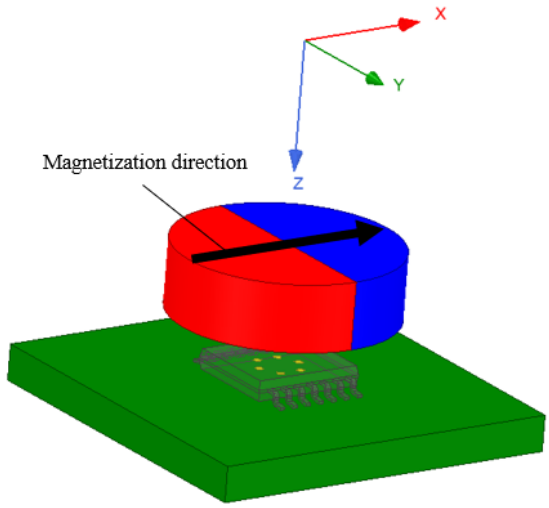

Figure 3: Isometric view of the A33022 and the cylinder magnet with diametrical magnetization

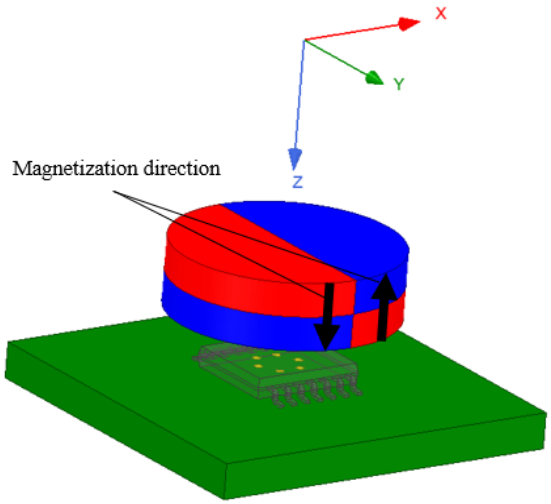

Figure 4: Isometric view of the A33022 and the cylinder magnet with four-pole axial magnetization

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Input Magnetic Flux Density Definitions

Each of the three signal channels observes a differential field as the magnet rotates above the IC. When discussing sensor performance, it is often easier to use the single-ended value of the input magnetic flux density, B_{IN}, instead of the differential value. B_{IN} is the average single-ended field exhibited across all Hall plates. For a perfectly aligned system, B_{IN} is the maximum field any single Hall plate experiences over a complete magnet rotation. Its relationship to the differential channel field is shown in Figure 5. B_{IN} is defined as:

$$B_{IN} = \frac{1}{3} \times \sqrt{\left(\frac{\sqrt{3}}{2}(CH_B + CH_C)\right)^2 + \left(CH_A + \frac{1}{2}(CH_B - CH_C)\right)^2}$$

B_{IN} defines the device resolution, where a high B_{IN} results in better resolution.

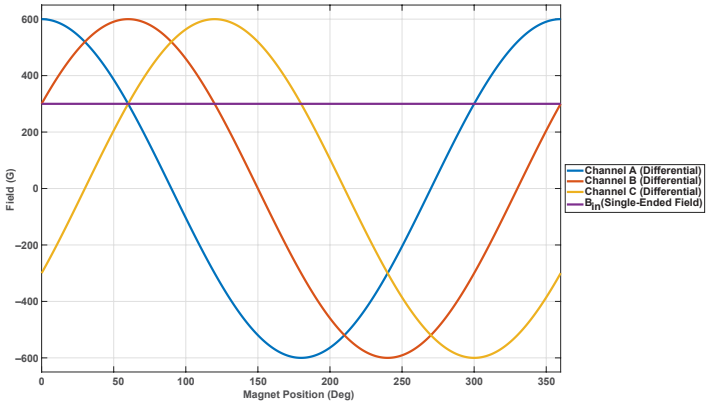

Figure 5: Differential channels and B_{IN} over magnet position with ideal IC position

System Level Timing

Internal registers are updated with a new angle value every t_{ANG}. The delay from the time of input until generation of a processed angle value is $t_{RESPONSE}$. SPI, which is asynchronously clocked, results in a varying latency depending on sampling frequency and SCLK speed. Register values transmitted are latched on the first SCLK edge of the SPI response frame. This results in a variable age in the angle data, ranging from $t_{RESPONSE} + t_{SPI}$ to $t_{RESPONSE} + t_{ANG} + t_{SPI}$, where t_{SPI} is the length of a read response packet, and t_{ANG} is the update rate of the angle register.

Similar to SPI, when using the PWM or SENT output, the output packet is not synchronized with the internal update rate of the sensor.

For PWM, the angle is latched at the beginning of the carrier frequency period (effectively at the rising edge of the PWM output). Because of this, the age of the angle value, once read by the system microcontroller, may be up to $t_{RESPONSE} + t_{ANG} + 1/f_{PWM}$. For SENT, the angle is typically latched at the beginning of the SENT frame (see SENT details for more information). The age of the data, once read, is $\approx t_{RESPONSE} + t_{ANG} + t_{SENT}$, where t_{SENT} is the length of the SENT packet.

Impact of High-Speed Sensing

Due to latency in the signal path, angle information is delayed by $t_{RESPONSE}$. This delay equates to a greater angle value as the rotational velocity increases (i.e., a magnet rotating at 20,000 rpm traverses twice as much angular distance in a fixed time period as a magnet rotating at 10,000 rpm), and is referred to as angular lag.

The lag is directly proportional to rpm. If the velocity is known, compensation for this lag can be made externally.

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Operational Modes

PWM OUTPUT

The A33022 provides a pulse-width-modulated output with a duty cycle proportional to the measured angle. The PWM frame consists of fixed low and high times as well as the linear region (or active period) used to communicate angle data.

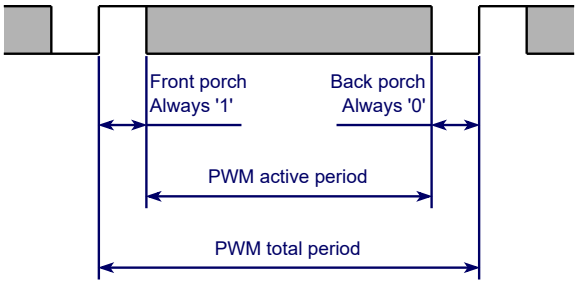

Figure 6: PWM output

PWM Carrier Frequency

The PWM carrier frequency is controlled by the SENT_PWM_RATE EEPROM field. The configured frequency also determines the resolution of the communicated angle message.

SENT_PWM_RATE	PWM Frequency (Hz)	Resolution (Bits)
0	125.0	15
1	166.7	15
2	250.0	14
3	333.3	14
4	500.0	13
5	666.7	13
6	800.0	13
7	1000.0	12
8	1333.3	12
9	1600.0	12
10	2000.0	11
11	2666.7	11
12	4000.0	10
13	5333.3	10
14	8000.0	9
15	16000.0	8

Fixed High and Low Times

The fixed high and low times of the PWM frame are configurable via the EEPROM PWM_PORCH_SEL field. The times are always applied symmetrically, such that a setting of 0 results in a duty cycle range of 2% to 98% (guaranteed 2% for the low and high porch sections).

PWM_PORCH_SEL	Fixed Time (% Duty Cycle) (Fixed Time = Front Porch and Back Porch)
0	2
1	3
2	4
3	5
4	6
5	7
6	8
7	0

Fault Reporting

The PWM output reports error with two high-level options:

- Tristate the output; or
- Go to a predetermined duty cycle and carrier frequency, depending on the error.

Errors can also be masked to prevent them from impacting the PWM output. For additional details, refer to the Error Reporting Through PWM section.

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Push/Pull Behavior

The PWM output follows the same push/pull behavior as described for the SENT protocol.

PWM/SENT Output Drive Control

The PWM/SENT output can be selected for the following states:

- Open-drain.
- Push-assist mode:
  - The high-side FET is used during the rising edge of the transaction only.
- Full push-pull.

The operating mode of the PWM/SENT output driver is controlled by the PUSH_DRIVE EEPROM field.

Register	Bits	Value	Description
PUSH_DRIVE	2	0	Open-drain SENT
		1	Push-assisted SENT
		2	Push-pull SENT
		3	Open-drain SENT

An additional Idle_Push field specifies the behavior of the output driver between SENT frames (in the pause pulse).

Register	Value	Description
IDLE_PUSH	0	In PUSH_PULL SENT, high-impedance (high-Z) during idle state
	1	In PUSH_PULL SENT, push during idle state

Operation throughout the SENT frame is described in the table below.

Device State	POR	Idle (Pause)	Trigger	Message High		Message Low
PUSH_DRIVE = 0 or 3	High-Z	High-Z	Trigger Pulse	High-Z		Pull-Low
PUSH_DRIVE = 1	High-Z	High-Z	Trigger Pulse	Push	High-Z	Pull-Low
PUSH_DRIVE = 2; IDLE_PUSH = 0	High-Z	High-Z	Trigger Pulse	Push		Pull-Low
PUSH_DRIVE = 2; IDLE_PUSH = 1	High-Z	Push	Trigger Pulse [1]	Push		Pull-Low

[1] Controller must overdrive the device output current.

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Linearization Feature

The A33022 contains 16 fixed segments of linearization for the main signal path and all three redundant signal paths. Linearization allows for the conversion of the sensor measured magnetic field data into a customer-desired output. This can be used to correct minor imperfections in the magnet or mounting tolerances.

Linearization converts the measured angle (sensed by the IC) into a corrected output angle. Typically, this is used to align the measured angle to the mechanical angle (the actual magnet position).

The IC performs linearization by taking the measured angle and adding/subtracting a correction factor. This correction factor differs over the measured angle and is based on linearization coefficients stored in EEPROM. There are 16 coefficients, or Y entries (16 for each main and redundant channel), corresponding to the 16 measured angles corresponding to [0°, 22.5°, 45°, …, 315°, and 337.5°]. For electrical angles not matching an entry in the EEPROM table, the correction factor is calculated by linearly interpolating between the two closest coefficients.

The Y linearization EEPROM fields are 8-bit signed values; each coefficient has a range of –128 to 127 LSB, corresponding to a correction of –11.25 to +11.25 degrees (0.088° step size). The EEPROM field name is in the form of XX_LINEARIZATION_YY, where XX stands for AB, BC, CA, or MAIN, and YY ranges from 0 to 15. YY = 0 corresponds to the angle correction for the measured position 0°. YY = 1 corresponds to the angle correction for the measured position 22.5°. See Table 2 for more details. For example, MAIN_LINEARIZATION_7 is the angle correction applied to the measured MAIN_ANGLE = 157.5°.

Figure 7 is shown as an example of a nonlinear curve that is corrected by the sensor. In this example, the Y values contained within EEPROM fields YY = 3, 4, and 8 are positive numbers, while the Y values within EEPROM fields YY = 6 and 7 are negative numbers (YY = 5 provides essentially no correction).

The A33022 sample programmer can be used to calculate the linearization coefficients or, alternatively, a MATLAB function can be used, as provided in the Appendix (see the MATLAB Function to Compute the A33022 Linearization Coefficients section).

Note that, in the case of a short stroke (roation < 360°), for proper linearization at the range ends, calibration is recommended with a linearization point beyond both ends of the stroke. If that is not possible, the alternative recommendation is to use a calculation that includes extrapolation of the measured angles at the first-neighbor calibration angles. For example, if the range is [20°:100°], programming of XX_LINEARIZATION_0 and XX_LINEARIZATION_5 is recommended, in addition to XX_LINEARIZATION_1 to XX_LINEARIZATION_4.

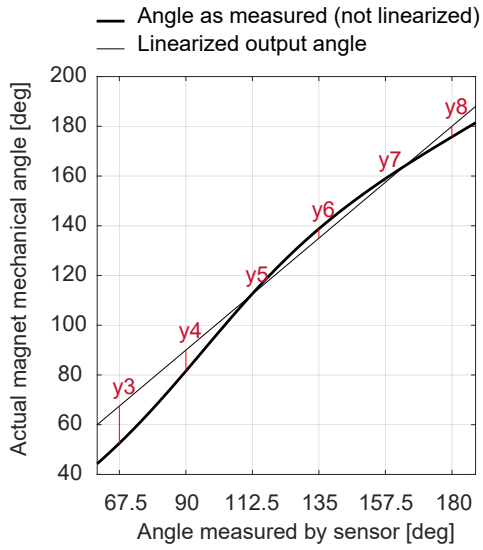

Figure 7: Schematic view of output angle linearization

Table 1: EEPROM Names and Angles

EEPROM Field XX stands for AB, BC, CA, or MAIN	Corresponding measured angle to be corrected (degrees)
XX_LINEARIZATION_0	0
XX_LINEARIZATION_1	22.5
XX_LINEARIZATION_2	45
XX_LINEARIZATION_3	67.5
XX_LINEARIZATION_4	90
XX_LINEARIZATION_5	112.5
XX_LINEARIZATION_6	135
XX_LINEARIZATION_7	157.5
XX_LINEARIZATION_8	180
XX_LINEARIZATION_9	202.5
XX_LINEARIZATION_10	225
XX_LINEARIZATION_11	247.5
XX_LINEARIZATION_12	270
XX_LINEARIZATION_13	292.5
XX_LINEARIZATION_14	315
XX_LINEARIZATION_15	337.5

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DEVICE PROGRAMMING INTERFACES

The A33022 can be programmed in two ways:

- Using the *SPI interface* for input and output
- Using a *Manchester protocol* on the PWM/SENT pin to send and receive data

The A33022 does not require special supply voltages to write to the EEPROM.

All accessible fields of the IC may be read and written using both protocols. If EEPROM locking is used, write access using either protocol may be limited.

Interface Structure

The A33022 consists of two memory blocks: direct memory (primary serial registers); and extended memory (EEPROM, shadow memory, volatile registers). The primary serial interface registers are used for direct writes and reads by the host controller for frequently required information (for example, angle data, warning flags, field strength, and temperature). All forms of communication (including the extended locations) operate through the primary registers, whether it be via SPI or Manchester.

The primary serial registers provide data and address location for accessing extended memory locations. Accessing these extended locations is done in an indirect fashion: The controller writes into the primary interface to give a command to the sensor to access the extended locations. Read/Write is executed, and the result is again presented in the primary interface. This concept is shown in Figure 8.

For writing extended locations, the primary interface registers INDIRECT_WR_ADDRESS (primary: 0x1), INDIRECT_WR_DATA_MSB (primary: 0x2), and INDIRECT_WR_DATA_LSB (primary 0x3) are used for writing extended memory locations. INDIRECT_WR_ADDRESS holds the address of the target extended memory location to be written. INDIRECT_WR_DATA_MSB and INDIRECT_WR_DATA_LSB, contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_WR_STATUS (primary: 0x4) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For reading extended locations, the primary interface registers INDIRECT_RD_ADDRESS (primary: 0x5), INDIRECT_RD_DATA_MSB (primary: 0x7), and INDIRECT_RD_DATA_LSB (primary 0x8) are used for reading extended memory locations. INDIRECT_RD_ADDRESS holds the address of the target extended memory location to be read. INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB contain the two high bytes and the two low bytes for the extended location contents. The INDIRECT_RD_STATUS (primary: 0x6) register is used for commands and status information. For further information and other register fields associated with indirect memory transactions, refer to Read Transaction from EEPROM and Other Extended Locations.

For more information on EEPROM and shadow memory read and write access, see EEPROM and Shadow Memory Usage.

The primary serial interface can be accessed using the SPI and using the Manchester interface. These two interfaces are detailed in the following sections.

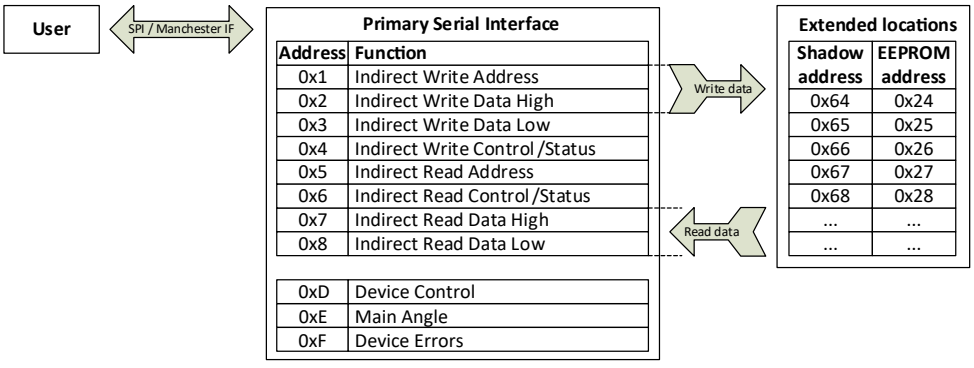

Figure 8: Serial registers allow access to extended memory (EEPROM and shadow)

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SPI

The A33022 provides a full-duplex 4-pin SPI interface, using SPI mode 3 (CPHA = 1, CPOL = 1).

The sensor responds to commands received on the MOSI (controller-out/peripheral in), SCLK (serial clock), and $\overline{CS}$ (chip-select) pins, and outputs data on the MISO (controller in/peripheral out) pin. SPI may operate at either 3.3 V or 5 V, depending on the interface voltage specified for the part number.

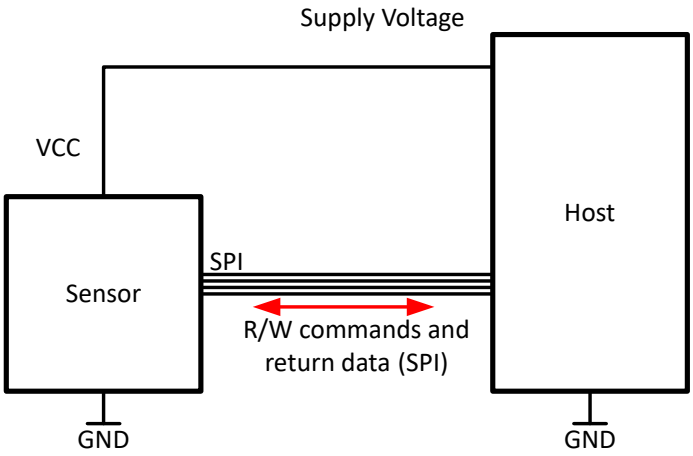

Figure 9: SPI Interface Programming Setup

TIMING

The interface timing parameters from Table 2 are displayed in Figure 10 and Figure 11.

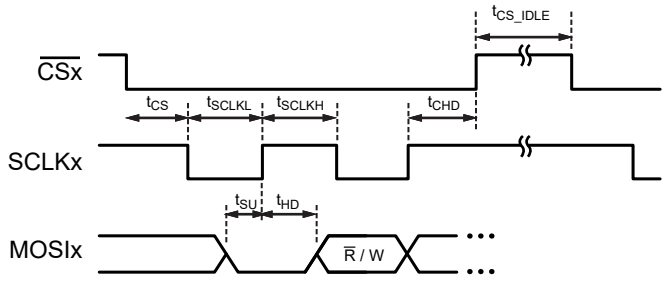

Figure 10: SPI Interface Timings Input

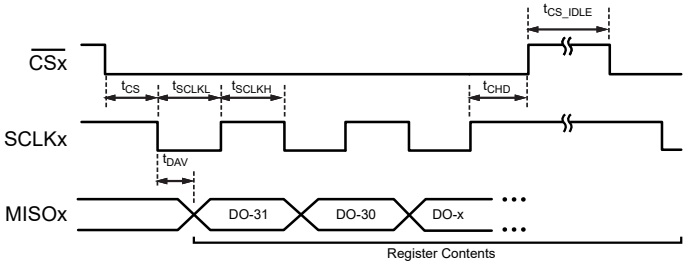

Figure 11: SPI Interface Timings Output

Table 2: SPI Interface Timings Output [1]

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SPI Message Length	SPI_{LENGTH}		32	–	32	bits
SPI Clock Frequency	f_{SCLK}	MISO pins, $C_L \le 20$ pF	0.1	–	10	MHz
		MISO pins, $C_L \le 50$ pF	0.1	–	1	MHz
SPI Clock Duty Cycle	D_{fSCLK}	SPI_{CLKDC}	40	–	60	%
SPI Frame Rate	f_{SPI}	SPI message is 32 bits	3	–	289	kHz
Chip Select to First SCLK Edge	t_{CS}	Time from $\overline{CS}$ going low to SCLK falling edge	50	–	–	ns
Chip Select Idle Time	t_{CS_IDLE}	Time $\overline{CS}$ must be high between SPI message frames	200	–	–	ns
Data Output Valid Time	t_{DAV}	Data output valid after SCLK falling edge, $C_L = 20$ pF	–	–	50	ns
MOSI Setup Time	t_{SU}	Input setup time before SCLK rising edge	25	–	–	ns
MOSI Hold Time	t_{HD}	Input hold time after SCLK rising edge	40	–	–	ns
SCLK to $\overline{CS}$ Hold Time	t_{CHD}	Hold SCLK high time before $\overline{CS}$ rising edge	5	–	–	ns

[1] Parameter is not measured at final test. Limits are based on design simulations.

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MESSAGE FRAME

The SPI interface uses a 32-bit packet and is designed to provide a high level of confidence in data integrity. Three SPI transactions are possible: write cycle, read request (from the controller), and read response (from the peripheral).

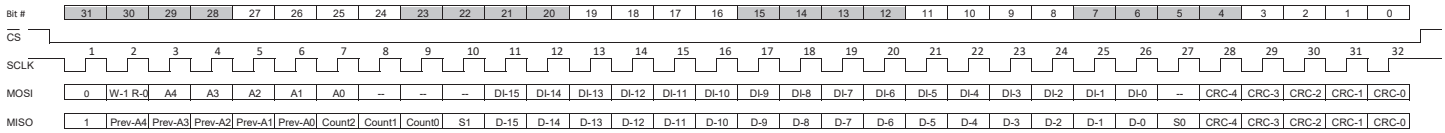

Figure 12: 32-Bit SPI Frame

Write Cycle or Read Request Cycle

The frame structures of the write cycle and read request are shown in Figure 13 and Figure 14, respectively. The frames consist of:

- Start Bit [31]: Static bit with logic = 0. This bit is not used in the CRC calculation.
- R/W [30]: Read/Write bit set to logic = 1 indicates a write cycle; logic = 0 indicates a read request.
- Address [29:25]: Address bits for accessing primary registers.
- Data [21:6]: Data bit for writing primary registers. Considered immaterial for a read request.
- CRC [4:0]: CRC bits calculated on the frame bits [30:5].
- Immaterial bits [24:22, 5]: Can be set to logic = 1 or logic = 0.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	1	Address [4:0]					—			Data [15:0]																—	CRC [4:0]				

Figure 13: Write Cycle SPI Frame

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	0	0	Address [4:0]					—			Data [15:0] (Immaterial for a read request)																—	CRC [4:0]				

Figure 14: Read Request Cycle Frame

Read Response Cycle

The read response cycle frame is sent from the IC, as shown in Figure 15. The frame consists of the following:

- Start bit [31]: This bit is set to logic = 1. This bit is not used in the CRC calculation.
- Previous address [30:26]: Register address corresponding to the read request data.
- Frame count [25:23]. Frame counter increments with each SPI frame.
- S1 [22]: Status/Error Flag
  - Logical OR of all unmasked error flags.
  - Will clear once presented following a read (assuming condition has cleared).
- S0 [5]: Status/Error Flag
  - Logical OR of all unmasked error flags.
  - Will clear once presented following a read (assuming condition has cleared).
- Data [21:6]: Data contents from primary register.
- CRC [4:0]: CRC bits calculated over the frame [30:5].

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	Previous Address [4:0]					Frame Count [2:0]			S1	Data [15:0]																S0	CRC [4:0]				

Figure 15: Read Response Cycle Frame

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SPI CRC

Each SPI frame includes a 5-bit CRC, calculated using the polynomial: $x^5 + x^2 + 1$ with a seed value of 11111_2.

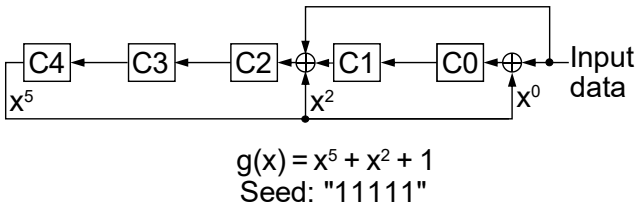

Figure 16: CRC Calculation with Left Shift Register

The outgoing CRC is calculated by the A33022 and transmitted on the MISO pin. The incoming CRC must be calculated by the controller and included on the MOSI pin. The A33022 checks the CRC on every incoming frame, and any invalid frame is ignored. The CRC achieves a Hamming distance of 3 for secure data transmission.

The CRC may be calculated with the following C code:

```
#include <stdio.h>
#include <stdint.h>
#include <stdbool.h>
/**
 * Computes a 5-bit CRC using the polynomial X^5 + x^2 + 1
 *
 * This function calculates a 5-bit Cyclic Redundancy Check (CRC)
 * for a given SPI Frame.
 * It utilizes the specified polynomial (X^5 + x^2 + 1) for compu-
tation.
 *
 * @param data The input data for which the CRC is to be calcu-
lated.
 * @param numberOfBits The number of bits to consider for the CRC
calculation.
 *        Should be set to 26, MSB of SPI frame is not included in
CRC calc.
 * @return The computed 5-bit CRC value as a 16-bit unsigned inte-
ger. The CRC
 *         is based on the provided polynomial and the specified
number of bits
 *         from the input data
 */
uint16_t SPI_CRC5(uint64_t data, uint16_t numberOfBits) {
       bool C0 = false;
       bool C1 = false;
       bool C2 = false;
       bool C3 = false;
       bool C4 = false;

       bool C0p = true;
       bool C1p = true;
       bool C2p = true;
       bool C3p = true;
       bool C4p = true;

       bool newBit = false;

       uint64_t bitMask = 1;
       bitMask <<= numberOfBits - 1;

       for (; bitMask != 0; bitMask >>=1) {
                newBit = ((data & bitMask) != 0);

                C4 = C3p;
                C3 = C2p;
                C2 = C1p ^ C4p ^ newBit;
                C1 = C0p;
                C0 = C4p ^ newBit;

                C0p = C0;
                C1p = C1;
                C2p = C2;
                C3p = C3;
                C4p = C4;
       }
       return (C4? 16U: 0U) + (C3? 8U: 0U) + (C2? 4U: 0U) + (C1?
2U: 0U) + (C0? 1U: 0U);
}
```


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The CRC may be calculated with the following Python code:

```
def spi_crc(data_frame):
    """
    SPI CRC: Takes 27 bit input and generates 5 bit CRC.
    Polynomial = x^5 + x^2 + 1
    Initial CRC value set to all 1s

    Input:
        data_frame: a string representing 27 bit binary data
    """
    crc = list('11111')  #CRC seed = 11111
    # MSB of SPI frame is not used during CRC calculation.
    for j in range(1, 27):
        old_crc = crc
        aux_crc_1 = crc[1]
        aux_crc_4 = crc[4]
        crc[4] = int(old_crc[3])
        crc[3] = int(old_crc[2])
        crc[2] = int(aux_crc_1) ^ int(aux_crc_4) ^ int(data_frame[j])
        crc[1] = int(old_crc[0])
        crc[0] = int(aux_crc_4) ^ int(data_frame[j])
    #flips calculated CRC around to obtain value in proper order
    crc = crc[::-1]
    return crc
```

A MATLAB implementation of the CRC is:

```
function [output_binary_word,CRC]=Allegro_CRC_x5_x2(input_
binary_word)
%% Initialization
CRC=ones(5,1);
%% CRC calculation
for i=1:length(input_binary_word)
    old_CRC=CRC;
    aux_CRC2=CRC(2);
    aux_CRC5=CRC(5);
    CRC(5)=old_CRC(4);
    CRC(4)=old_CRC(3);
    aux=xor(aux_CRC2,aux_CRC5);
    CRC(3)=xor(aux,str2num(input_binary_word(i)));
    CRC(2)=old_CRC(1);
    CRC(1)=xor(aux_CRC5,str2num(input_binary_word(i)));
end
%% Outputs
CRC=[num2str(CRC(5)) num2str(CRC(4)) num2str(CRC(3))
num2str(CRC(2)) num2str(CRC(1))];
output_binary_word=[input_binary_word CRC];
```


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MISO RESPONSE ON RECEIPT OF BAD CRC

When the A33022 detects an incorrect incoming CRC, the IER flag (direct address 0x0F, bit 15) asserts. A special SPI packet from the A33022 is returned on the next SPI frame. The contents of this special SPI packet are:

- Previous Address [30:26]: Set to 0x11.
- Data [21:6]: Contains the contents of the error register (primary: 0xF).
  - Note: The IER flag is not set on this first SPI packet; however, a read of the error register (address 0x0F) shows the IER flag asserted.

This packet is shown in Figure 17.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	1	Frame Count [2:0]			0	IER	XEE	BSY	SME	EUE	ESE	POR	OVCC	UVCC	MSH	MSL	SMM	OFE	SAT	TSE	VCF	0	CRC [4:0]				

Figure 17: First MISO Response Following a Bad Incoming CRC

MISO RESPONSE FOLLOWING A WRITE

Following a write operation, the MISO packet contains predetermined values within the Previous Address and Data fields:

- Previous Address [30:26]: Set 0x10.
- Data [21:6]: Primary angle value (ANGLE_OUT_MAIN from primary 0xE).

This packet is shown in Figure 18.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MISO	1	1	0	0	0	0	Frame Count [2:0]			S1	ANGLE_OUT_MAIN																S0	CRC [4:0]				

Figure 18: MISO Response Following a Write Operation

SPI POWER-ON RESPONSE

After a power-cycle, S1 and S0 are set to logic = 1 until the ANGLE_RDY (primary: 0xC [0]) bit is set and no other errors are locked. This is an indication to the controller that the signal chain has stabilized and the angle is valid. In addition, transitioning S1 and S0 from logic = 1 to logic = 0 allows for the detection of a stuck diagnostic bit. The full content of the first SPI return packet following a power-on is 0x80400021. This response only occurs following a full power-cycle. The SPI logic does not reset following a full or soft reset initiate via the CTRL register (Address 0x0D).

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Description	1	Address					Frame Cnt			S1	Data																S0	CRC				
Binary	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Figure 19: Initial SPI Response Frame Following Power-On

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Manchester Interface

The A33022 incorporates a serial interface shared with the PWM/SENT pin (Note: The A33022 may be programmed via SPI, with additional wiring connections). The device uses a point-to-point communication protocol based on Manchester encoding per G.E. Thomas (a rising edge indicates logic = 0, and a falling edge indicates logic = 1), where the address and data are transmitted with the MSB first. The addressable Manchester code implementation uses the logic states of the SA0/SA1 pins to set address values for each die. In this way, individual communication can be performed with up to four A33022 die per line.

Only the PWM/SENT pin is used for communication and entering into Manchester mode. The V_{CC} level is not used to enter Manchester mode.

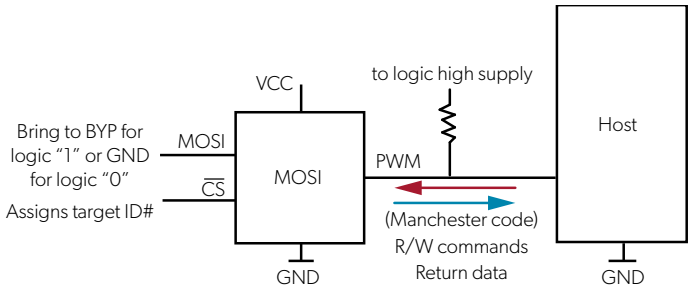

Figure 20: Manchester Programming Interface Setup

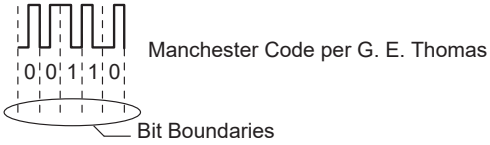

Figure 21: Manchester Code

MANCHESTER MESSAGE STRUCTURE

The general format of the Manchester message frame is shown in Table 3. Serial binary data is encoded using a Manchester encoding scheme, where logic = 1 is indicated by a falling edge within the bit boundary, and logic = 0 is indicated by a rising edge within the bit boundary. The time period for the bit boundary is determined by the baud rate initiated by the external controller. The A33022 read acknowledge is transmitted at the same rate as the command message frame. The bits are described in Table 3.

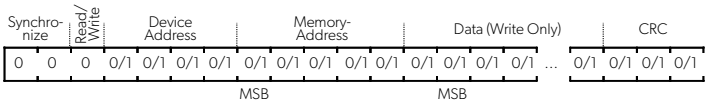

Figure 22: Manchester Message Structure

Table 3: Manchester Message Structure

Quantity of Bits	Name	Values	Description
2	Synchro-nization	0	Used to identify the beginning of a serial interface command and communication bit time
1	Read / Write	0	[As required] Write operation
		1	[As required] Read operation
4	Device Address	0x to 0xF	Used to identify device on the bus
5	Address	0x-0x1F	[Read/Write] Register address (of primary serial interface)
16	Data	0/1	Write only
3	CRC	0/1	Bits to check the validity of frame

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SPECIFYING A DEVICE ADDRESS

An A33022 die is assigned a specific die ID value by the logical state of the SA0 and SA1 pins.

Table 4: Die ID

SA1	SA0	ID Value
0	0	ID0
0	1	ID1
1	0	ID2
1	1	ID3

Using the 4 bits of the Device Address field (of the Manchester write frame), different die may be selected via their assigned ID value, allowing up to four die to be individually addressed and providing for different group addressing schemes. If the Device Address contains all zeros, no ID comparison is made, allowing all A33022 devices to be addressed at once.

Table 5: Device Address

Device Address			
ID3	ID2	ID1	ID0

Example:

If the Device Address of a Manchester packet is 4'b1000, only the die that has ID3 set (both SA1 and SA0 held high) is addressed.

READ COMMAND

The Read command is 15 bits in length, composed of 2 synchronization bits, 1 R/W bit, 4 die ID bits, 5 memory address bits, and 3 CRC bits.

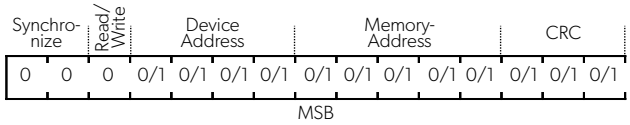

Figure 23: Manchester Read Request Command

READ ACKNOWLEDGE

The Read Acknowledge frame is composed of the synchronization bits, 16 data bits, and 3 CRC bits.

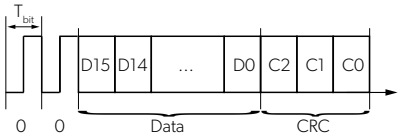

Figure 24: Manchester Read Acknowledge Command

WRITE COMMAND

The Write command is 31 bits in length, composed of 2 synchronization bits, 1 R/W bit, 4 die ID bits, 5 memory address bits, 16 data bits, and 3 CRC bits.

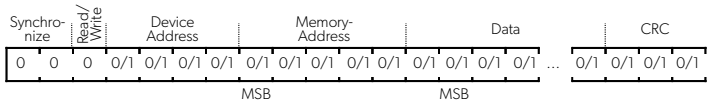

Figure 25: Manchester Write Command

The 5-bit memory address corresponds to the serial register address to which the 16 bits will be written.

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TIMING DURING A MANCHESTER READ RESPONSE

The A33022 never initiates communication. The A33022 recognizes four transactions: write access, write to EEPROM, write to volatile, and read. Only the read transaction prompts the A33022 to respond with data. When responding to a read command, the A33022 does not check for line contention; it is the responsibility of the controller to release the line in time and to be ready to read the data sent by the A33022.

After a read command is received, there is a delay between when the last bit of the command is sent to the device and when the device begins to respond on the line. This delay has two parts:

- The first part of the delay (t_d) occurs between the time the last bit of the read command is received and the time the device begins to pull the line low in preparation to send data.
- The second part of the delay (t_b) occurs between the time the device pulls the line low to the time the device begins outputting data. The output is fully readable as long as the controller releases control before $t_d + t_b$; however, it is recommended that the line be released before t_d.

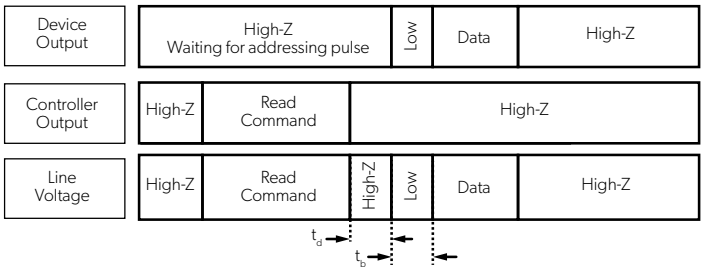

Figure 26: Manchester Read Response Timing

MANCHESTER CRC

The Manchester serial interface uses a cyclic redundancy check (CRC) for data-bit error checking (synchronization bits are ignored by the check). The CRC algorithm is based on the following polynomial and the CRC calculation is represented graphically in Figure 27. The trailing 3 bits of a message frame comprise the CRC token. The CRC is initialized at 0b111.

$$g(x) = x^3 + x + 1$$

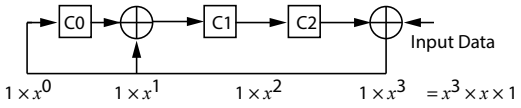

Figure 27: Manchester CRC Calculation

The 3-bit Manchester CRC can be calculated using the following C code:

```
// command: the Manchester command, right justified, does
not include the space for the CRC
// numberOfBits: number of bits in the command not includ-
ing the 2 zero sync bits at the start of the command and the
three CRC bits
// Returns: The three bit CRC
// This code can be tested at http://codepad.org/yqTKnfmD

uint16_t ManchesterCRC(uint64_t data, uint16_t numberOfBits)
{
	bool C0 = false;
	bool C1 = false;
	bool C2 = false;
	bool C0p = true;
	bool C1p = true;
	bool C2p = true;
	uint64_t bitMask = 1;

	bitMask <<= numberOfBits - 1;

	// Calculate the state machine
	for (; bitMask != 0; bitMask >>= 1)
	{
		C2 = C1p;
		C0 = C2p ^ ((data & bitMask) != 0);
		C1 = C0 ^ C0p;

		C0p = C0;
		C1p = C1;
		C2p = C2;
	}

	return (C2 ? 4U : 0U) + (C1 ? 2U : 0U) + (C0 ? 1U : 0U);
}
```


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DEFAULT MANCHESTER DRIVE OPERATION

When in Manchester mode, the device communicates via an open-drain driver. This applies even when the device has been configured with push/pull or assisted SENT/PWM.

ENTERING MANCHESTER COMMUNICATION MODE

The method of Manchester entry is determined by the PWM/SENT configuration of the IC. The specific entry requirements are controlled by OUTMSG_MODE (extended: 0x25 [2:0]) and SENT_PWM_RATE (extended 0x25: [7:3]) EEPROM fields.

1. If the IC is configured for PWM (OUTMSG_MODE = 0), the output line must be held low for at least 2 PWM periods prior to sending the Manchester entry code (as shown in Figure 27)
2. If using a form of free-streaming or Triggered SENT (OUTMSG_MODE = 1, 2, 6, or 7) the SENT frame must be interrupted by an Auxiliary Interrupt Pulse followed by the Manchester entry code (as shown in Figure 28 and Figure 29).
3. If using a version of Shared SENT (OUTMSG_MODE = 3, 4, OR 5), a specific F_AUX pulse is required, followed by the Manchester entry code (Figure 30).

A summary is shown in Table 6.

The method of entry is independent of the PWM_SENT_ENABLE (extended: 0x3F [17]) setting.

IMPORTANT: With the PWM/SENT output disabled (PWM_SENT_ENABLE = 0), the entry method is still defined by the settings of OUTMSG_MODE and SENT_PWM_RATE.

The A33022 is shipped with the following configurations set by the Allegro factory:

- PWM_SENT_ENABLE = 0
- OUTMSG_MODE = 0
- SENT_PWM_RATE = 0

Table 6: Auxiliary Command Parameters [1]

Parameter	Symbol	Description		Min	Typ.	Max	Units
Hold Time	t_{hold}	PWM	Auxiliary Command	2 × PWM period	–	–	µs
		SSENT—Short	F_AUX	56	63	70	ticks
		SSENT—Long	F_AUX	216	240	264	ticks
		ASENT	F_AUX	56	63	70	ticks
		SENT	Aux. Interrupt Pulse	30	–	–	ticks
		TSENT	Aux. Interrupt Pulse	30	–	–	ticks
Edge Detection Time	t_{gate}			0.7	–	–	µs
Access Code Window	t_{msgRX}			1.4	–	300	µs

[1] Parameter is not measured at final test. Determined by design.

Table 7: Manchester Access Code

Parameter	Description	Value (Hex)
Manchester Access Code	Enables Manchester Communication. PWM output disabled. Enables Extended Reads/Writes.	C4 18 0E 81

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Manchester Auxiliary Interrupt Pulse for PWM Output Mode

To initialize communication using the Manchester Auxiliary command when the A33022 is configured with PWM output, the auxiliary interrupt pulse can be applied at any time. The auxiliary pulse must have a minimum width of t_{HOLD}, after which the pulse is released for t_{GATE} plus the rise time to allow the line to pull high and the device to register a rising edge. After this, the controller must pull low for t_{GATE} before beginning to send the Manchester access code. If the device does not recognize the first rising edge of the Manchester access code before t_{msgRX}, after the hold time, a timeout of the device occurs, Manchester initialization aborts, and PWM functionality returns. The Manchester Auxiliary command for PWM output is shown in Figure 28.

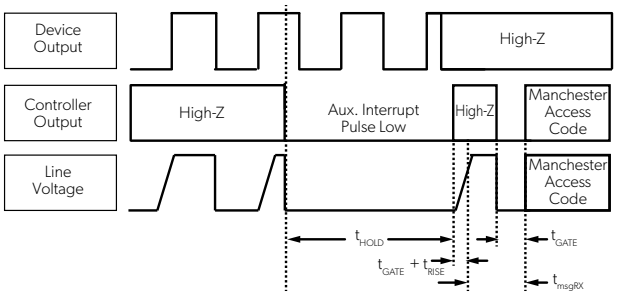

Figure 28: Entering Manchester from PWM

Manchester Auxiliary Command for SENT Output Mode

To initialize communication using the Manchester auxiliary command when the A33022 is configured with free-streaming SENT (OUTMSG_MODE = 1 or 7), the auxiliary interrupt pulse can begin at any time. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to pull high, followed by a low period of t_{GATE} before sending the Manchester access code. If the first rising edge of the Manchester access code is not observed before t_{msgRX}, a timeout of the the device occurs, Manchester initialization aborts, and the device returns to normal functionality. The Manchester auxiliary command is shown in Figure 29.

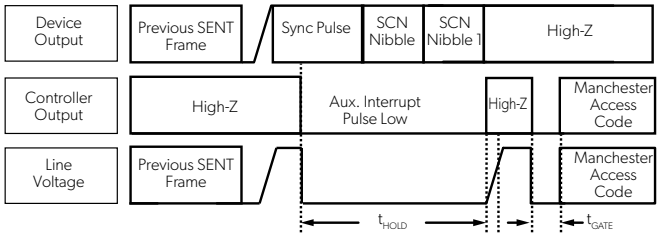

Figure 29: Entering Manchester using SENT

Manchester Auxiliary Command for TSENT Output Mode

To initiate Manchester communication when the A33022 is configured with the TSENT output (OUTMSG_MODE = 2 or 6), the auxiliary interrupt pulse must be transmitted during the SENT message frame, requiring a trigger pulse to begin a SENT frame. The auxiliary interrupt pulse must begin between 8 and 56 ticks following the completion of the trigger pulse. The pulse must have a minimum width of t_{HOLD}, after which the pulse must be released for t_{GATE} plus the rise time to allow the line to return high, followed by a low period of t_{GATE} before sending the Manchester access code. If the first rising edge of the Manchester access code is not observed before t_{msgRX}, a timeout of the device occurs, Manchester initiation aborts, and the device returns to normal functionality. The Manchester Auxiliary command is shown in Figure 30.

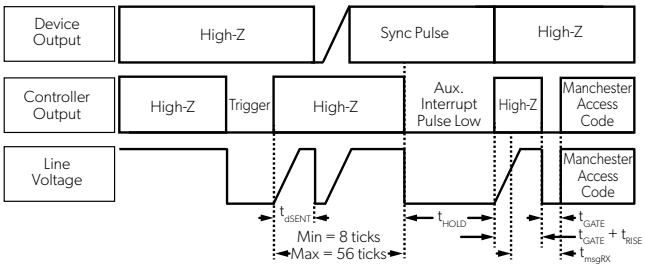

Figure 30: Entering Manchester using TSENT

Manchester Auxiliary Command for Shared SENT (SSENT and ASENT)

To initialize communication using the Manchester Auxiliary command when the A33022 is configured with SSENT or ASENT output, the auxiliary function pulse, F_AUX, is applied as the frame request pulse. The auxiliary pulse must have a minimum width of t_{HOLD}. After the pulse is released, the output line is required to go high-Z for t_{GATE} plus the rise time. The controller must then pull the output line low for t_{GATE} before sending the Manchester access code. If the first rising edge of the access code is not recognized before t_{msgRX}, a timeout occurs, the Manchester initialization aborts, and the output returns to normal functionality.

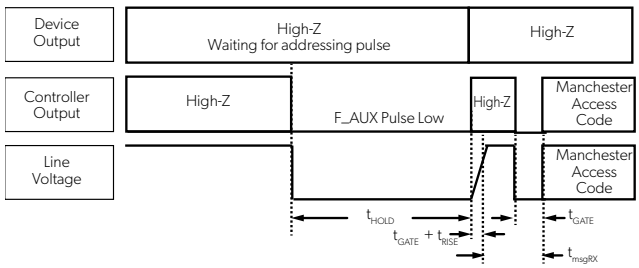

Figure 31: Entering Manchester using Shared SENT

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SENT INTERFACE

SENT Output

The A33022 features a SENT output conforming to the SENT data transmission specification SAEJ716 JAN2016.

Message Structure

Data within a SENT message frame is represented as a series of nibbles, with the following characteristics:

- Each nibble is an ordered pair of a low-voltage interval followed by a high-voltage interval.
- The low-voltage interval acts as the delimiting state, which acts as a boundary between each nibble. The length of this low-voltage interval is fixed at five ticks.
- The high-voltage interval performs the job of the information state and is variable in duration in order to contain the data payload of the nibble.
- The slew rate of the rising and falling edge may be adjusted using the PWM_SENT_HS_DRV_SEL and PWM_SENT_LS_DRV_SEL parameters.
  - High side (rising edge control) requires setting the PUSH_DRIVE field.

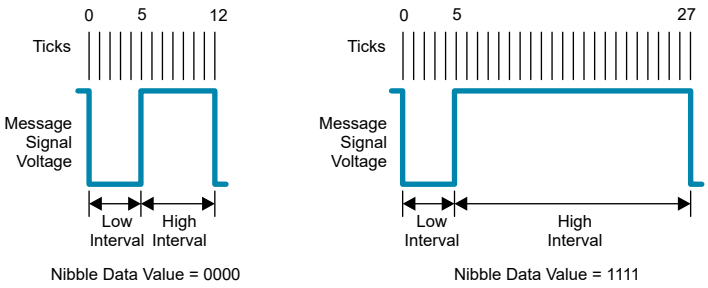

Figure 32: General Value Formation for SENT 0000 (left), 1111 (right)

The duration of a nibble is denominated in ticks. The period of a tick is set by the SENT_PWM_RATE EEPROM field. The duration of the nibble is the sum of the low-voltage interval plus the high-voltage interval.

The parts of a SENT message are arranged in the following required sequence:

1. **Synchronization and Calibration:** Flags the start of the SENT message.
2. **Status and Communication Nibble:** Provides the status of the A33022 and the optional serial data determined by the setting of the SENT_SCN_CFG parameter.
3. **Data:** Angle information and optional data.
4. **CRC:** Error checking.
5. **Pause Pulse (optional):** Fill pulse between SENT message frames.

Table 8: Nibble Composition and Value

Quantity of Ticks			Binary (4-bit) Value	Decimal Equivalent Value
Low-Voltage Interval	High-Voltage Interval	Total		
5	7	12	0000	0
5	8	13	0001	1
5	9	14	0010	2
⋮	⋮	⋮	⋮	⋮
5	21	26	1110	14
5	22	27	1111	15

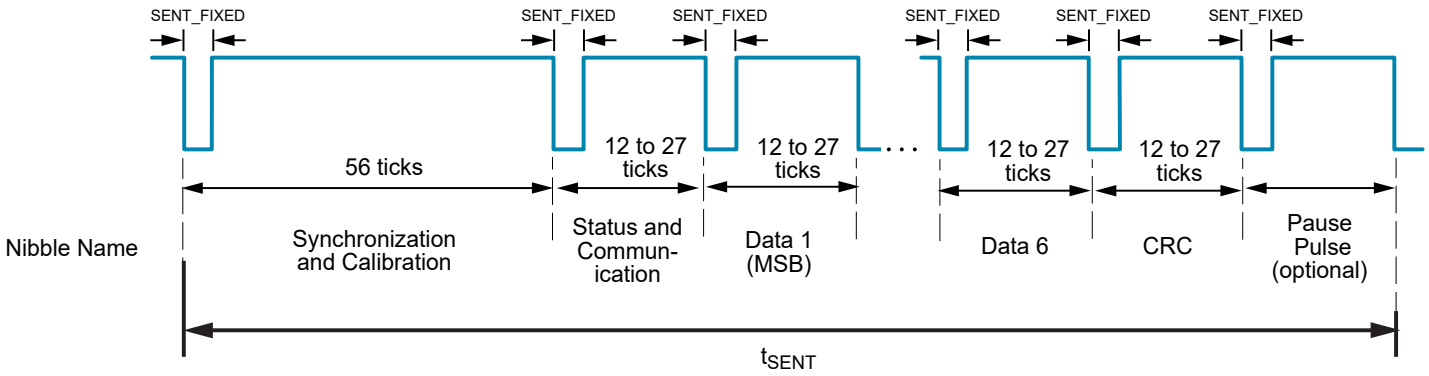

Figure 33: General Format for SENT Message Frame

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SENT Specifications

DATA FRAME CONTENTS

Contents of SENT packets are configurable, as controlled by the SENT_DATA_CFG field in EEPROM.

SENT_DATA_CFG	NIBBLE 1	NIBBLE 2	NIBBLE 3	NIBBLE 4	NIBBLE 5	NIBBLE 6
0	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	NA	NA	NA
1	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	NA	NA
2	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [15:12]	STATUS [11:8]	COUNT [3:0]
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [7:4]	STATUS [3:0]	COUNT [3:0]
3	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	DATAID[3:0]	EXDATA [7:4]	EXDATA [3:0]
4	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [7:4]	COUNT [3:0]	~MAIN_ANGLE [15:12]
5	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]
6	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	NA	NA
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	COUNT [3:0]	NA	NA
7	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [15:12]	STATUS [11:8]	COUNT [3:0]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	STATUS [7:4]	STATUS [3:0]	COUNT [3:0]
8	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	ID	NA	NA
9	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	ID	NA
10	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [15:12]	COUNT [3:0]	ID
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [11:8]	COUNT [3:0]	ID
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [7:4]	COUNT [3:0]	ID
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [3:0]	COUNT [3:0]	ID
11	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [15:12]	STATUS [11:8]	{1'B0,ID[2:0]}
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	STATUS [7:4]	STATUS [3:0]	{1'B1,ID[2:0]}
12	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	DATAID[3:0]	EXDATA [3:0]	ID
13	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	~MAIN_ANGLE [15:12]	ID
14	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	ID	NA
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	COUNT [3:0]	ID	NA
15	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [7:4]	COUNT [3:0]	~MAIN_ANGLE [15:12]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	COUNT [7:4]	COUNT [3:0]	~DIAG_ANGLE [15:12]
16	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	~MAIN_ANGLE [7:4]	~MAIN_ANGLE [11:8]	~MAIN_ANGLE [15:12]
17	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	COUNT [3:0]	~MAIN_ANGLE [11:8]	~MAIN_ANGLE [15:12]
18	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	NA	NA
19	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	NA
20	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [15:12]	COUNT [3:0]
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [11:8]	COUNT [3:0]
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [7:4]	COUNT [3:0]
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [3:0]	COUNT [3:0]

Continued on next page...

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SENT Specifications (continued)

SENT_DATA_CFG	NIBBLE 1	NIBBLE 2	NIBBLE 3	NIBBLE 4	NIBBLE 5	NIBBLE 6
21	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [15:12]	{2'B00,ID[1:0]}
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [11:8]	{2'B01,ID[1:0]}
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [7:4]	{2'B10,ID[1:0]}
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [3:0]	{2'B11,ID[1:0]}
22	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	DATAID[3:0]	EXDATA [3:0]
23	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	~MAIN_ANGLE [15:12]
24	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	NA
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	COUNT [3:0]	NA
25	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [15:12]	COUNT [3:0]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	STATUS [11:8]	COUNT [3:0]
	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	STATUS [7:4]	COUNT [3:0]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	STATUS [3:0]	COUNT [3:0]
26	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	ID	NA
27	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	ID
28	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	ID
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	COUNT [3:0]	ID
29	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	COUNT [3:0]	~MAIN_ANGLE [15:12]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	COUNT [3:0]	~DIAG_ANGLE [15:12]
30	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	{COUNT [2:0],CRC2 [4]}	CRC2 [3:0]
31	MAIN_ANGLE [15:12]	MAIN_ANGLE [11:8]	MAIN_ANGLE [7:4]	MAIN_ANGLE [3:0]	{COUNT [2:0],CRC2 [4]}	CRC2 [3:0]
	DIAG_ANGLE [15:12]	DIAG_ANGLE [11:8]	DIAG_ANGLE [7:4]	DIAG_ANGLE [3:0]	{COUNT [2:0],CRC2 [4]}	CRC2 [3:0]

ID NIBBLE

The ID nibble is defined as shown in Table 9.

Table 9: ID Nibble

ID Nibble			
3	**2**	**1**	**0**
0	0	ID [1]	ID [0]

The ID values communicate the logic states of SA0 and SA1 pins. The upper 2 bits can be replaced with a 2-bit counter, depending on the SENT DATA_MODE.

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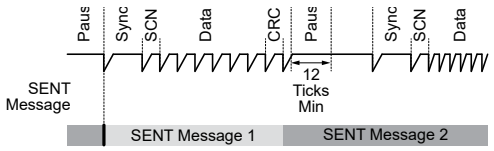
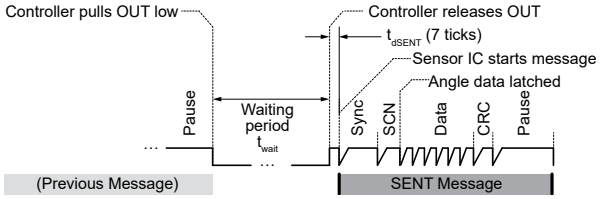
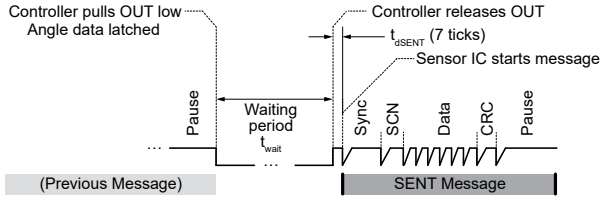
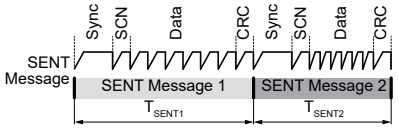
SENT Output Modes

The timing and method of SENT transmission may be configured using the outmsg_mode field within EEPROM. Methods of SENT transmission are shown in Table 10 and SENT output modes are shown in Table 11.

Table 10: Methods of SENT Transmission

Free-Streaming SENT	• Angle information is automatically placed on the SENT line with no prompting from the host. Depending on settings, the SENT message frames may be transmitted back-to-back or synchronized with the angle update. • OUTMSG_MODE = 1 and 7 are examples of free-streaming SENT.
Triggered SENT (TSENT)	• A SENT message frame occurs only when initiated by the host. Prior to the trigger, the A33022 outputs a continuous pause pulse, during which the host triggers a SENT frame by pulling the SENT line low for a minimum of $T_{Trig(MIN)}$. Once the SENT line is released by the host, the A33022 responds with a SENT message frame. • OUTMSG_MODE = 2 and 6 are examples of triggered SENT.
Shared SENT	• Two distinct formats—sequential SENT (SSENT) and addressable SENT (ASENT). Shared SENT allows sharing a single SENT line among four comtpatible devices. • OUTMSG_MODE = 3, 4, and 5 are examples of shared SENT.

Table 11: SENT Output Modes (outmsg_mode EEPROM Field)

Code	Visual	Description
0	–	• SENT Disabled. PWM enabled.
1		• Internally synchronized SENT (ISENT). Free-streaming SENT synchronized to the angle update. • A pause pulse is inserted until fresh data becomes available. The pause pulse has a minimum length of 12 ticks between SENT messages. • Angle data is sampled near the end of the status and communication nibble (SCN).
2		• Triggered SENT (TSENT). • Data is latched near the end of SCN. • Controller initiates a SENT transmission by pulling the line low during the pause pulse. After the controller releases the output, and after a delay of t_{dSENT}, the SENT message begins.
3	–	• Sequential SENT—Long. • See Shared SENT section (to be added later).
4	–	• Sequential SENT. • See Shared SENT section (to be added later).
5	–	• Addressable SENT (ASENT). • See Shared SENT section (to be added later).
6		• TSENT. • Data is latched on the falling edge of the trigger. • Similar to OUTMSG_MODE = 2, except angle data is latched once the output line is pulled low.
7		• Free-streaming SENT. No pause pulse.

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EEPROM AND SHADOW MEMORY USAGE

The A33022 device features include integrated EEPROM to permanently store configuration parameters for operation. EEPROM is customer programmable and retains data, or parameter values, to configure the device for the application requirements. After a reset or EEPROM write operation, parameter data is copied from EEPROM to shadow (volatile) memory. Parameter data in shadow memory can be overwritten by performing an extended write to the shadow addresses. Access of device parameters through shadow memory is faster than access through EEPROM. In situations where it is desired to test many parameters quickly before permanently programming, use of shadow memory is recommended. The shadow memory registers have the same format as EEPROM and are accessed at extended addresses 0x40 higher than the equivalent EEPROM address. Some bits do not impact device operation and are not copied into shadow memory. Shadow registers do not contain the ECC bits and may have read or write protection restrictions similar to EEPROM.

Enabling EEPROM Access

Writes to indirect memory, EEPROM, and shadow memory are restricted and require an unlock code (reading is allowed without unlocking the device). The unlock code is written to the primary serial register access (primary: 0x1E [15:0]). This involves two write commands, which should be executed one after the other:

For SPI communication:
Write 0xC418 to register primary 0x1E [15:0].
Write 0x0E80 to register primary 0x1E [15:0].
For Manchester communication:
Write 0xC418 to register primary 0x1E [15:0].
Write 0x0E81 to register primary 0x1E [15:0].

When the communication enable bit, MANCH_COMM_E (extended 0xA5 [15]), is written with logic = 0, or when a reset event occurs, the communications mode is disabled.

The access status is indicated by the direct serial register access. A read of primary 0x1E [1] set to logic = 1 indicates the customer unlock code is set.

The customer unlock code is not required for write and read operations to all direct serial registers.

Following an EEPROM write, EEPROM margin checking should be performed. The device must be unlocked when performing margin checks.

EEPROM and Shadow Access Protections

The A33022 contains features to protect against unwanted EEPROM access.

- Setting the EEPROM parameter MEM_LOCK (extended: 0x24 [21:18]) to a value of 0xC (1100 binary) restricts write access to prevent changes to the EEPROM registers. Temporary changes to device configuration settings are still possible by writing to the indirect volatile and shadow memory. Note, any changes to the indirect volatile memory are reset after a device reset event. Read access of the EEPROM is still possible.
- Setting the EEPROM parameter MEM_LOCK (extended: 0x24 [21:18]) to a value of 0x3 (0011 binary) restricts write access to prevent changes to EEPROM, indirect volatile, and shadow memory. Once set, the parameter settings in indirect memory are read only. Read access is still possible.
- Writes to MEM_LOCK with the above values are one-time access only and are not erasable through subsequent write commands.

Write Transactions to Extended Memory: EEPROM, Shadow, and Volatile

Invoking an extended write access is a three-step process:

1. Write the target extended address to the primary register INDIRECT_WR_ADDRESS (primary: 0x1 [7:0]).
2. Write the desired data, for the target extended register, to the primary registers INDIRECT_WR_DATA_MSB (primary: 0x2 [15:0]) and INDIRECT_WR_DATA_LSB (primary: 0x3 [15:0]). The register INDIRECT_WR_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_WR_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.
3. Execute the extended memory write by setting the extended memory execute write bit (EXW; primary: 0x4 [15]), to logic = 1.
    a. EEPROM writes require ≈ 6.5 ms to complete.

When EXW is set, the 32 bits of data contained in INDIRECT_WR_DATA_LSB and INDIRECT_WR_DATA_LSB are written to the indirect memory address specified by INDIRECT_WR_ADDRESS. The status of the write operation may be interrogated by polling the primary register INDIRECT_WR_STATUS (primary: 0x4). The write-in-progress bit (WIP; primary: 0x4 [8]), when set, indicates the write transaction in progress. The write operation done bit (WDN; primary: 0x4 [0]), when set, indicates the write transaction is done or complete. The extended execute error status bit (XEE; primary: 0x0F [14]), when set, indicates an error occurred when executing the write. For example, if a write is attempted without the proper access enabled, XEE indicates an error.

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Read Transaction from EEPROM and Other Extended Locations

Extended access is provided to additional memory space via the direct registers. This access includes the EEPROM and EEPROM shadow registers. All extended registers are up to 32 bits wide. Invoking an extended read access is a three-step process:

1. Write the extended address to be read into the INDIRECT_RD_ADDRESS (primary: 0x5) register (using SPI or Manchester direct access). The 8-bit extended address that determines which extended memory address to access is INDIRECT_RD_ADDRESS.
2. Invoke the extended access by writing the extended read bit (EXR; primary: 0x6 [15]) with a value of 1. The address specified in INDIRECT_RD_ADDRESS is then read, and the data is loaded into the registers INDIRECT_RD_DATA_MSB (primary: 0x7) and INDIRECT_RD_DATA_LSB (primary: 0x8).
3. Read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB (using SPI or Manchester direct access) to get the full data contents of the extended read address. The register INDIRECT_RD_DATA_LSB corresponds to the data bits [15:0] of the target extended memory address. The register INDIRECT_RD_DATA_MSB corresponds to the data bits [31:16] of the target extended memory address.

EEPROM read accesses may take up to 2 µs to complete. The read operation done bit (RDN; primary: 0x6 [0]) can be polled to determine if the read access is complete before reading the data. Shadow register reads complete in one system clock cycle after synchronization. Do not attempt to read the registers INDIRECT_RD_DATA_MSB and INDIRECT_RD_DATA_LSB if the read access is in process (RIP; primary: 0x6 [8] = 1), as it could change during the serial access, which would result in inconsistent data. It is also possible that an SPI CRC error would be detected if the data were to change during the serial read via the SPI interface.

Shadow Memory Read and Write Transactions

Shadow memory read and write transactions are identical to those for EEPROM. Instead of addressing to the EEPROM extended address, the shadow extended addresses must be addressed. Shadow extended addresses are located at an offset of 0x40 above the EEPROM. For all addresses, refer to the EEPROM section, Table 12 and Table 13.

EEPROM Margin Check

The A33022 contains a test mode, EEPROM margining, to check the logic levels of the EEPROM bits. EEPROM margining is customer accessible. EEPROM margining is selectable to check all logic = 1 values, logic = 0 values, or both. The results of the test are reported back in extended memory registers 0x85, 0x83, and 0x82. Note that a fail of the margin test does not force the outputs to a diagnostic state or trigger a diagnostic error flag. The following is a step-by-step procedure to verify EEPROM programming:

1. Enable EEPROM access by sending the unlock code to primary address 0x1E
2. Write a 1 to the MARGIN_START field (volatile 0x85 [0])
   a. Once started the device will automatically check high/low thresholds for all EEPROM addresses.
3. Read MARGIN_STATUS (volatile 0x85 [4:3])
   0 = No result from margin testing (margin testing not run)
   1 = Pass. Margin checking completed with no errors.
   2 = Failure detected during margin testing
   3 = Running. Margin testing is still running.
4. If a margin failure is detected additional information can be retrieved.
   MARGIN_MIN_MAX_FAIL [volatile 0x85 [5]
   0 = Margin low threshold failure
   1 = Margin high threshold failure
   EE_ADDR [volatile 0x82 [12:7] contains the failing address.

5. EEPROM should not be considered valid unless margin testing passes. If the margin failure occurs on a previously modified address space, EEPROM can be rewritten and margin checking repeated in an attempt to clear the issue.

For more information about EEPROM margining, refer to the Volatile Memory section (addresses 0x82, 0x83, and 0x85). Time required to verify margin levels across all EEPROM is ≈100 µs

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PRIMARY SERIAL INTERFACE REGISTER REFERENCE

Table 12: Direct Serial Interface Registers Bits Map

Address	Access	Name	Upper Byte (MSB)								Lower Byte (LSB)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	RO	NULL_REG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1	RW	INDIRECT_WR_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
0x2	RW	INDIRECT_WR_DATA_MSB	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
0x3	RW	INDIRECT_WR_DATA_LSB	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
0x4	WO/RO	INDIRECT_WR_STATUS	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
0x5	RW	INDIRECT_RD_ADDRESS	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							
0x6	WO/RO	INDIRECT_RD_STATUS	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
0x7	RO	INDIRECT_RD_DATA_MSB	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
0x8	RO	INDIRECT_RD_DATA_LSB	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
0x9	RO	HP_A_REG	HP_A															
0xa	RO	HP_B_REG	HP_B															
0xb	RO	HP_C_REG	HP_C															
0xc	RO/RC	STATUS_REG	0	0	0	R	R	R	ECC_ SELF_ TEST_ FAILED_ FLAG	0	POKS_ SELF_ TEST_ FAILED_ FLAG	MASK_ ACTIVE	R	0	0	0	0	0	ANG_RDY
0xd	RW	CTRL	0	0	0	0	0	0	0	0	0	0	0	0	FULL_ RST	SOFT_ RST	R	R
0xe	RO	MAIN_ANGLE	ANGLE_OUT_MAIN															
0xf	RO/RC	ERROR	IER	XEE	BSY	SME	EUE	ESE	POR	OVCC	UVCC	MSH	MSL	SMM	OFE	SAT	TSE	VCF
0x10	RO	TEMP12B_P	0	0	0	0	TEMP_OUT_P											
0x11	RO	TEMP12B_S	0	0	0	0	TEMP_OUT_S											
0x12	RO	FIELD_REG	FIELD_MAG															
0x13	RO	ANGLE_DIAG_AB	ANGLE_OUT_AB															
0x14	RO	ANGLE_DIAG_BC	ANGLE_OUT_BC															
0x15	RO	ANGLE_DIAG_CA	ANGLE_OUT_CA															
0x16	Ro	ANGLE_DIAG_LATCH	ANGLE_OUT_DIAG_LATCH															
0x1e	WO/RO	ACCESS	RESERVED														CUSTOMER_ACCESS	FACTORY_ACCESS
0x1f	RW	LOOPBACK_REG	LOOPBACK															

RO: Read only | WO: Write only | RW: Read and write | RC: Read and bit clears after read (if condition has cleared)

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Address 0x00 (NOP) Null Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Address 0x01 (INDIRECT_WR_ADDRESS) Extended Write Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_WR_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_ADDR [7:0]:
Target address to be used for an extended memory write. Address ranges:

- 0x00 through 0x3F: EEPROM (requires ≈6.5 ms following execution of a write)
- 0x40 through 0x7F: Shadow (Volatile)
- 0x80 through 0xAA: Miscellaneous (Volatile)

Address 0x02 (INDIRECT_WR_DATA_MSB) Extended Write Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_3								INDIRECT_WR_DATA_2							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_3 [15:8]:
Fourth (upper) byte of data for an extended write operation. Corresponds to bit [31:24] of the extended write address.

INDIRECT_WR_DATA_2 [7:0]:
Third byte of data for an extended write operation. Corresponds to bit [23:16] of the extended write address.

Address 0x03 (INDIRECT_WR_DATA_LSB) Extended Write Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_WR_DATA_1								INDIRECT_WR_DATA_0							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_WR_DATA_1 [15:8]:
Second byte of data for an extended write operation. Corresponds to bit [15:8] of the extended write address.

INDIRECT_WR_DATA_0 [7:0]:
First (lower) byte of data for an extended write operation. Corresponds to bit [7:0] of the extended write address.

Address 0x04 (INDIRECT_WR_STATUS) Extended Write Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXW	0	0	0	0	0	0	WIP	0	0	0	0	0	0	0	WDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXW [15]:
Initial extended write by writing "1". Sets WIP. Clears WDN. Write-only, always reads back "0".

WIP [8]:
When logic = 1, a write operation is in progress.

WDN [0]:
When logic = 1, a write operation is complete. Clears when EXW is set to logic = 1.

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Address 0x05 (INDIRECT_RD_ADDRESS) Extended Read Address

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	INDIRECT_RD_ADDR							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW

INDIRECT_RD_ADDR [7:0]:
Address to be used for an extended read. Address ranges:

- 0x00 through 0x3F: EEPROM (requires ≈ 2 µs)
- 0x40 through 0x7F: Shadow (Volatile)
- 0x80 through 0xAA: Miscellaneous (Volatile)

Address 0x06 (INDIRECT_RD_STATUS) Extended Read Control and Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXR	0	0	0	0	0	0	RIP	0	0	0	0	0	0	0	RDN
Access	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EXR [15]:
Initial extended read by writing 1. Sets RIP. Clears RDN. Write-only, always reads back 0.

RIP [8]:
When logic = 1, a read operation is in progress.

RDN [0]:
When logic = 1, a read operation is complete. Clears when EXR is set to logic = 1.

Address 0x07 (INDIRECT_RD_DATA_MSB) Extended Read Data Bytes High

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_3								INDIRECT_RD_DATA_2							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

INDIRECT_RD_DATA_3 [15:8]:
Fourth (upper) byte of data for an extended read operation. Corresponds to bit [31:24] of the extended read address, after execution of a read operation.

INDIRECT_RD_DATA_2 [7:0]:
Third byte of data for an extended read operation. Corresponds to bit [23:16] of the extended read address, after execution of a read operation.

Address 0x08 (INDIRECT_RD_DATA_LSB) Extended Read Data Bytes Low

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INDIRECT_RD_DATA_1								INDIRECT_RD_DATA_0							
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Contains the lower 16 bits of data following an indirect read operation (such as an EEPROM read). Also stores previous contents of the error register (0x0F) following a read of that register.

INDIRECT_RD_DATA_1 [15:8]:
Second byte of data for an extended read operation. Corresponds to bit [15:8] of the extended read address, after execution of a read operation.

INDIRECT_RD_DATA_0 [7:0]:
First (lower) byte of data for an extended read operation. Corresponds to bit [7:0] of the extended read address, after execution of a read operation.

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Address 0x09 (HP_A_REG) Channel A Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HP_A															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

HP_A [15:0]:
The full differential field (in gauss) seen by the channel can be calculated as:

Differential Field (G) = Channel_Reading/S

where S = 23 LSB/G for part numbers with suffix 300 and S = 15.5 for part numbers with suffix 600.

The returned gauss value is indicative only.

Address 0x0A (HP_B_REG) Channel B Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HP_B															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

HP_B [15:0]:
The full differential field (in gauss) seen by the channel can be calculated as:

Differential Field (G) = Channel_Reading/S

where S = 23 LSB/G for part numbers with suffix 300 and S = 15.5 for part numbers with suffix 600.

The returned gauss value is indicative only.

Address 0x0B (HP_C_REG) Channel C Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	HP_C															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

HP_C [15:0]:
The full differential field (in gauss) seen by the channel can be calculated as:

Differential Field (G) = Channel_Reading/S

where S = 23 LSB/G for part numbers with suffix 300 and S = 15.5 for part numbers with suffix 600.

The returned gauss value is indicative only.

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Address 0x0C (STATUS_REG) Device Status Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	R	R	R	ECC_ SELF_ TEST_ FAILED_ FLAG	0	POKS_ SELF_ TEST_ FAILED_ FLAG	MASK_ ACTIVE	R	0	0	0	0	ANG_ RDY
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RC	RC	RC	RO	RO

Reserved [12] [11] [10] [5]:
Reserved bits. No function.

ECC_SELF_TEST_FAILED_FLAG [9]:
Indicates the error corrector code (ECC) self-test failed. ECC self-test checks the ECC mechanism of the EEPROM memory system.

POKS_SELF_TEST_FAILED_FLAG [7]:
Indicates power OK/current OK self-test (POKs/IOKs) failed.

MASK_ACTIVE [6]:
Indicates that at least one fault masking bit is active.

ANG_RDY [0]:
Angle ready informational flag: This flag is set when the first angle calculated in the MAIN, AB, BC, and CA paths are ready.

Address 0x0D (CTRL) Control Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	FULL_ RST	SOFT_ RST	R	R
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW

FULL_RST [3]:
Full reset. When FULL_RST = 1, a full reset of the device logic is triggered, including a full load of the EEPROM, reset of all the status and error registers, reset of the signal processing, the reset of the outputs and communications protocols (with the exception of SPI), and reset of the main controller. This function includes all functions performed in SOFT_RST. After the reset is complete, the power-on reset flag (POR; primary: 0xF [9]) is asserted. A full reset will not reset the status of the access code (If the device has been unlocked, the unlock code is not required to be sent following a full reset).

SOFT_RST [2]:
Soft Reset. When SOFT_RST = 1, a full reset of the device logic is triggered, including reset of all the status and error registers, reset of the signal processing, and reset of the outputs and communications protocols (with the exception of SPI). After the reset is complete, the POR flag (primary: 0xF [9]) is asserted.

Reserved [1:0]:
Reserved bits. No function.

Address 0x0E (MAIN_ANGLE) Main Angle Output

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_MAIN															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE_OUT_MAIN [15:0]:
Register indicates the calculated angle from the three differential channels δ_{MAIN}. The parameter is a 16-bit unsigned integer with value of ANGLE_OUT_MAIN × $360/2^{16}$ in degrees. A read of this register latches the data in ANGLE_OUT_DIAG_LATCH (primary: 0x16 [15:0]).

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Address 0x0F (ERROR) Device Error Flags

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IER	XEE	BSY	SME	EUE	ESE	POR	OVCC	UVCC	MSH	MSL	SMM	OFE	SAT	TSE	VCF
Access	RC	RC	RC	RO	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC	RC

Error register, flags clear on read. All flags latch, meaning they remain high until cleared. Following a read, previous contents of the error register are stored in address 0x08 (INDIRECT_RD_DATA_LSB). This allows data to be retrieved if lost during transmission.

IER [15]:
Interface error. Invalid SPI packet detected. Packet was discarded. Also indicates an error in the Manchester communication.

Value	Description
0	No interface error
1	Interface error

XEE [14]:
Extended execute error. A command initiated by an extended write failed. Write failed due to access error (not unlocked) or EEPROM write failure.

Value	Description
0	No incoming extended error
1	Extended execute error

BSY [13]:
Extended access overflow. An extended write or extended read was initiated before the previous operation was complete.

Value	Description
0	No extended access error
1	Extended access error

SME [12]:
Shadow memory error. Indicates detection of a multiple-input signature request (MISR) error in the shadow memory. This error requires a reset to clear.

Value	Description
0	No shadow memory error
1	Shadow memory error

EUE [11]:
EEPROM uncorrectable error. A multi-bit EEPROM read error occurred. EEPROM bit errors are only checked on EEPROM load (i.e., power-on or reset). A reset is required to clear this error and for the condition to no longer be present.

Value	Description
0	No multi-bit EEPROM error
1	Multi-bit EEPROM error

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ESE [10]:
EEPROM soft error. A correctable (single-bit) EEPROM read occurred. EEPROM bit errors are only checked on EEPROM load (power-on or reset). Single-bit errors are detected and corrected in shadow memory using the Hamming ECC.

Value	Description
0	No single-bit EEPROM error
1	EEPROM single-bit error

POR [9]:
Reset condition. Indicates a reset event or EEPROM load has occurred.

Value	Description
0	No reset
1	Device has been reset. Volatile registers are reinitialized

OVCC [8]:
VCC overvoltage condition. Indicates an overvoltage condition on the supply pin VCC. Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No VCC overvoltage error
1	VCC overvoltage error

UVCC [7]:
VCC undervoltage condition. Indicates an undervoltage condition on the supply pin VCC. Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No VCC undervoltage error
1	VCC undervoltage error

MSH [6]:
Magnetic signal high fault. Indicates the magnitude of the magnetic input signal sensed is above the high-limit threshold. The high-limit threshold is set via EEPROM parameter MSH_THR (extended: 0x24 [2:0]).

The MSH_THR parameter is compared to FIELD_MAG (primary: 0x12 [15:0]). Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field high fault
1	Magnetic field above the high threshold, MSH_THR

MSL [5]:
Magnetic signal low fault. Indicates the magnitude of the magnetic input signal sensed is below the low-limit threshold. The low-limit threshold is set via EEPROM parameter MSL_THR (extended: 0x24 [5:3]).

The MSL_THR parameter is compared to FIELD_MAG (primary: 0x12 [15:0]). Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No magnetic field low fault
1	Magnetic field below the low threshold MSL_THR

SMM [4]:
Signal mismatch error. Indicates a mismatch between ANGLE_OUT_MAIN δ_{MAIN} and any of the diagnostic angles (ANGLE_OUT_AB δ_{AB}, ANGLE_OUT_BC δ_{BC}, or ANGLE_OUT_CA δ_{CA}). The angle mismatch threshold is set via EEPROM parameter ANGLE_MISMATCH (extended 0x24 [7:6]).

An error detected by this monitor continues to assert until the fault condition is removed (and the register is cleared).

The signal mismatch error also reports a built-in self-test (BIST) error. An error detected by this monitor requires a reset to clear.

Value	Description
0	No angle mismatch or error register BIST failure detected
1	Angle mismatch or error register BIST failure detected

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OFE [3]:
Oscillator frequency error. One of the oscillator watchdog circuits monitoring the high-frequency and low-frequency oscillators has detected a fault. Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No oscillator error
1	Oscillator watchdog error

SAT [2]:
Channel saturation flag. Indicates internal signals, including the inputs of the ADCs, saturated prior to the angle calculation. May indicate the magnetic input is outside of the specified range. Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	No saturation detected in the signal path
1	Saturation conditions detected within the channel signal path

TSE [1]:
Temperature sensor error. The primary or secondary temperature sensor calculated output is less than –60°C or greater than 170°C. Also reports when the calculated temperature output of the primary and secondary temperature sensors differs by more than 20°C. Continues to assert until the fault condition is removed (and the register is cleared).

Value	Description
0	Primary and secondary temperature sensors within range
1	Primary or secondary temperature sensor calculated output is less than –60°C or greater than 170°C, or the primary temperature sensor calculated output differs more than 20°C when compared to the secondary temperature sensor calculated output.

VCF [0]:
Voltage check fault. Indicates a failure of an internal reference voltage. Continues to assert until the fault condition is removed (and the register is cleared).

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Address 0x10 (TEMP12B_P) Primary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	TEMP_OUT_P											
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

TEMP_OUT_P [11:0]:
Current ambient temperature from the primary channel internal temperature sensor. Value is a 12-bit signed integer, where temperature [°C] ≈(temp_out_p/8) + 25.

Address 0x11 (TEMP12B_S) Secondary Channel Temperature Sensor Reading

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	TEMP_OUT_S											
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

TEMP_OUT_S [11:0]:
Current ambient temperature from the secondary channel internal temperature sensor. Value is a 12-bit signed integer, where temperature [°C] ≈(temp_out_s/8) + 25.

Address 0x12 (FIELD_REG) FIELD_MAG

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FIELD_MAG															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FIELD_MAG [15:0]:
Indicates the amplitude of the input magnetic flux density, B_{IN}. Value is a 16-bit unsigned integer.

The LSB read value is converted to gauss with $B_{IN}(G)$ = FIELD_MAG(LSB)/(S × 1.304 × 3), where S = 23 LSB/G for part numbers with suffix 300, and S = 15.5 LSB/G for part numbers with suffix 600. The returned gauss value is indicative only.

Address 0x13 (ANGLE_DIAG_AB) Diagnostic AB Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_AB															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE_OUT_AB [15:0]:
Angle output from channel AB δ_{AB}. The parameter is a 16-bit unsigned integer with a value of ANGLE_OUT_AB × $360/2^{16}$ in degrees.

Address 0x14 (ANGLE_DIAG_BC) Diagnostic BC Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_BC															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE_OUT_BC [15:0]:
Angle output from channel BC δ_{BC}. The parameter is a 16-bit unsigned integer with a value of ANGLE_OUT_BC × $360/2^{16}$ in degrees.

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Address 0x15 (ANGLE_DIAG_CA) Diagnostic CA Channel Angle Value (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_CA															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE_OUT_CA [15:0]:
Angle output from channel CA δ_{CA}. The parameter is a 16-bit unsigned integer with a value of ANGLE_OUT_CA × $360/2^{16}$ in degrees.

Address 0x16 (ANGLE_DIAG_LATCH) Latched Main Angle (16 bits)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ANGLE_OUT_DIAG_LATCH															
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ANGLE_OUT_DIAG_LATCH [15:0]:
Latched angle output from the selected redundant channel (AB, BC, or CA). Selectable channel with DIAG_CHANNEL_SEL (extended 0x3F [19:18]). The parameter is a 16-bit unsigned integer with a value of ANGLE_OUT_DIAG_LATCH × $360/2^{16}$ in degrees.

Address 0x1E (ACCESS) Access Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RESERVED														CUSTOMER_ACCESS	FACTORY_ACCESS
Access	WO	WO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

ACCESS_KEY [15:0]:
Writing to register 0x1E is a special command to enable access to the extended memory space, EEPROM, and volatile. For more information, see Enabling EEPROM Access.

CUSTOMER_ACCESS [1]:
Indicates state of access to customer registers within the extended memory space. If logic = 1, access to the customer registers within the extended memory space is enabled.

FACTORY_ACCESS [0]:
Indicates state of access to factory registers within the extended memory space. If logic = 1, access to the factory registers within the extended memory space is enabled.

Address 0x1F (LOOPBACK_REG) Loopback Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LOOPBACK															
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

LOOPBACK [15:0]:
Customer loopback register. The registers allow the external controller to perform a loopback test of the SPI communication between the controller and the peripheral A33022.

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Extended Memory Table

EEPROM (NONVOLATILE), SHADOW (VOLATILE), AND MISCELLANEOUS (VOLATILE)

The EEPROM/shadow register bitmap is shown below. All EEPROM and shadow contents can be read by the user, without unlocking. Writing requires a device unlock. The shadow memory is a copy of the EEPROM in the address range 0x40 through 0x7F.

Table 13: EEPROM/Shadow Memory Map

EEPROM Addr	Shadow Addr	31:26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0	N/A	ECC	Factory Reserved				Y_DIE_LOC								X_DIE_LOC								Factory Reserved					
0x1	N/A	ECC	Factory Reserved				FACTORY_LOT																FACTORY_WAFER					
0x2	N/A	ECC	CAS_ID																Factory Reserved									
0x3	N/A	ECC	EXTRA_1	EXTRA_0	UNUSED_3																							
0x4 to 0x23	N/A	Factory Reserved																										
0x24	0x64	ECC	UNUSED_24_B		MASK_4	EXTENDED_POK_IO_EN	MEM_LOCK				R	BLOCK_VOLATILE_OUTPUT	MAKE_ERRORS_HIGH_Z	PASSTHROUGH_EN	MASK_3	MASK_2	MASK_1	MASK_0	LPM_DIS_C	UNUSED_24_A	ANGLE_MISMATCH		MSL_THR		MSH_THR		
0x25	0x65	ECC	CFG_NO_SAMPLE		CFG_MAX_SENSOR		TRIGGER_CFG		CFG_ZERO_SAMPLE	CFG_SLOT_SYNC	CFG_SLOT_MARKING	CFG_POR_OFFLINE	CFG_IDLE_SYNC	SENT_CRC_CFG	SENT_SCN_CFG		SENT_DATA_CFG					SENT_PWM_RATE				OUTMSG_MODE		
0x26	0x66	ECC	UNUSED_26		AB_LINEARIZATION_2								AB_LINEARIZATION_1									AB_LINEARIZATION_0						
0x27	0x67	ECC	UNUSED_27		AB_LINEARIZATION_5								AB_LINEARIZATION_4									AB_LINEARIZATION_3						
0x28	0x68	ECC	UNUSED_28		AB_LINEARIZATION_8								AB_LINEARIZATION_7									AB_LINEARIZATION_6						
0x29	0x69	ECC	UNUSED_29		AB_LINEARIZATION_11								AB_LINEARIZATION_10									AB_LINEARIZATION_9						
0x2A	0x6A	ECC	UNUSED_2A		AB_LINEARIZATION_14								AB_LINEARIZATION_13									AB_LINEARIZATION_12						
0x2B	0x6B	ECC	UNUSED_2B					AB_LIN_EN	CUST_ANGLE_OFFSET													AB_LINEARIZATION_15						
0x2C	0x6C	ECC	UNUSED_2C		BC_LINEARIZATION_2								BC_LINEARIZATION_1									BC_LINEARIZATION_0						
0x2D	0x6D	ECC	UNUSED_2D		BC_LINEARIZATION_5								BC_LINEARIZATION_4									BC_LINEARIZATION_3						
0x2E	0x6E	ECC	UNUSED_2E		BC_LINEARIZATION_8								BC_LINEARIZATION_7									BC_LINEARIZATION_6						
0x2F	0x6F	ECC	UNUSED_2F		BC_LINEARIZATION_11								BC_LINEARIZATION_10									BC_LINEARIZATION_9						
0x30	0x70	ECC	UNUSED_30		BC_LINEARIZATION_14								BC_LINEARIZATION_13									BC_LINEARIZATION_12						
0x31	0x71	ECC	UNUSED_31																	BC_LIN_EN		BC_LINEARIZATION_15						
0x32	0x72	ECC	UNUSED_32		CA_LINEARIZATION_2								CA_LINEARIZATION_1									CA_LINEARIZATION_0						
0x33	0x73	ECC	UNUSED_33		CA_LINEARIZATION_5								CA_LINEARIZATION_4									CA_LINEARIZATION_3						
0x34	0x74	ECC	UNUSED_34		CA_LINEARIZATION_8								CA_LINEARIZATION_7									CA_LINEARIZATION_6						
0x35	0x75	ECC	UNUSED_35		CA_LINEARIZATION_11								CA_LINEARIZATION_10									CA_LINEARIZATION_9						
0x36	0x76	ECC	UNUSED_36		CA_LINEARIZATION_14								CA_LINEARIZATION_13									CA_LINEARIZATION_12						
0x37	0x77	ECC	UNUSED_37												IIR_BW_SEL			SPARE_CUST		CA_LIN_EN		CA_LINEARIZATION_15						
0x38	0x78	ECC	UNUSED_38		MAIN_LINEARIZATION_2								MAIN_LINEARIZATION_1									MAIN_LINEARIZATION_0						
0x39	0x79	ECC	UNUSED_39		MAIN_LINEARIZATION_5								MAIN_LINEARIZATION_4									MAIN_LINEARIZATION_3						
0x3A	0x7A	ECC	UNUSED_3A		MAIN_LINEARIZATION_8								MAIN_LINEARIZATION_7									MAIN_LINEARIZATION_6						
0x3B	0x7B	ECC	UNUSED_3B		MAIN_LINEARIZATION_11								MAIN_LINEARIZATION_10									MAIN_LINEARIZATION_9						
0x3C	0x7C	ECC	UNUSED_3C		MAIN_LINEARIZATION_14								MAIN_LINEARIZATION_13									MAIN_LINEARIZATION_12						
0x3D	0x7D	ECC	UNUSED_3D																ROT_DIR_P	MAIN_LIN_EN		MAIN_LINEARIZATION_15						
0x3E	0x7E	ECC	UNUSED_3E		CUSTOMER_ID																							
0x3F	0x7F	ECC	PWM_SENT_LS_DRV_SEL		PWM_SENT_HS_DRV_SEL		DIAG_CHANNEL_SEL		PWM_SENT_ENABLE	0	0	0	PWM_PORCH_SEL				0		IDLE_PUSH	PUSH_DRIVE		D_ONESHOT_EN	D_SENT_HYST_CFG		CFG_SPCMIN_ADJ		CFG_FSAMPLE_ADR		ROT_DIR_S

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EEPROM

Address 0x0

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				Y_DIE_LOC								X_DIE_LOC								factory reserved					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

Y_DIE_LOC [21:14]:
Y coordinate of die. Used for identification.

X_DIE_LOC [13:6]:
X coordinate of die. Used for identification.

Address 0x1

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	factory reserved				FACTORY_LOT																FACTORY_WAFER					
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

FACTORY_LOT [21:6]:
Identification number. When used in combination with Y_DIE_LOC, X_DIE_LOC, and FACTORY_WAFER, creates a unique identification for device traceability. The register access is customer read only.

FACTORY_WAFER [5:0]:
Identification number. When used in combination with Y_DIE_LOC, X_DIE_LOC, and FACTORY_LOT, creates a unique identification for device traceability. The register access is customer read only.

Address 0x2

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAS_ID																factory reserved									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

CAS_ID [25:10]:
Type of identification number. May contain an identification number to distinguish a specific device configuration. The register access is customer read only.

Address 0x3

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EXTRA_1	EXTRA_0	unused																							
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

EXTRA_1 [25]:
Extra, unused, EEPROM bit. May be written by customer.

EXTRA_0 [24]:
Extra, unused, EEPROM bit. May be written by customer.

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Address 0x24

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		M4	EPOK	MEM_LOCK				R	BVO	HI_Z	PAS	M3	M2	M1	M0	FR	R	AMM		MSL			MSH		
Default	0	0	0	1*	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

* Set to 1 for 5 V I/O configuration. Set to 0 for 3.3 V I/O configurations.

MASK_4 [23]:

Masks SENT_RED_BUF_ERR from setting the S1 and S0 error bits (SENT only). Does not mask the status bits. An error detected in the redundant SENT buffer is indicated in SENT_RED_BUF_ERR.

Value	Description
0	SENT_RED_BUF_ERR is not masked.
1	SENT_RED_BUF_ERR is masked. Will not assert S0 or S1 flags.

EXTENDED_POK_IO_EN [22]:

Extended operational voltage when in 5 V I/O mode.

Value	Description
0	V_{CC} operating range between 4.5 V and 5.5 V (when PASSTHROUGH_EN =1) or between 6 V and 18 V (when PASSTHROUGH_EN = 0).
1	Extended V_{CC} operating range between 3.7 V and 5.5 V (when PASSTHROUGH_EN = 1) or 4.5 V to 18 V (when PASSTHROUGH_EN = 0).

MEM_LOCK [21:18]:

Memory lock bits.

Value	Description
1100_b	Writing to EEPROM is locked.
0011_b	Writing to EEPROM and Shadow is locked.
All others	No Lock.

Reserved [17] [8]:

Reserved bits. No function.

BLOCK_VOLATILE_OUTPUT [16]:

Prevents test modes within volatile memory space from affecting the output.

Value	Description
0	Volatile bits allowed to function normally.
1	Prevents operation of volatile bits that may impact output.

MAKE_ERRORS_HIGH_Z [15]:

Controls PWM error reporting. See Error Reporting Through PWM for additional details.

Value	Description
0	PWM outputs at half frequency and at a fixed duty cycle in response to an error flag.
1	PWM output goes to a high-impedance state in response to an error flag.

PASSTHROUGH_EN [14]:

Enables passthrough mode of the I/O regulator. When set, the I/O regulator is disabled and the I/O voltage is supplied by V_{CC}, allowing 5 V I/O operation when powered from a 5 V source.

Value	Description
0	I/O regulator enabled.
1	I/O regulator disabled. I/O voltage supplied by V_{CC}. Supports 5 V I/O operation with 5 V V_{CC}.

MASK_3 [13]:

Masks the signal mismatch (SMM) flag reporting through PWM or setting S1/S0 bits within SPI/SENT.

Value	Description
0	SMM flag is reported via PWM and sets S1/S0 in SPI/SENT.
1	SMM flag does not set S1/S0 bits in SPI or SENT. SMM flag is not reported via PWM.

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MASK_2 [12]:

Masks the following bits from reporting an error in PWM or setting S1/S0 within SPI and SENT:

- SAT
- MSH
- MSL

Value	Description
0	SAT, MSL, and MSH flags are reported via PWM and set S1/S0 in SPI/SENT.
1	SAT, MSL, and MSH flags do not set S1/S0 bits in SPI or SENT. SAT, MLS, and MSH flags are not reported via PWM.

MASK_1 [11]:

Masks the temperature sensor error (TSE) flag from reporting an error in PWM or setting S1/S0 within SPI and SENT.

Value	Description
0	TSE flag is reported via PWM and sets S1/S0 in SPI/SENT.
1	TSE flag does not set S1/S0 bits in SPI or SENT. TSE flag is not reported via PWM.

MASK_0 [10]:

Masks the following bits from reporting an error in PWM or setting S1/S0 within SPI and SENT:

- VCF
- UVCC
- OVCC

Also masks the OFE flag from asserting the S1/S0 flags within SPI and SENT.

Value	Description
0	VCF, UVCC, and OVCC flags are reported via PWM and S1/S0 are set in SPI/SENT. OFE flag asserts the S1/S0 bits within SPI and SENT.
1	VCF, UVCC, OVCC, and OFE flags do not set S1/S0 bits in SPI or SENT. VCF, UVCC, and OVCC flags are not reported via PWM.

Factory Reserved [9]:

Reserved bit.
Must be set to logic 1.

ANGLE_MISMATCH [7:6]:

Angle mismatch. Sets the threshold for allowable mismatch between the main and redundant angle outputs. If the main and redundant angle values differ more than the threshold, the SMM flag is asserted.

Value	Angle Mismatch Threshold
0	3°
1 (default)	5°
2	8°
3	12°

MSL_THR [5:3]:

Magnetic threshold low value. Sets the low threshold of the input magnetic flux density, B_{IN}. If FIELD_MAG is below the threshold, the MSL flag will be set. When MSL_THR is set to 0, the low threshold comparison is disabled.

Note: The field_mag value is converted to Gauss using:

$$B_{IN}(G) = (FIELD\_MAG_{LSB})/(S \times 3.912),$$

where:

S = 23 for part numbers with suffix 300, and S = 15.5 for part numbers with suffix 600.

Example:

To set the low field threshold to 100 G, first find the corresponding value in codes by rearranging the equation shown above.

For part numbers with suffix 300, 100 G corresponds to a FIELD_MAG of 8,998 codes. The threshold setting closest to this value is Code 1.

Value	Threshold Value in Digital Codes	Approx. Field in G (Part Numbers with Suffix 300)	Approx. Field in G (Part Numbers with Suffix 600)
0	0	Disabled	Disabled
1 (default)	9,830	109	162
2	13,107	146	216
3	19,661	219	324
4	22,938	255	378
5	26,214	291	432
6	29,491	328	486
7	32,768	364	540

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MSH_THR [2:0]:
Magnetic threshold high value. Sets the high threshold of the input magnetic flux density, B_{IN}. If FIELD_MAG is above the threshold, the MSH flag will be set. When logic = 0, high-threshold comparison is disabled.

Note: The field_mag value is converted to Gauss using:

$$B_{IN}(G) = (FIELD\_MAG_{LSB})/(S \times 3.912),$$

where:

S = 23 for part numbers with suffix 300, and S = 15.5 for part numbers with suffix 600.

Example:

To set the high field threshold to 400 G, first find the corresponding value in codes by rearranging the equation shown above.

For part numbers with suffix 300, 400 G corresponds to a FIELD_MAG of 35,990 codes. The threshold setting closest to this is logic = 4.

Value	Threshold Value in Digital Codes	Approx. Field in G (part numbers with suffix 300)	Approx. Field in G (part numbers with suffix 600)
0	65,535	Disabled	Disabled
1 (default)	52,429	583	865
2	45,875	510	757
3	39,322	437	648
4	36,045	401	594
5	32,768	364	540
6	29,491	328	486
7	26,214	291	432

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Address 0x25

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NS	MAX_SENS		TRIG_CFG		ZS	SS	SM	PO	CRC	CIS	SCN_CFG		SENT_DATA_CFG					SENT_PWM_RATE					OUTMSG_MODE		
Default	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CFG_NO_SAMPLE [25]:

SENT no sample. If logic = 1, the F_SAMPLE pulse does not perform a sample-and-hold operation.

Value	Description
0	On receipt of an F_SAMPLE pulse, sensor samples and holds angle data.
1	Sensor does not sample-and-hold data on receipt of an F_SAMPLE pulse.

CFG_MAX_SENSOR [24:23]:

SENT max sensor. Only for SSENT and SSENT Long (OUTMSG_MODE = 3 or 4). Defines the uppermost address on the bus, beyond which the internal slot counter wraps back to 0.

Value	Description
0	One IC on the bus
1	Two ICs on the bus
2	Three ICs on the bus
3	Four ICs on the bus

TRIGGER_CFG [22:21]:

SENT trigger configuration. Sets the minimum trigger length. TSENT only (OUTMSG_MODE = 2 or 5).

Value	Minimum Trigger Time
0	2.5 µs
1	5.0 µs
2	10 µs
3	0.5 µs

CFG_ZERO_SAMPLE [20]:

SENT zero sample. SSENT and SSENT only (OUTMSG_MODE = 3 or 4). If logic = 1, the sensor does not sample-and-hold on slot 0.

Value	Description
0	No special action on slot = 0.
1	Sensor performs a sample-and-hold when its slot counter resets to 0.

CFG_SLOT_SYNC [19]:

SENT slot synchronization (sync). SSENT only. Allows the sensor to synchronize to the bus after a reset based on the slot marking of the other sensor. Only valid if CFG_SLOT_MARKING = 1. Requires CFG_POR_OFFLINE = 1.

Value	Description
0	Slot sync disabled. Sensor will stay off the bus after reset.
1	Slot sync enabled.

CFG_SLOT_MARKING [18]:

SENT slot marking. SSENT only. When enabled, the sensor adds a delay time following an address pulse, prior to responding. Delay time is set based on IC address. Allows differentiation of addressed sensor on the bus. Can be used in conjunction with slot sync (CFG_SLOT_SYNC) to allow an IC to resynchronize its slot counter following a reset.

Value	Description
0	Slot marking is disabled
1	Slot marking is enabled.

CFG_POR_OFFLINE [17]:

SENT POR offline. SSENT and SSENT Long (OUTMSG_MODE = 3 or 4). If logic = 1, the IC remains offline following a reset. If logic = 0 and the slot counter is set to logic = 0, the IC goes online following a reset.

Value	Description
0	After reset, IC will go online with slot counter = 0.
1	Sensor stays offline following a reset. IC will go online following a slot counter synchronization. Actions that may result in synchronization: • F_SYNC pulse • Idle sync (if CFG_IDLE_SYNC = 1) • Slot sync (if slot synchronization and slot marking are enabled)

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CFG_IDLE_SYNC [16]:

SENT idle sync. SSENT and SSENT Long (OUTMSG_ MODE = 3 or 4). If logic = 1 and a SENT bus goes idle for longer than 511 ticks, the slot counter resets to logic = 0.

Value	Description
0	No idle sync.
1	Slot counter resets if SENT bus is idle (no edge transitions) for greater than 511 ticks.

SENT_CRC_CFG [15]:

SENT CRC configuration. This bit allows the SENT frame CRC nibble to include the contents of the status and communication nibble (SCN).

Value	Description
0	SCN contents not included in the SENT frame CRC nibble.
1	SCN contents included via the CRC nibble (does not conform with the J2716 SENT Standard)

SENT_SCN_CFG [14:13]:

SENT SCN configuration. Defines the contents of the status and communication nibble (SCN).

Value (Binary)	Bit 3 [1]	Bit 2 [1]	Bit 1	Bit 0
00	Serial Sync	Serial Data	S1	S0
01	0	0	S1	S0
10	DEVICE_ID [1]	DEVICE_ID [0]	S1	S0
11	Serial Sync	Serial Data	S1	S0

[1] Serial Sync and Serial Data compose the “Short Serial” message.

S1 and S0 set if an error flag is asserted.

SENT_DATA_CFG [12:8]:

SENT data frame configuration. Selects the quantity and content of the data nibbles within the SENT message frame. See SENT description for additional details.

Value	Description
0	Angle only (3 data nibbles)
1	Angle (3) + frame count (1)
2	Angle (3) + rotating status (3)
3	Angle (3) + rotating extended data (3)
4	Angle (3) + frame count (2) + ~first nibble (1) “Secure sensor” format.
5	Angle (3) + diagnostic angle (3)
6	Rotating angle (3) + frame count (1)
7	Rotating angle (3) + rotating status (2) + frame count (1)
8	Angle (3) + ID (1)
9	Angle (3) + frame count (1) + ID (1)
10	Angle (3) + rotating status (1) + frame count (1) + ID (1)
11	Angle (3) + rotating status (2) + [count, ID] (1)
12	Angle (3) + rotating extended data (2) + ID (1)
13	Angle (3) + frame count (1) + ~first nibble (1) + ID (1)
14	Rotating angle (3) + frame count (1) + ID (1)
15	Rotating angle (3) + frame count (2) + ~first nibble (1)
16	Angle (3) + ~flipped angle (3)
17	Angle (3) + frame count (1) + ~second nibble (1) + ~first nibble (1)
18	Angle only (4 data nibbles)
19	Angle (4) + frame count (1)
20	Angle (4) + rotating status (1) + frame count (1)
21	Angle (4) + rotating status (1) + [count, ID] (1)
22	Angle (4) + rotating extended data (2)
23	Angle (4) + frame count (1) + ~first nibble (1)
24	Rotating angle (4) + frame count (1)
25	Rotating angle (4) + rotating status (1) + frame count (1)
26	Angle (4) + ID (1)
27	Angle (4) + frame count (1) + ID (1)
28	Rotating angle (4) + frame count (1) + ID (1)
29	Rotating angle (4) + frame count (1) + ~first nibble (1)
30	Angle (4) + [count, CRC2] (2)
31	Rotating angle (4) + [count, CRC2] (2)

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SENT_PWM_RATE [7:3]:

Configures the SENT tick time and PWM carrier frequency.

PWM Mode

The lower 4 bits of field control the PWM carrier frequency (PWM Freq). The upper bit does not influence PWM speed.

Value (Binary)	PWM Freq (Hz)
0000	125
0001	166.7
0010	250
0011	333.3
0100	500
0101	666.7
0110	800
0111	1000

Value (Binary)	PWM Freq (Hz)
1000	1333.3
1001	1600
1010	2000
1011	2666.7
1100	4000
1101	5333.3
1110	8000
1111	16000

SENT Mode

Sets the SENT tick time. Code 0 is forced to 1 µs. Between Code 1 and Code 23, tick times increase in multiples of an 8 MHz clock (0.125 µs). Between Code 24 and Code 31, tick times increase in 0.5 µs increments.

Value	SENT Tick Time (µs)	Counts in 8 MHz Clock Ticks
0	1	8
1	0.25	2
2	0.375	3
3	0.5	4
…	…	…
7	1	8
…	…	…
11	1.5	12
…	…	…
15	2	16
…	…	…
23	3	24
24	3.5	28
25	4	32
…	…	…
31	7	56

OUTMSG_MODE [2:0]:

SENT operating mode. Selects between the various SENT operating modes. For additional details, refer to the SENT Output Modes section.

Value (Binary)	Description
000	SENT disabled. PWM enabled.
001	ISENT (internally synchronized SENT). ISENT is a free-streaming SENT frame with a pause pulse.
010	TSENT (triggered SENT). Data latched near end of SCN.
011	Sequential SENT—Long (Long SSENT)
100	Sequential SENT (SSENT)
101	Addressable SENT (ASENT)
110	TSENT. Data latched on falling edge of trigger.
111	Free-streaming SENT. No pause pulse between frames.

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Address 0x26 through 0x2A

The AB channel linearization fields. Each address space contains three linearization fields, each 8 bits in size. A total of 16 linearization fields are provided for the AB angle channel.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		AB_LINEARIZATION_N (2, 5, 8, 11, 14)								AB_LINEARIZATION_N (1, 4, 7, 10, 13)								AB_LINEARIZATION_N (0, 3, 6, 9, 12)							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

AB_LINEARIZATION_N:

Linearization field for angle channel AB. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the (N × 22.5)° angle position.

Example:

The AB_LINEARIZATION_12 field applies correction to the measured value of (12 × 22.5°) = 270°.

Value (Binary)	Description
0000 0000	0° compensation at the (N × 22.5)° position.
0000 0001	≈ 0.088° is added to the reading at the (N × 22.5)° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the (N × 22.5)° position.
1000 0000	–11.25° is added to the reading at the (N × 22.5)° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the (N × 22.5)° position.

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Address 0x2B

Additional AB channel linearization fields and customer angle offset field.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED					AB_L	CUST_ANGLE_OFFSET												AB_LINEARIZATION_15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

AB_LIN_ENABLE [20]:

AB channel linearization enable. Enables segmented linearization on AB angle channel.

Value	Description
0	No linearization is applied to the AB angle.
1	Linearization is applied to the AB channel.

AB_LINEARIZATION_15 [7:0]:

Linearization field for angle channel AB. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the 337° angle position.

Value (Binary)	Description
0000 0000	0° compensation at the 337° position.
0000 0001	≈ 0.088° is added to the reading at the 337° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the 337° position.
1000 0000	–11.25° is added to the reading at the 337° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the 337° position.

CUST_ANGLE_OFFSET [19:8]:

Angle offset (zero position) adjustment. Offsets the reported angle value to relocate the 0° reference point. Applied *before* linearization to *all channels* (AB, BC, CA, and main). This value is added to the computed angle. 12-bit field with 12-bit resolution (≈ 0.088°).

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Address 0x2C through 0x30

BC channel linearization fields. Each address space contains three linearization fields, each 8 bits in size. A total of 16 linearization fields are provided for the BC angle channel.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		BC_LINEARIZATION_N (2, 5, 8, 11, 14)								BC_LINEARIZATION_N (1, 4, 7, 10, 13)								BC_LINEARIZATION_N (0, 3, 6, 9, 12)							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BC_LINEARIZATION_N:

Linearization field for angle channel BC. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the (N × 22.5)° angle position.

Example:

The BC_LINEARIZATION_12 field applies correction to the measured value of (12 × 22.5°) = 270°.

Value (Binary)	Description
0000 0000	0° compensation at the (N × 22.5)° position.
0000 0001	≈ 0.088° is added to the reading at the (N × 22.5)° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the (N × 22.5)° position.
1000 0000	–11.25° is added to the reading at the (N × 22.5)° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the (N × 22.5)° position.

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Address 0x31

Final BC channel linearization field. BC channel linearization enable.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED																	BC_L	BC_LINEARIZATION_15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

BC_LIN_ENABLE [8]:

BC channel linearization enable. Enables segmented linearization on BC angle channel.

Value	Description
0	No linearization is applied to the BC angle.
1	Linearization is applied to the BC channel.

BC_LINEARIZATION_15 [7:0]:

Linearization field for angle channel BC. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the 337° angle position.

Value (Binary)	Description
0000 0000	0° compensation at the 337° position.
0000 0001	≈ 0.088° is added to the reading at the 337° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the 337° position.
1000 0000	–11.25° is added to the reading at the 337° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the 337° position.

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Address 0x32 through 0x36

CA channel linearization fields. Each address space contains 3 linearization fields, each 8 bits in size. A total of 16 linearization fields are provided for the CA angle channel.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		CA_LINEARIZATION_N (2, 5, 8, 11, 14)								CA_LINEARIZATION_N (1, 4, 7, 10, 13)								CA_LINEARIZATION_N (0, 3, 6, 9, 12)							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CA_LINEARIZATION_N:

Linearization field for angle channel CA. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the (N × 22.5)° angle position. Example: the CA_LINEARIZATION_12 field applies correction to the measured value of (12 × 22.5°) = 270°.

Value (Binary)	Description
0000 0000	0° compensation at the (N × 22.5)° position.
0000 0001	≈ 0.088° is added to the reading at the (N × 22.5)° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the (N × 22.5)° position.
1000 0000	–11.25° is added to the reading at the (N × 22.5)° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the (N × 22.5)° position.

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Address 0x37

Filter settings, CA channel linearization enable, and final CA channel linearization coefficient field.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED												IIR_BW_SEL			R	R	CA_L	CA_LINEARIZATION_15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

IIR_BW_SEL [13:11]:

Filter setting for all three angle channels.

Value	Bandwidth (kHz)	Typical Response Time (µs) [1]
0	3.125	90
1	6.25	45
2 (default)	12.5	25
3	25	20
4	50	15

[1] Response time defined as the time between the magnet crossing a given angle and the angle updating within the IC. No communication delay is considered.

Reserved [10:9]

Reserved bits. No function.

CA_LIN_ENABLE [8]:

CA channel linearization enable. Enables segmented linearization on CA angle channel.

Value	Description
0	No linearization is applied to the CA angle.
1	Linearization is applied to the CA channel.

Value is determined by design. Not measured at final test.

CA_LINEARIZATION_15 [7:0]:

Linearization field for angle channel CA. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the 337° angle position.

Value (Binary)	Description
0000 0000	0° compensation at the 337° position.
0000 0001	≈ 0.088° is added to the reading at the 337° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the 337° position.
1000 0000	–11.25° is added to the reading at the 337° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the 337° position.

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Address 0x38 through 0x3C

Main channel linearization fields. Each address space contains three linearization fields, each 8 bits in size. A total of 16 linearization fields are provided for the main angle channel.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		MAIN_LINEARIZATION_N (2, 5, 8, 11, 14)								MAIN_LINEARIZATION_N (1, 4, 7, 10, 13)								MAIN_LINEARIZATION_N (0, 3, 6, 9, 12)							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

MAIN_LINEARIZATION_N:

Linearization field for the main angle channel. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the (N × 22.5)° angle position.

Example:

The MAIN_LINEARIZATION_12 field applies correction to the measured value of (12 × 22.5°) = 270°.

Value (Binary)	Description
0000 0000	0° compensation at the (N × 22.5)° position.
0000 0001	≈ 0.088° is added to the reading at the (N × 22.5)° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the (N × 22.5)° position.
1000 0000	–11.25° is added to the reading at the (N × 22.5)° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the (N × 22.5)° position.

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Address 0x3D

Final linearization field for the main angle channel. Main channel linearization enable. Main channel rotation selector.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED																RO_P	M_L	MAIN_LINEARIZATION_15							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

ROT_DIR_P [9]:

Rotation direction primary (main). If set to logic = 0, counter-clockwise magnetic rotation (when viewed looking at the top of the IC) results in an increasing angle output. If set to logic = 1, clockwise rotation results in an increasing angle. Applied after customer offset and before linearization. Only applied to the main angle channel.

Value	Description
0	Angle increases with a counterclockwise rotation (when viewed from above the magnet and device).
1	Angle increases with a clockwise rotation (when viewed from above the magnet and device).

MAIN_LIN_ENABLE [8]:

Main channel linearization enable. Enables segmented linearization on the main angle channel.

Value	Description
0	No linearization is applied to the main angle.
1	Linearization is applied to the main channel.

BC_LINEARIZATION_15 [7:0]:

Linearization field for the main angle channel. 8-bit signed value with 12-bit angle resolution (≈ 0.088° step size). Compensation value applied to the 337° angle position.

Value (Binary)	Description
0000 0000	0° compensation at the 337° position.
0000 0001	≈ 0.088° is added to the reading at the 337° position.
…	…
0111 1111	≈ 11.16° is added to the reading at the 337° position.
1000 0000	–11.25° is added to the reading at the 337° position.
…	…
1111 1111	≈ –0.088° is added to the reading at the 337° position.

Address 0x3E

Customer scratch pad.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNUSED		CUSTOMER_ID																							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

CUSTOMER_ID [23:0]:

Customer identification scratch pad.
An open EEPROM space for customer use.

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Address 0x3F

Additional PWM and SENT settings.

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LS_DRV			HS_DRV			DIAG_CH		PW_E	UNUSED			PWM_PORCH			R	I_P	PUSH_DRV		ONE	SNT_HYS		MIN_ADJ		FA	RO_S
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PWM_SENT_LS_DRV_SEL [25:23]:

PWM/SENT low-side drive control. Controls the fall time of PWM and SENT.

Value	Typical Falling Slew Time 10% – 90%; C_L = 1 nF; R_L = 1.2 kΩ to 5 V (µs) [1]
0	0.18 (no slew control)
1	0.35
2	0.46
3	0.78
4	0.94
5	1.19
6	1.69
7	3.23

[1] Determined by design. Not measured at final test.

PWM_SENT_HS_DRV_SEL [22:20]:

PWM/SENT high-side drive control. Controls the rising time of PWM and SENT. High side is active only if the push_drive EEPROM field is set to logic = 2 or logic = 3.

Value	Typical Rising Slew Time 10% – 90%; C_L 1 nF; R_L = 4.7 kΩ to GND; I/O level = 3.3 V (µs) [1]
0	0.36 (no slew control)
1	0.4
2	0.5
3	0.7
4	0.78
5	1.0
6	1.7
7	3.7

[1] Determined by design. Not measured at final test.

DIAG_CHANNEL_SEL [19:18]:

Diagnostic channel selection. Selects which of the three secondary angle channels is reported as the diagnostic channel. The diagnostic channel is reported in various SENT frames and populates the ANGLE_OUT_DIAG_LATCH value within direct address 0x16.

Value	Description
0	AB channel is the diagnostic angle (DIAG_SEL)
1	AB channel is the diagnostic angle (DIAG_SEL)
2	BC channel is the diagnostic angle (DIAG_SEL)
3	CA channel is the diagnostic angle (DIAG_SEL)

PWM_SENT_ENABLE [17]:

Enables the PWM and SENT output. Once enabled, operation is determined by OUTMSG_MODE.

Value	Description
0	PWM/SENT pin is disabled.
1	PWM/SENT pin is enabled. Operation is determined by the PWM/SENT settings.

PWM_PORCH_SEL [13:11]

PWM output fixed low and high time selection. This parameter configures the fixed low and high time of the PWM output.

Value	PWM Low Clamp (% Duty Cycle)	PWM High Clamp (% Duty Cycle)
0	2	98
1	3	97
2	4	96
3	5	95
4	6	94
5	7	93
6	8	92
7	0	100

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RESERVED [10]:
Reserved bit. No function.

IDLE_PUSH [9]:
Idle push control. Specifies the behavior of the output driver during the idle state for triggered and shared SENT modes (OUTMSG_MODE = 2, 3, 4, 5, 6). The idle state is defined as the state during which the output is inactive awaiting a trigger signal.

Value	Description
0	Output goes to high-z during the idle state
1	Output pushes high (high-side driver is activated) during idle state. Only active if PUSH_DRIVE = 2.

When enabled, the controller must overdrive the device to properly trigger the IC (does not conform with the J2716 SENT Standard).

Use Case:

To prevent external noise from creating false trigger events.

PUSH_DRIVE [8:7]:
Defines the PWM/SENT output driver behavior.

Value	Description
0	Open-drain.
1	Push-assisted. Output stage drives high only during low-to-high edge transitions, after which the output enters high-z for the remainder of the SENT high time.
2	Push-Pull. Output stage actively pushes/pulls for the entire SENT frame. Output will be high-z during the idle state unless IDLE_PUSH = 1.
3	Open-drain.

D_ONESHOT_EN [6]:
Enables one-shot current of PWM/SENT low-side and high-side drivers. When enabled, a precharge is applied to the PWM/SENT drivers, reducing the delay to the start of the rising/falling edge. Recommended when applying a large amount of edge delay (high value of PWM_SENT_LS_DRV_SEL or PWM_SENT_HS_DRV_SEL).

Value	Description
0	Precharge is not applied to the output dirver. High levels of drive strength throttling may add delay to the start of the rising/falling edge.
1 (recommended)	Precharge is applied to output driver. Reduces the delay at the beginning of the rising/falling output edge.

D_SENT_HYST_CFG [5:4]:
Adjusts the SENT and Manchester trigger thresholds. Must be set to code 0 or 2. Values of 1 and 3 are invalid and may result in abnormal operation.

Value	Falling Threshold (V)		Rising Threshold (V)	
	Min	Max	Min	Max
0	1.48	1.76	2.21	2.49
2	1.48	1.76	1.92	2.19

CFG_SPCMIN_ADJ [3:2]:
Function pulse adjust, for SSENT Long only (OUTMSG_MODE = 3). Increases the lower threshold of the F_OUTPUT pulse by the number of ticks in this field (in the range of 0 through 3). For fast tick times (less than 1.5 µs), this adjustment may be needed to prevent the IC from interpreting a SENT low period as a function pulse. All devices sharing a bus should be configured with matching settings.

Value	Description
0	F_OUTPUT minimum is 9 ticks.
1	F_OUTPUT minimum is 10 ticks.
2	F_OUTPUT minimum is 11 ticks.
3	F_OUTPUT minimum is 12 ticks.

CFG_FSAMPLE_ADR [1]:
SENT F_SAMPLE addressing. If logic = 1, the sensor treats the F_SAMPLE pulse as an addressing pulse. If CFG_NO_SAMPLE = 1, the sensor does not sample-and-hold the angle data.

Value	Description
0	F_SAMPLE is treated as a broadcast pulse. Sensor will sample-and-hold the angle data on any F_SAMPLE pulse (unless CFG_NO_SAMPLE = 1).
1	F_SAMPLE is treated as an addressing pulse. Sensor will only sample-and-hold the angle data on an F_SAMPLE pulse if properly addressed.

ROT_DIR_S [0]:
Rotation direction secondary. If set to logic = 0, counterclockwise magnetic rotation (when viewed looking down on the top of the IC) results in an increasing angle output. If set to logic = 1, clockwise rotation results in an increasing angle. Applied after customer offset, before linearization. Applied to channels AB, BC, and CA.

Value	Description
0	Angle increases with a counterclockwise rotation (when viewed from above the magnet and device).
1	Angle increases with a clockwise rotation (when viewed from above the magnet and device).

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VOLATILE MEMORY

Table 14: Volatile Memory Map

Address	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x82	0	0	0	0	0	0	0	EE_DBE_FLAG	EE_SBE_FLAG	EE_ECC						EE_ADDR						EE_ERR_STATUS					CP_ERR	EE_ERR
0x83	0	0	EE_DATA																									
0x85	0	0	0	0	0	0	0	0	0	0	0	0	0	0	EE_LOOP	EE_TEST_ADDR						EE_USE_TEST_ADDR	MARGIN_MIN_MAX_FAIL	MARGIN_ STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
0xa5	0	0	0	0	0	0	0	0	0	0	0	0	MANCH_COMM_E	RESERVED														
0xa9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POKS_TEST_RUNNING	POKS_TEST_START

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Address 0x82

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	EE_DBE_FLAG	EE_SBE_FLAG	EE_ECC						EE_ADDR						EE_ERR_STATUS					CP_ERR	EE_ERR
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RC	RC

EE_DBE_FLAG [20]:

Error flag indicates detection of an EEPROM dual-bit error. The EEPROM ECC logic detects an address with a dual-bit error. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM dual bit error detected
1	EEPROM dual bit error detected

EE_SBE_FLAG [20]:

Error flag indicates detection of an EEPROM single-bit error. The EEPROM ECC logic detects an address with a single-bit error. The ECC logic automatically corrects the faulty bit in the volatile region of memory. This check runs after a reset event or EEPROM load event.

Value	Description
0	No EEPROM single-bit error detected
1	EEPROM single-bit error detected

EE_ECC [18:13]:

EEPROM ECC data. After the internal margin test is complete, this parameter contains the ECC data bits of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x85 [4:3]) for margin results information.

EE_ADDR [12:7]:

EEPROM address data. After the internal margin test is complete, this parameter contains the address of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x85 [4:3]) for margin results information.

EE_ERR_STATUS [6:2]:

Indicates the error status of the last EEPROM write. If logic > 0, an error was detected during the last EEPROM write.

CP_ERR [1]:

Indicates the error status of the EEPROM write charge pump during the last EEPROM write. If logic = 1, an error is detected, and the error is set in EE_ERR_STATUS (extended: 0x82 [6:2]).

EE_ERR [0]:

Indicates detection of an EEPROM write error. If logic = 1, an EEPROM write error is detected. The bit clears after read.

Address 0x83

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EE_DATA																									
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

EE_DATA [25:0]:

EEPROM field data. After the internal margin test is complete, this parameter contains information from the data fields of the first fault address found during the margin test. Data in this parameter is only valid if the margin test reports a failure. See MARGIN_STATUS (extended: 0x85 [4:3]) for margin results information.

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Address 0x85

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	EE_LOOP	EE_TEST_ADDR						EE_USE_TEST_ADDR	MARGIN_MIN_MAX_FAIL	MARGIN_STATUS		MARGIN_NO_MIN	MARGIN_NO_MAX	MARGIN_START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RO	RO	RO	RW	RW	RW

EE_LOOP [13]:

Continuously loops the margin test. When bit logic = 1, the margin test loops continuously. If an error is detected or if MARGIN_START (extended: 0x85 [0]) is cleared, the margin test stops.

Value	Description
0	Margin test runs once
1	Margin test loops continuously until an error is detected

EE_TEST_ADDR [12:7]:

Optional start address for margin test. Defines the starting address for the margin test when EE_USE_TEST_ADDR (extended: 0x85 [6]) is set to logic = 1.

EE_USE_TEST_ADDR [6]:

When set to logic = 1, the margin test starts at the address defined by EE_TEST_ADDR (extended: 0x85 [12:7]).

Value	Description
0	Margin test starts at address 0x0
1	Margin test starts at address defined by ee_test_addr

MARGIN_MIN_MAX_FAIL [5]:

If a margin failure is detected, this bit indicates if the failure was detected at the minimum or maximum reference level.

Value	Description
0	Margin test failure detected at minimum threshold
1	Margin test failure detected at maximum threshold

MARGIN_STATUS [4:3]:

Indicates the status of the margin test. The bits clear after a read or reset event.

Value	Description
0	Reset condition: No result from margin test
1	Pass: No errors detected during margin test
2	Fail: Error detected during margin test
3	In progress: Margin test still running

MARGIN_NO_MIN [2]:

Disables the minimum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the low reference level.

Value	Description
0	Margin test includes check at the low reference level
1	Margin test does not include check at the low reference level

MARGIN_NO_MAX [1]:

Disables the maximum reference level during margin test. When set to logic = 1, the margin test does not check for errors at the high reference level.

Value	Description
0	Margin test includes check at the high reference level
1	Margin test does not include check at the high reference level

MARGIN_START [0]:

Triggers start of margin test. When set to logic = 1, the margin test begins. The bit clears when the margin test completes and EE_LOOP (extended: 0x85 [13]) = 0; if ee_loop = 1, the margin test runs until MARGIN_START = 0. If the margin test detects an error, the MARGIN_START bit clears.

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Address 0xA5

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	MANCH_COMM_E	reserved														
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

MANCH_COMM_E [15]:

Enables Manchester communications mode on the PWM output pin. When logic = 1, the PWM output stops and the pin becomes an input/output pin for Manchester communication. This bit is set directly with a write operation or indirectly using the access code. To exit Manchester communications mode, MANCH_COMM_E is set to logic = 0.

Address 0xA9

Bit	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	POKS_TEST_ RUNNING	POKS_TEST_ START
Access	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW

POKS_TEST_RUNNING [1]:

POKs/IOKs startup test is running.

Value	Description
0	POKs/IOKs startup test is not running.
1	POKs/IOKs startup test is running.

POKS_TEST_START [0]:

When set to logic = 1, runs the POKs/IOKs self-test. If an error occurs, it is reported in POKS_SELF_TEST_FAILED_FLAG (primary: 0xC [7]).

⚠ CAUTION: If PASSTHROUGH_EN = 1, V_{CC} must be less than 5.5 V before initiating self-test. Failure to reduce V_{CC} to less than 5.5 V may result in device damage.

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SAFETY AND DIAGNOSTICS

The A33022 was developed in accordance with the ASIL design flow (ISO 26262) and incorporates several internal diagnostics as well as error/warning/status flags enabling the host microcontroller to assess the operational status of the die.

A short summary of the diagnostics is provided below. A complete listing and discussion of the A33022 safety features may be found in the Safety Manual.

Status, Error, and Warning Flags

The A33022 features include several status, error, and warning flags. These flags allow the external controller to act in response to a detected fault condition. Table 15 provides a summary list of the flags. More information is also found in the Primary Serial Interface Register Reference.

All flags may be read through the primary serial registers (primary: 0xF) via SPI or Manchester communication. These error flags remain set until the register is read or reset, and the condition is removed.

Error Reporting Through SPI

There are two error reporting bits, S0 and S1, within the A33022 SPI frame. The value of S0 and S1 represent the logical “or” of the bits within the error register. The S0 and S1 bits clear after an SPI read transaction and the condition for the flag no longer exists. Note, after a reset event, S0 = 1 and S1 = 1. If an error flag is masked, the result of this flag is not reported by S0 or S1.

Information Flags

The A33022 features a dedicated status register (primary 0xC), providing informational flags to the external controller. These flags may be useful for the external controller to monitor operation. Table 16 provides a summary list of the information status flags. More information is also found in the Primary Serial Interface Register Reference.

Table 15: Status and Error Flags

Status and Error Flag	Description	Flag Response
VCF	Voltage Check Failure	VCF = 1 (primary: 0xF [0]
TSE	Temperature Sensor Error	TSE = 1 (primary: 0xF [1]
SAT	Saturation Error	SAT = 1 (primary: 0xF [2]
OFE	Oscillator Frequency Discrepancy Error	OFE = 1 (primary: 0xF [3]
SMM	Signal Path (primary channel versus secondary channel) Mismatch Error	SMM = 1 (primary: 0xF [4]
MSL	Magnet Sense Low (input condition below low threshold) Error	MSL = 1 (primary: 0xF [5]
MSH	Magnet Sense High (input condition above high threshold) Error	MSL = 1 (primary: 0xF [6]
UVCC	Undervoltage Error	UVCC = 1 (primary: 0xF [7]
OVCC	Overvoltage Error	OVCC = 1 (primary: 0xF [8]
POR	Power-On Reset Event	POR = 1 (primary: 0xF [9]
ESE	Single-Bit EEPROM Error (correctable)	ESE = 1 (primary: 0xF [10]
EUE	Multi-Bit EEPROM Error (uncorrectable)	EUE = 1 (primary: 0xF [11]
SME	Shadow Memory Error. (Multiple Input Shift Register signature error)	SME = 1 (primary: 0xF [12]
BSY	Extended Access Busy Condition	BSY = 1 (primary: 0xF [13]
XEE	Extended Execute Error Condition	EXE = 1 (primary: 0xF [14]
IER	Interface Error Condition	IER = 1 (primary: 0xF [15]

Table 16: Status Register Contents (Primary 0xC)

Bit Value	Status Flag	Description
0	ANG_RDY	Angle Ready
6	MASK_ACTIVE	Mask active
7	POKS_ SELF_ TEST_ FAILED_ FLAG	POK/IOK self-test
9	ECC_SELF _TEST_ FAILED_ FLAG	Error Correction Code self-test

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Error Reporting Through PWM

The PWM output is configurable to report flags using a special frequency and duty cycle or by going to a high-impedance state. The parameter MAKE_ERRORS_HIGH_Z (extended: 0x24 [15]) configures the PWM error reporting function. When MAKE_ERRORS_HIGH_Z = 1, the error flags result in a PWM at high-impedance state for a minimum of two periods. When MAKE_ERRORS_HIGH_Z = 0, the PWM reports the error flags at a defined duty cycle, shown in Table 18, and at half the frequency defined by SENT_PWM_RATE (extended: 0x25 [7:3]).

In the event of multiple error flags, when MAKE_ERRORS_HIGH_Z = 0, the PWM output reports the error condition according to priority. Table 18 lists the error flags in the order of priority from highest to lowest. The highest-priority error dictates the PWM duty cycle. Error flags OFE, SME, and EUE are the highest priority flags and report through the PWM output by a high-impedance state (100% duty cycle).

The parameter PWM_PORCH_SEL (extended: 0x3F [13:11]) configures the PWM minimum and maximum duty cycle and also sets the duty cycle used for error reporting.

The duty cycle for a specific error and PWM_PORCH_SEL setting are shown in Table 18.

Table 17: MAKE_ERRORS_HIGH_Z

Code	Description
0	PWM carrier frequency is halved, and the highest priority error is output on PWM at the selected duty cycle.
1	PWM tristates on an error.

Table 18: PWM Error Flag Duty Cycle

PMW_PORCH_SEL →		0	1	2	3	4	5	6	7
Porch Value (%)		2%	3%	4%	5%	6%	7%	8%	0%
Error	Priority	Duty Cycle (%)							
OFE [1]	Highest	100	100	100	100	100	100	100	100
SME [1]	Highest	100	100	100	100	100	100	100	100
EUE [1]	Highest	100	100	100	100	100	100	100	100
POR	1	16.3	16.3	16.3	16.3	16.4	16.4	16.2	14.9
UVCC	2	38.9	38.8	38.6	38.9	38.8	38.7	38.6	38.4
VCF	3	33.3	33.2	33.2	33.2	33.3	33.0	33.0	32.6
OVCC	4	72.4	72.7	72.6	72.4	72.6	72.4	72.6	73.3
TSE	5	66.8	66.8	66.8	66.8	66.7	67.0	67.0	67.5
MSH	6	61.1	61.2	61.4	61.1	61.2	61.3	61.4	61.5
SAT	7	56.6	56.5	56.7	56.5	56.7	56.6	56.8	56.9
MSL	8	44.5	44.3	44.4	44.5	44.3	44.4	44.2	44.3
SMM	9	22.0	21.8	22.0	21.9	21.9	21.8	21.8	20.8
ESE	10	78.1	78.2	78.0	78.1	78.1	78.2	78.2	79.2

[1] The IC must be reset to clear the flag.

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APPLICATION INFORMATION

Once the device is powered on, the rate of change of V_{CC} for any magnitude larger than 1 V should be limited to less than 1 V/µs.

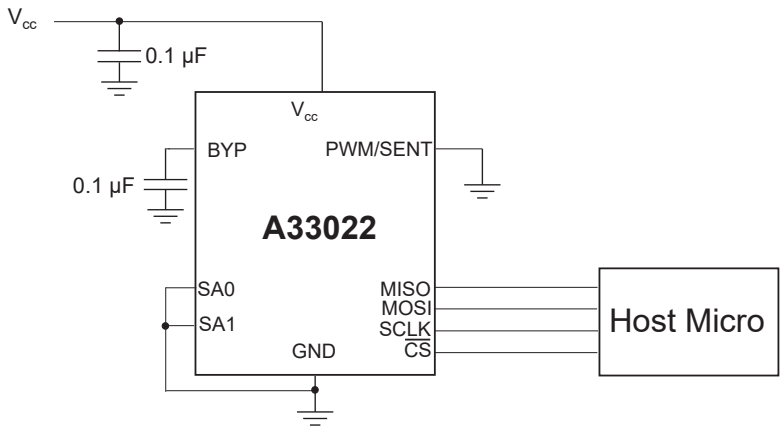

Figure 34: A33022 Configured with SPI.

PWM/SENT line should be connected to ground if not used.

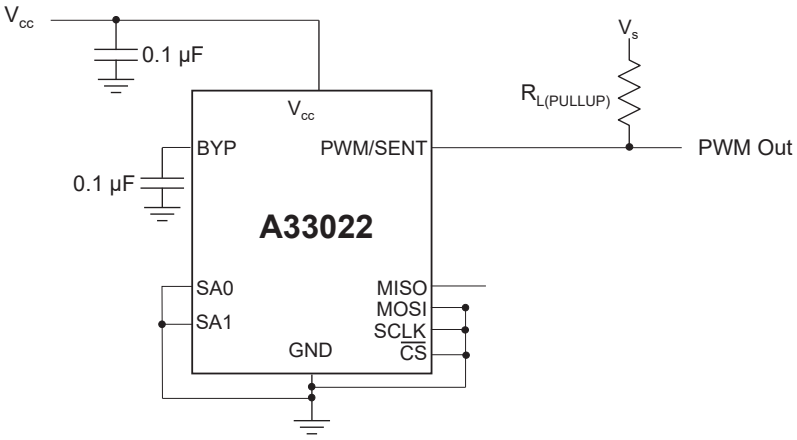

Figure 35: Example A33022 configuration using PWM/SENT output.

Digital reads/writes requests transmitted via Manchester encoding on the PWM/SENT line.
SA0/SA1 configured to 00_2 assigning ID0 as Manchester/SENT Address.
Connect SA0/SA1 to BYP to assign a logic 1.

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I/O STRUCTURES

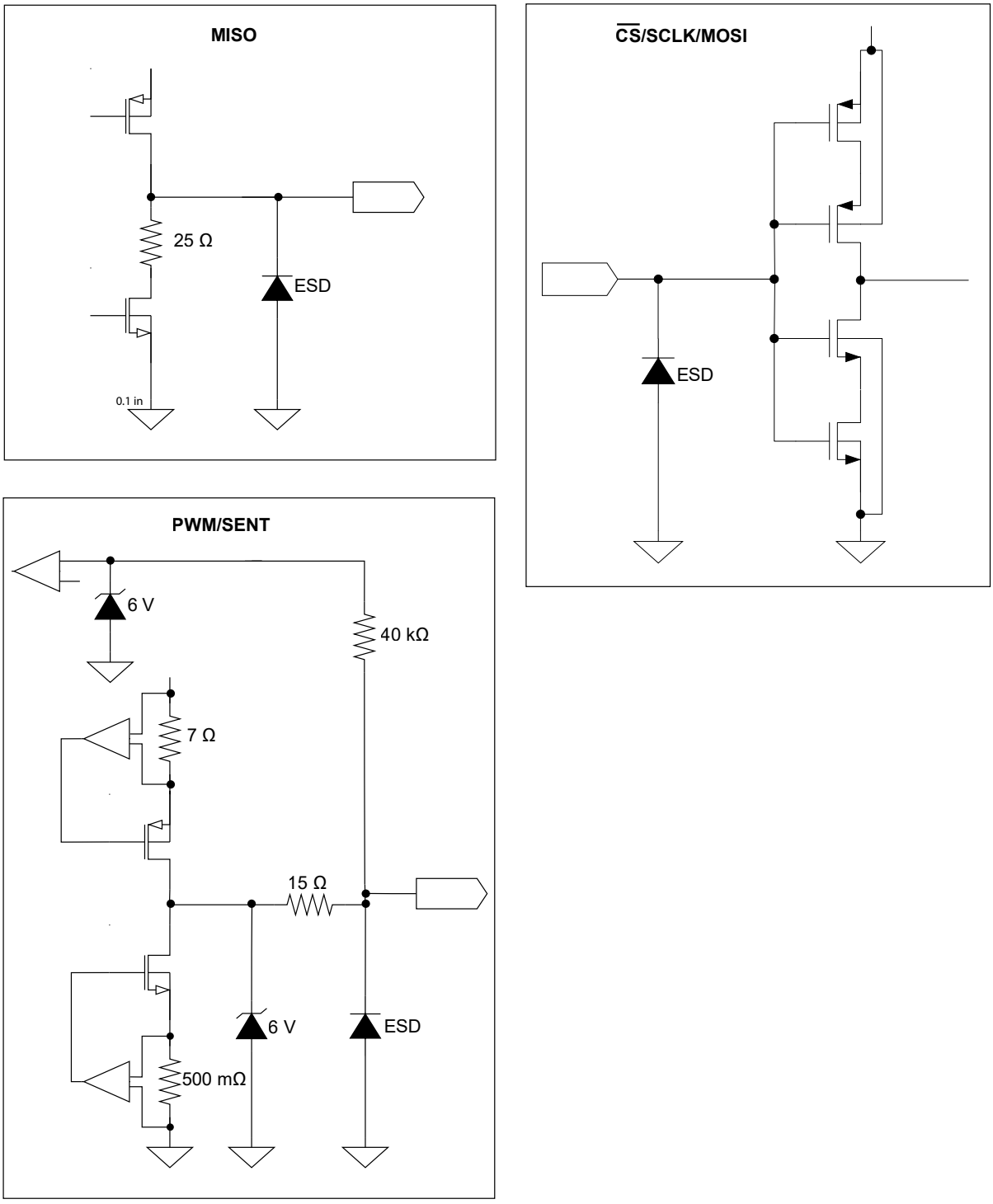

Figure 36: I/O Structure

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PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153 AB-1)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

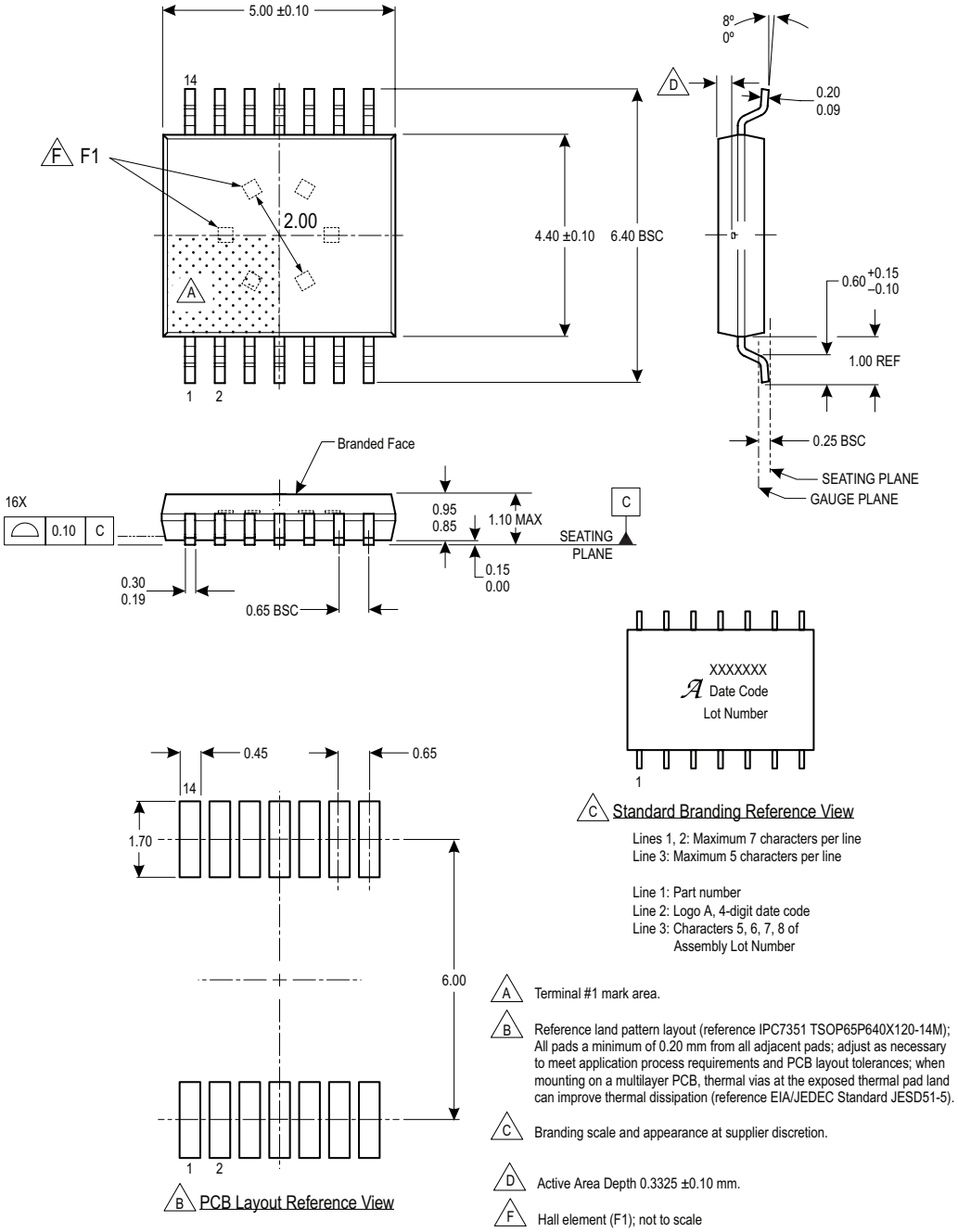

Figure 37: 14-Pin TSSOP Package

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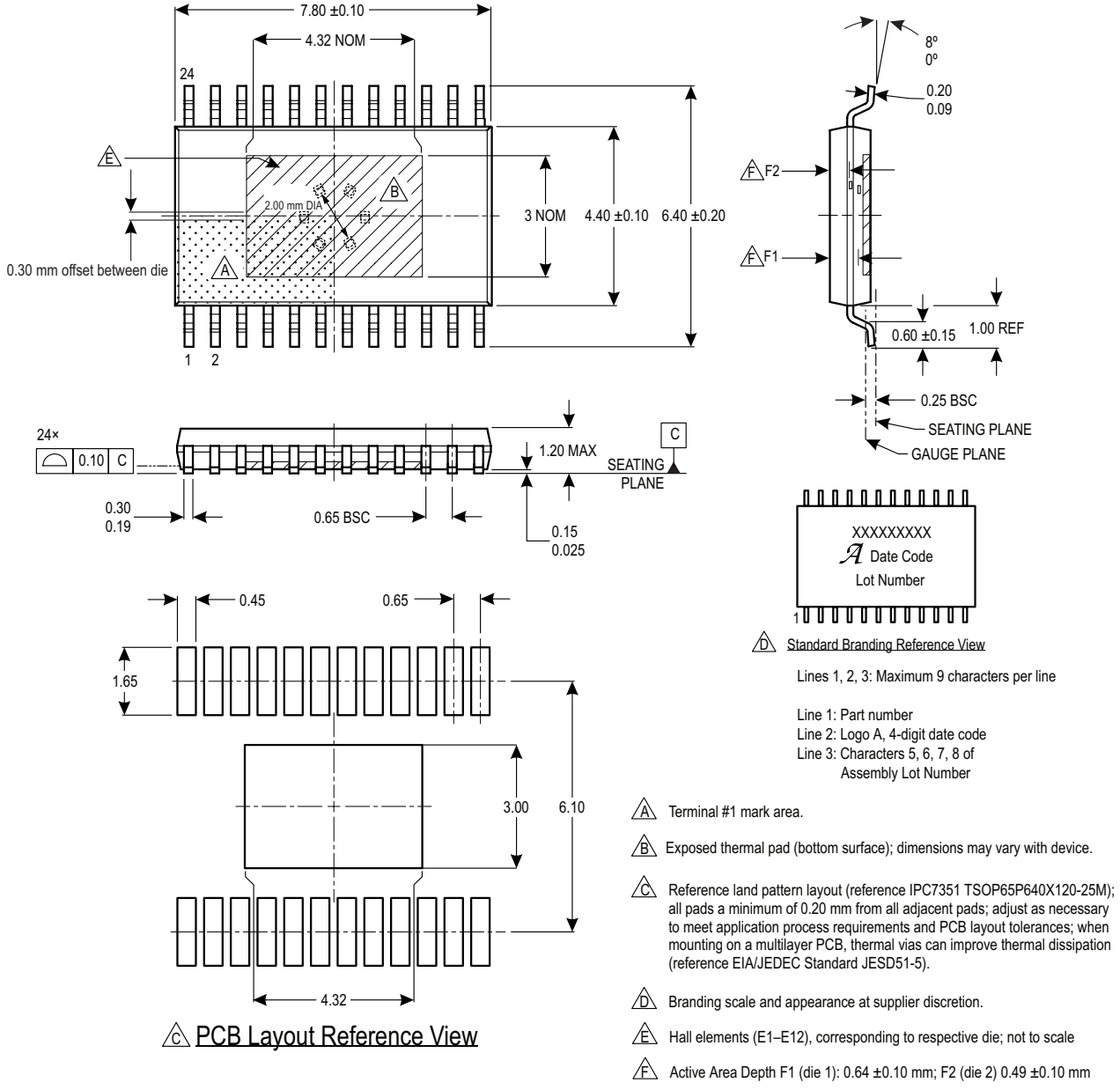
For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Lines 1, 2, 3: Maximum 9 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Terminal #1 mark area.

B Exposed thermal pad (bottom surface); dimensions may vary with device.

C Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

D Branding scale and appearance at supplier discretion.

E Hall elements (E1–E12), corresponding to respective die; not to scale

F Active Area Depth F1 (die 1): 0.64 ±0.10 mm; F2 (die 2) 0.49 ±0.10 mm

Figure 38: 24-Pin eTSSOP Package

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Revision History

Number	Date	Description
–	August 29, 2023	Initial release.
1	December 13, 2023	Added dual-die 24-pin eTTSOP variant (pages 1, 4, 6, 73); updated Power-On Time values (page 7), and footnotes 1, 4, and 6 (page 8); updated Read Response Cycle section (page 22, SPI CRC section (page 23), SPI Power-On Response section (page 24), Table 3 (page 25), Write Command section (page 26), Write Transactions to Extended Memory section (page 34), EEPROM Margin Check section (page 35), INDIRECT_WR_ADDR section (page 37), Addresses 0x09-0x0B (page 39), FULL_RST section (page 40), FACTORY_ACCESS section (page 45); added default values to Addresses 0x24-0x3F (pages 48-62); updated Application Information section (page 70).
2	January 18, 2024	Updated Selection Guide (page 4) and Supply Current test conditions (page 7)
3	June 21, 2024	Updated status of ISO 26262 assessment (page 1), terminal list table (page 6), Operating characteristics table (page 12), Figure 2 (page 15), PWM Output figure numbering (page 17), figure numbering (page 24), Extended Memory table (page 46), Address 0x3F descriptor (page 63), Status Register Contents table (page 68), minor editorial updates throughout
4	October 28, 2024	Updated ASIL status (page 1)
5	January 31, 2025	Updated Operating Characteristics table (page 11), SPI CRC section (page 23), Address 0x08 section (page 39), Address 0x0F section (page 42), and Address 0x24 Magnetic Threshold High register section (page 51)
6	March 18, 2025	Updated Address 0x24 Magnetic Threshold High register section (page 51)

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APPENDIX

MATLAB Function to Compute the A33022 Linearization Coefficients

```
function [lin_coef,gap]=A33022_calc_lin_coef(angle_mech,angle_meas)
%
% This function computes the linearization coefficients for the A33022.
% Linearization is 16 segments with fixed pivot points (0°, 360°/16, 2*360°/16,..., 15×360°/16).
% The coefficients corresponds to the angle error between the measured angle at the pivot points
and the actual magnet position.
%
% Inputs:
%   - angle_mech: n×1 vector: actual magnet position: must be between 0° and 360° and monotically
increasing [°]
%   - angle_meas: n×1 vector: A33022 measured position at each angle_mech position (direct output
of A33022) [°]
%
% Outputs:
%   - lin_coef: 16×1 vector: contains the linearization coefficients [LSB]
%       o lin_coef(1) corresponds to XXX_linearization_0, lin_coef(2) corresponds to XXX_linear-
ization_1, ... , lin_coef(16) corresponds to XXX_linearization_15
%       o coefficients must be converted to 8 bits signed
%   - gap: 16×1 vector: angle error between actual mechanical position and measured position


%% Inspect inputs


% Re-arrange data if necessary
if size(angle_mech,2)>1
    angle_mech=angle_mech';
end
% Only 360° max input range is acceptable
if max(angle_mech)-min(angle_mech)>360
    error('Linearization range must be <=360°')
end
% angle_mech must be increasing
```


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```
if sum(diff(angle_mech)<0)>0
    error('angle_mech must be increasing')
end
% Avoid issues with 360° exact rotation
if wrapTo360(min(angle_mech))==wrapTo360(max(angle_mech))-360
    angle_mech=angle_mech(1:end-1);
    angle_meas=angle_meas(1:end-1);
end

%% Compute the angle error between measurements and actual position

% Re-arrange measured angle
angle_meas_temp=unwrap(wrapTo360(angle_meas)*2*pi/360)*360/2/pi;
angle_meas_temp=unique([angle_meas_temp-360;angle_meas_temp;angle_meas_temp+360],'stable');

% Re-arrange actual position
angle_mech_temp=unwrap(wrapTo360(angle_mech)*2*pi/360)*360/2/pi;
angle_mech_temp=unique([angle_mech_temp-360;angle_mech_temp;angle_mech_temp+360]);

% Interpolate actual position at linearization pivot positions
pivot=[0:360/16:360-360/16]';
mech_pos=interp1(angle_meas_temp,angle_mech_temp,pivot,'spline','extrap');

% Angle error between measurements and actual position
gap=wrapTo180(pivot-mech_pos);

%% Compute the linearization coefficients

% Select only the measurements inside the range
index=zeros(length(pivot),1);
for i=1:length(pivot)
    if min(abs(wrapTo360(angle_meas)-pivot(i)))<=360/16
```


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```
        index(i)=1;
    end
end
index=logical(index);

% Compute the coefficient (remove the mean offset)
lin_coef=round((gap-mean(gap(index)))/(2*11.25/2^8));

% Bound the linearization coefficients
lin_coef(isnan(lin_coef))=0;
lin_coef(lin_coef>2^7-1)=2^7-1;
lin_coef(lin_coef<-2^7)=-2^7;
```


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