A4918-1A

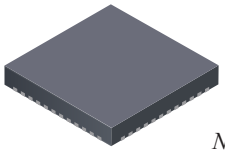
Automotive Three-Phase MOSFET Driver

FEATURES AND BENEFITS

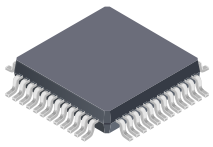
- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Charge pump for low supply voltage operation
- Top-off charge pump for 100% PWM
- Programmable gate drive voltage and strength
- 4.5 to 50 V supply voltage operating range
- Integrated logic supply
- Three programmable current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Extensive programmable diagnostics
- Diagnostic verification
- Safety assist features
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems

PACKAGES:

48-pin QFN with exposed thermal pad and wettable flank (suffix EV)



48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

DESCRIPTION

The A4918 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a 3-phase bridge arrangement and is specifically designed for automotive applications with high-power inductive loads, such as BLDC motors.

A unique charge pump regulator provides the supply for the MOSFET gate drive for battery voltages down to 7 V and allows the A4918 to operate with a reduced gate drive down to 4.5 V. Gate drive voltage and strength are programmable to help reduce EMC issues. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs with an additional above-battery charge pump to ensure that the bootstrap capacitors remain charged when held in the on state.

Full control is provided over all six power MOSFETs in the 3-phase bridge, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

The serial interface is provided to alter programmable settings and read back detailed diagnostic information.

The A4918 is supplied in a 48-terminal wettable flank QFN package (suffix EV) and a 48-pin QFP package (suffix JP), both with exposed thermal pad. These packages are lead (Pb) free with 100% matte-tin leadframe plating.

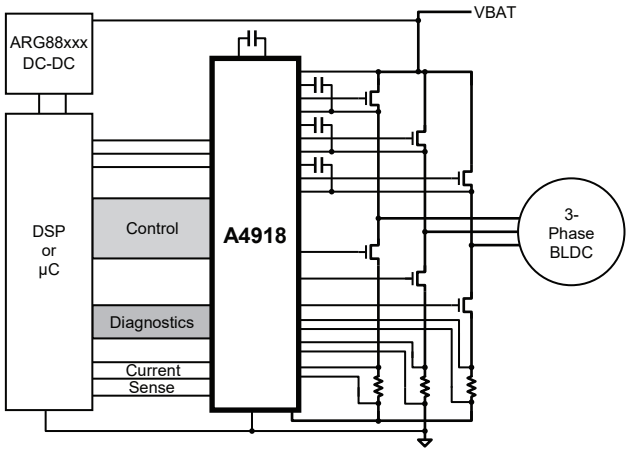


Figure 1: Typical Application

SELECTION GUIDE

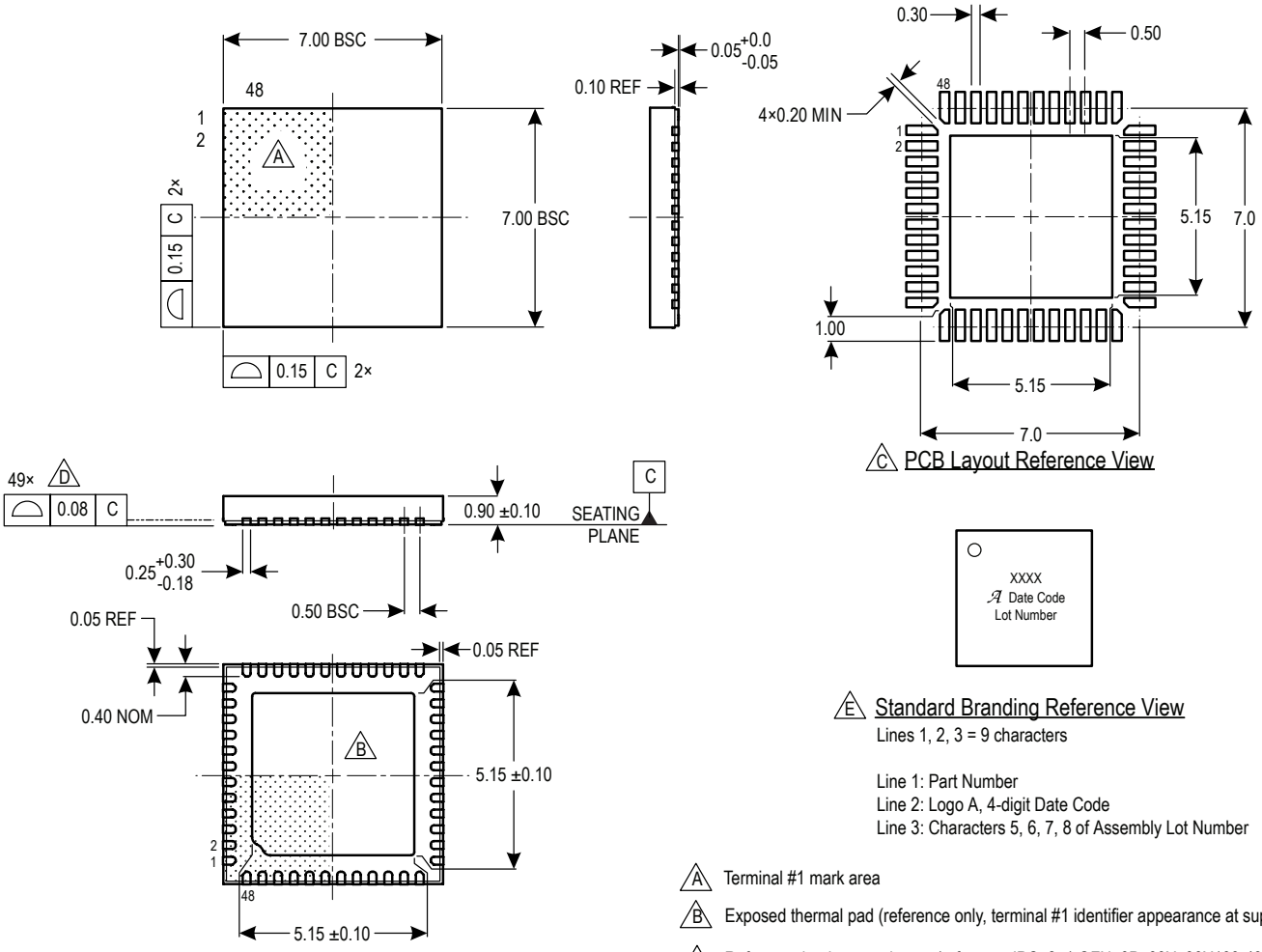
Part Number	I/O Logic	Packing	Package
A4918KEVSR-1A-3-T	3.3 V	4000 pieces per 13-inch reel	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank
A4918KEVSR-1A-5-T	5 V		
A4918KJPTR-1A-3-T	3.3 V	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-lead QFP with exposed thermal pad
A4918KJPTR-1A-5-T	5 V		

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 2: EV Package, 48-Pin QFN with Exposed Thermal Pad and Wettable Flank

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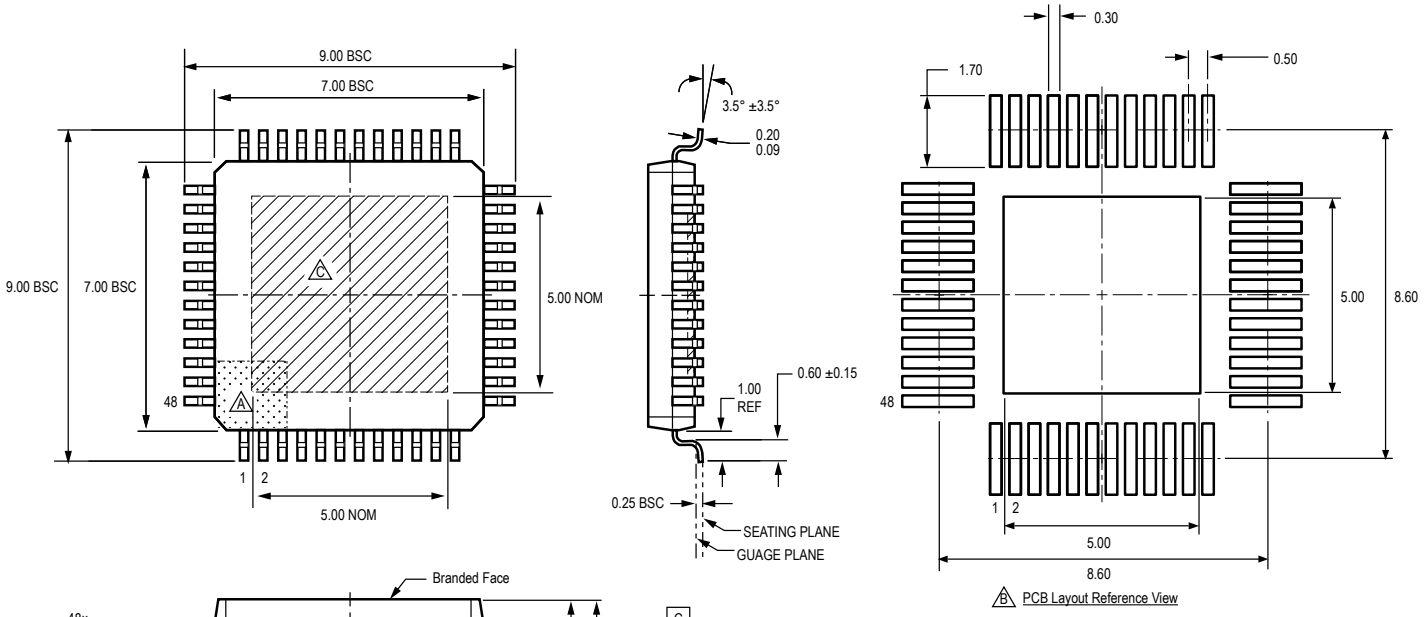
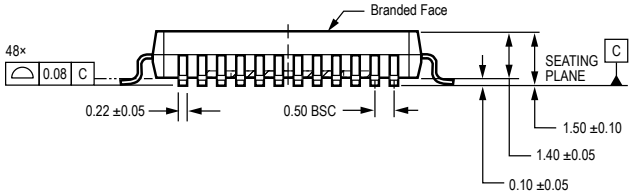
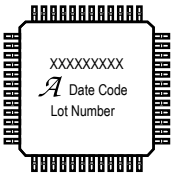
(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown







A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

Figure 3: JP Package, 48-Pin LQFP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	February 9, 2021	A4918-1A initial release. Derived from A4918-A datasheet dated 2 Dec 2019. Part numbers amended (page 2)
1	March 2, 2022	Updated package drawings (pages 69-70)
2	April 11, 2024	Changed logic I/O characteristic of input pull-down STRn to “input pull-up STRn” (page 8), updated DIAG output temperature range test conditions (page 11), updated bridge terminal connection verification diagram (page 36), updated serial register definition (page 43)
3	September 18, 2024	Created short-form variant of long-form datasheet

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