A4990

Automotive Dual Full-Bridge Driver

FEATURES AND BENEFITS

- Two full-bridge power outputs
- Typical application up to ±800 mA, 28 V
- Adjustable peak current limit control
- Minimum overcurrent shutdown at 1.4 A
- Continuous operation at high ambient temperature
- Synchronous rectification for low power dissipation
- Simple parallel interface control
- Inverted and non-inverted inputs
- No crossover current
- Low current consumption in sleep mode
- Error flag diagnostics
- Open load diagnostic during on-state for all outputs
- Outputs protected against overcurrent
- Overtemperature protection with hysteresis

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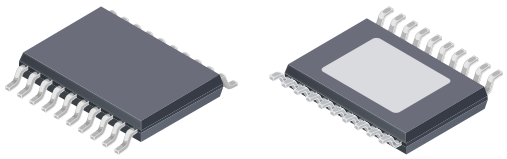
PACKAGE: 20-pin TSSOP with exposed thermal pad (suffix LP)



Not to scale

DESCRIPTION

The A4990 is a dual full-bridge driver for stepper motors and small brush DC motors in automotive applications. Each full bridge uses DMOS power devices with integrated freewheeling diodes. Control circuits prevent cross-conduction, or shoot-through, when switching between high-side and low-side drives.

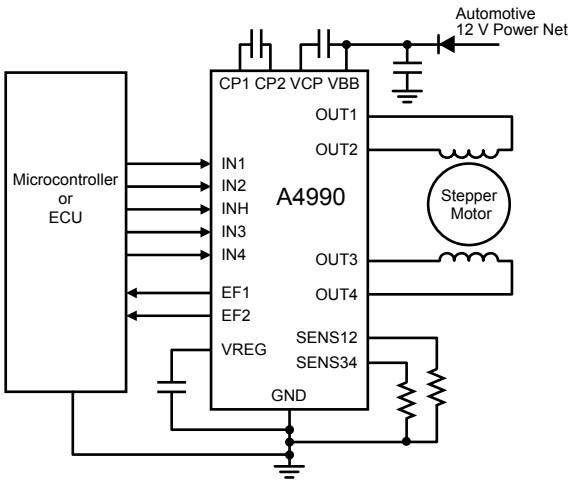
This device drives stepper motors with full current in either direction in each phase, allowing two-phase on, full-step operation. It drives DC motors in both directions and has brake capability. A single input turns-off both bridges, allowing motors to coast. All control modes can easily be achieved using 3, 4, or 5 outputs from a standard parallel interface of a microcontroller.

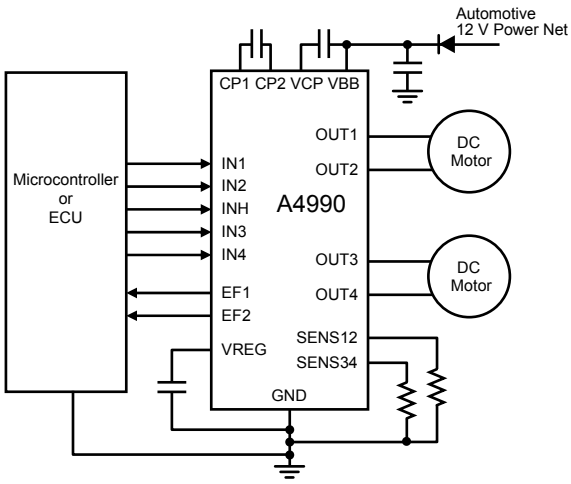
The peak motor current can be limited by sense resistor selection, providing higher efficiency, reduced motor heating, and longer motor life.

The outputs are protected from short circuits to supply and to ground, and low load-current detection is included. Chip level protection includes: overtemperature shutdown, and overvoltage and undervoltage lockout.

The A4990 is supplied in a 20-lead TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin lead frame plating.

Typical Applications





FEATURES AND BENEFITS (continued)

- Overvoltage and undervoltage lockout
- 3.3 V / 5 V compatible inputs with hysteresis
- Thermally enhanced package (exposed pad)
- Fully integrated in a compact TSSOP package for space sensitive applications

SELECTION GUIDE

Part Number	Packing	Package
A4990KLPTR-T	4000 pieces per 13-in. reel	4.4 mm × 6.5 mm, 1.2 mm nominal height 20-pin TSSOP with exposed thermal pad

ABSOLUTE MAXIMUM RATINGS with respect to ground

Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		–0.3 to 50	V
CP1 Pin			–0.3 to V_{BB}	V
CP2, VCP Pin			–0.3 to V_{BB} + 8	V
OUT1, OUT2, OUT3, OUT4 Pins			–0.3 to V_{BB}	V
IN1, IN2, IN3, IN4 Pins			–0.3 to 6	V
VREG Pin			–0.3 to 8.5	V
INH Pin			–0.3 to 6	V
EF1, EF2 Pins			–0.3 to 6	V
SENS12, SENS34 Pins			–0.3 to 1	V
Operating Ambient Temperature	T_A	L temperature range, limited by power dissipation	–40 to 150	°C
Maximum Junction Temperature	T_J(max)	Continuous	150	°C
		Single overtemperature event not exceeding 10 s, cumulative lifetime duration not exceeding 10 hours, specified by design characterization	175	°C
Storage Temperature	T_{stg}		–55 to 150	°C

Thermal Characteristics: May require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	Estimated, on Package LH, on 4-layer PCB based on JEDEC standard	31	°C/W
		Estimated, on 2-layer PCB with 3.8 in.^{2} of copper area each side	38	°C/W
Package Thermal Resistance (Junction to Case)	$R_{\theta JC}$	Estimated	2	°C/W

*Additional thermal information available on the Allegro website.

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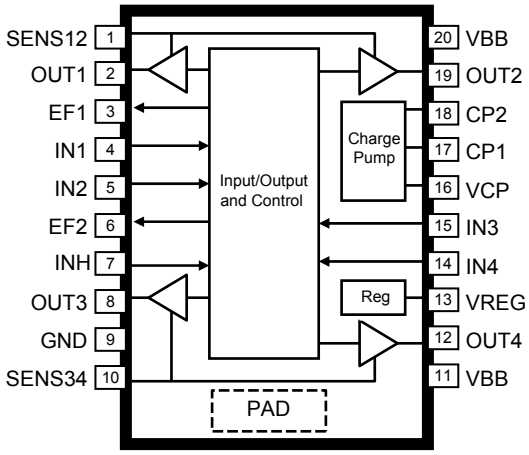
Pinout Diagram



Terminal List Table

Number	Name	Function
CP1	17	Charge pump capacitor
CP2	18	Charge pump capacitor
EF1	3	Error flag 1
EF2	6	Error flag 2
GND	9	Ground
IN1	4	Bridge control input 1, phase A
IN2	5	Bridge control input 2, phase A
IN3	15	Bridge control input 3, phase B
IN4	14	Bridge control input 4, phase B
INH	7	Drive disable input, active low
OUT1	2	Bridge output 1, phase A
OUT2	19	Bridge output 2, phase A
OUT3	8	Bridge output 3, phase B
OUT4	12	Bridge output 4, phase B
PAD	–	Exposed thermal pad for enhanced thermal dissipation
SENS12	1	Current sense node, phase A bridge
SENS34	10	Current sense node, phase B bridge
VBB	11, 20	Motor supply voltage
VCP	16	Pump storage capacitor
VREG	13	Regulated voltage

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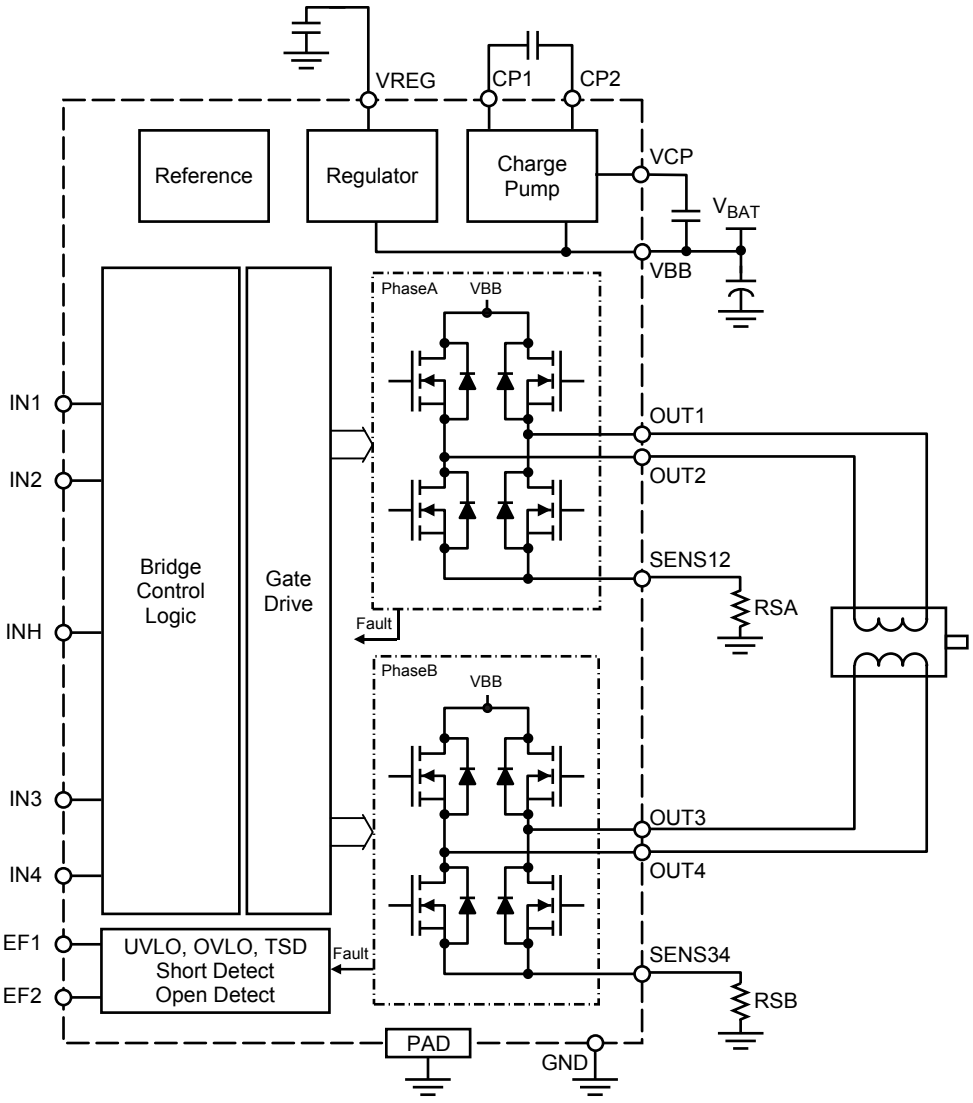
Functional Block Diagram



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ELECTRICAL CHARACTERISTICS: Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 28 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLIES						
Load Supply Voltage Range[1]	$V_{BB(func)}$	Functional, no unsafe states	0	–	50	V
	$V_{BB(op)}$	Outputs driving	6	–	V_{BBOV}	V
Load Supply Quiescent Current	I_{BBQ}	INH = high, IN1 = IN3 = low, IN2 = IN4 = high	–	7	10	mA
		INH < 0.5 V, sleep mode	–	1	5	µA
Charge Pump Voltage	V_{CP}	V_{BB} > 7.5 V, INH = high	–	V_{BB} + 6.7	–	V
Internal Regulator Voltage	V_{REG}	INH = high, V_{BB} > 7.5 V	–	7.2	–	V
Internal Regulator Dropout Voltage	V_{REGDO}	INH = high, V_{BB} > 5.6 V	–	100	200	mV
MOTOR BRIDGE OUTPUT						
High-Side On-Resistance [2]	$R_{DS(on)H}$	V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = –1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = –1 A, T_J = 25°C	–	625	750	mΩ
High-Side Body Diode Forward Voltage	V_{fH}	I_f = 1 A	–	–	1.4	V
Low-Side On-Resistance	$R_{DS(on)L}$	V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 25°C	–	500	600	mΩ
		V_{BB} = 13.5 V, I_{OUT} = 1 A, T_J = 150°C	–	900	1100	mΩ
		V_{BB} = 7 V, I_{OUT} = 1 A, T_J = 25°C	–	625	750	mΩ
Low-Side Body Diode Forward Voltage [2]	V_{fL}	I_f = –1 A	–	–	1.4	V
Dead Time	t_{DEAD}		–	500	–	ns
Output Leakage Current [2]	$I_{OUT(lkg)}$	INH = high, V_{OUT} = V_{BB}	–120	–65	–	µA
		INH = high, V_{OUT} = 0 V	–200	–120	–	µA
		INH = low, V_{OUT} = V_{BB}	–	<1.0	20	µA
		INH = low, V_{OUT} = 0 V	–20	<1.0	–	µA
CURRENT LIMIT						
Internal Oscillator Frequency	f_{OSC}		3.2	4	4.8	MHz
Blank Time	t_{BLANK}		2800	3500	4200	ns
PWM Frequency	f_{PWM}		17.3	21.7	26	kHz
Internal Reference Voltage	V_{REF}		1.1	1.2	1.3	V
Maximum Sense Voltage	V_{SMAX}		–	125	–	mV
Current Trip Point Error [3]	Err_{ITrip}		–	–	±10	%
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}		–	–	0.8	V
Logic Input Low Voltage for Sleep Mode (INH pin)	V_{ILS}		–	–	0.5	V
Logic Input High Voltage	V_{IH}		2.0	–	–	V
Logic Input Hysteresis	V_{Ihys}		100	300	–	mV

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ELECTRICAL CHARACTERISTICS Valid at T_J = –40°C to 150°C, V_{BB} = 7 to 28 V; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC INPUT AND OUTPUT (continued)						
Logic Input Pull-Down Current (IN1,IN3, INH pins)	I_{PD}	IN1 = IN3 = INH = 2 V	10	25	50	µA
Logic Input Pull-Up Current (IN2, IN4 pins) [2]	I_{PU}	IN2 = IN4 = 0.8 V	–10	–25	–50	µA
Logic Output Low Voltage (EF1, EF2 pins)	V_{OL}	EF1 = EF2 = 2 mA	–	0.2	0.4	V
Logic Output Leakage [2]	$I_{O(lkg)}$	0 V < V_O < V_{DD}	–1	–	1	µA
Logic Input Pulse Filter Time (IN1, IN2, IN3, IN4 pins)	t_{PIN}		–	80	–	ns
Sleep Mode Delay	t_{SLEEP}	From INH going low until sleep mode	–	300	–	µs
Wake-up from Reset	t_{EN}		–	–	2	ms
DIAGNOSTICS AND PROTECTION						
VBB Overvoltage Turn-Off Voltage	V_{BBOV}	V_{BB} rising	32	34	36	V
VBB Overvoltage Hysteresis	$V_{BBOVhys}$		2	–	4	V
VBB Undervoltage Threshold	V_{BBUV}	V_{BB} falling	5.2	5.5	5.8	V
VBB Undervoltage Hysteresis	V_{BBhys}		500	760	–	mV
VREG Undervoltage Threshold	V_{REGUV}	V_{REG} falling	4.6	4.8	4.95	V
VREG Undervoltage Hysteresis	$_{VREGhys}$		250	370	–	mV
High-Side Overcurrent Threshold	I_{OCH}	Sampled after t_{SCT}	1.4	2.05	2.65	A
High-Side Current Limit	I_{LIMH}	Active during t_{SCT}	3	5.5	8	A
Low-Side Overcurrent Sense Voltage	V_{OCL}	Sampled after t_{SCT}	210	250	290	mV
Overcurrent Fault Delay	t_{SCT}		1500	2000	2700	ns
Open Load Current	I_{OLP}		6	12	20	mA
Open Load Fault Delay	t_{dOLP}		717	896	1075	µs
Overtemperature Shutdown	T_{JF}	Temperature increasing	155	170	–	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = T_{JF} – T_{Jhys}	–	15	–	°C

[1] $V_{BB(func)}$ function is correct but parameters may not meet specification when 7 V > V_{BB} or V_{BB} > 28 V. Outputs not operational above V_{BBOV} or below V_{REGUVL}.

[2] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

[3] Current Trip Point Error is the difference between the actual current trip point and the target current trip point, referred to maximum full scale (100%) current: $Err_{Trip} = 100 \times (I_{TripActual} - I_{TripTarget}) / I_{FullScale}$ (%).

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Table 1. Functional Truth Table

Input/Output					Functional State		
Phase A							
INH	**IN1**	**IN2**	**OUT1**	**OUT2**	**Mode**	**Stepper Motor Operation**	**DC Motor Operation**
L	X	X	Z	Z	Sleep	Low current consumption	Low current consumption
H	Z	Z	L	L	Brake: low side	No phase current	Low-side brake
H	L	L	L	H	Current driven negative	Negative phase current	Motor turns counterclockwise
H	L	H	L	L	Low-side recirculation	No current	Low-side brake
H	H	L	H	H	High-side recirculation	No current	High-side brake
H	H	H	H	L	Current driven positive	Positive phase current	Motor turns clockwise
Phase B							
INH	**IN3**	**IN4**	**OUT3**	**OUT4**	**Mode**	**Stepper Motor Operation**	**DC Motor Operation**
L	X	X	Z	Z	Sleep	Low current consumption	Low current consumption
H	Z	Z	L	L	Brake: low side	No phase current	Low-side brake
H	L	L	L	H	Current driven negative	Negative phase current	Motor turns counterclockwise
H	L	H	L	L	Low-side recirculation	No current	Low-side brake
H	H	L	H	H	High-side recirculation	No current	High-side brake
H	H	H	H	L	Current driven positive	Positive phase current	Motor turns clockwise

X = don’t care, Z = high-impedance

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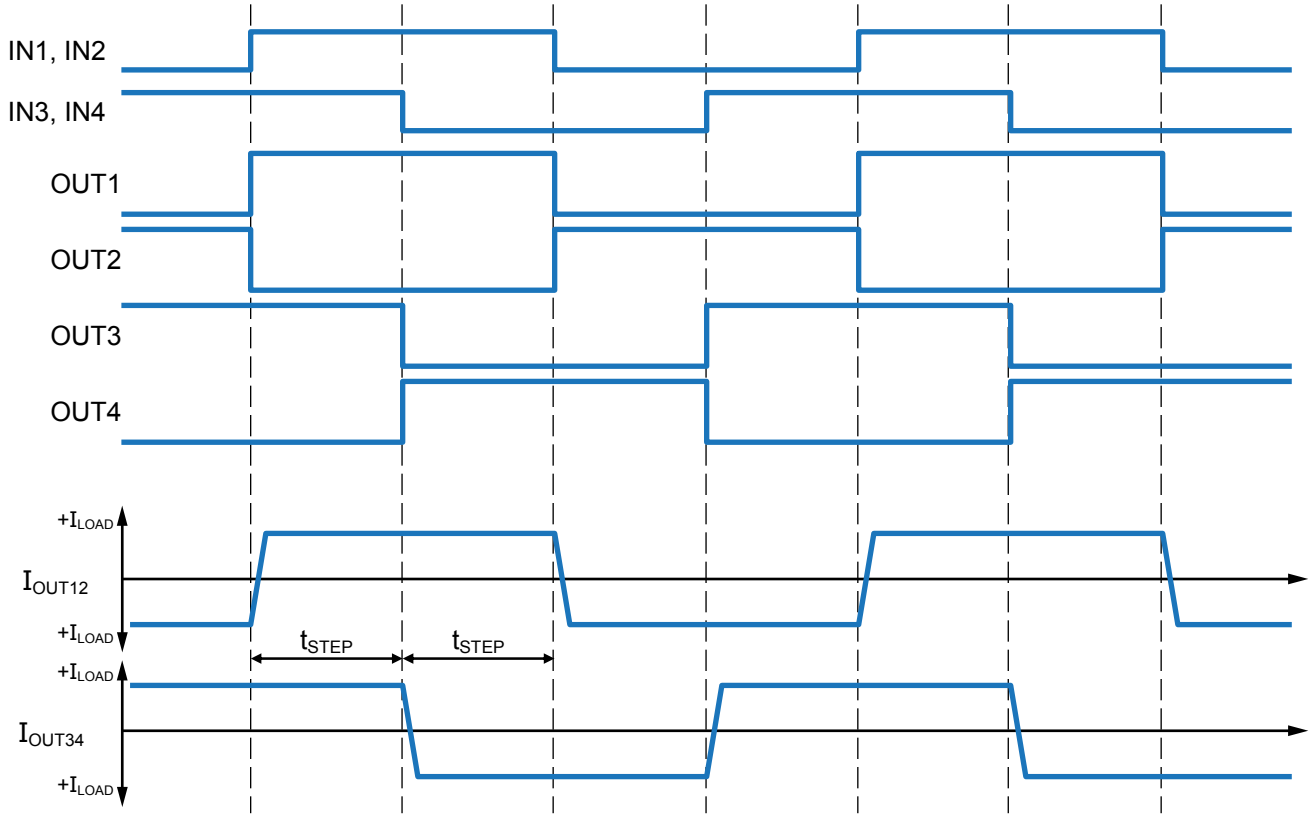

Figure 1. Stepper Motor Input and Output Sequence Timing Diagram

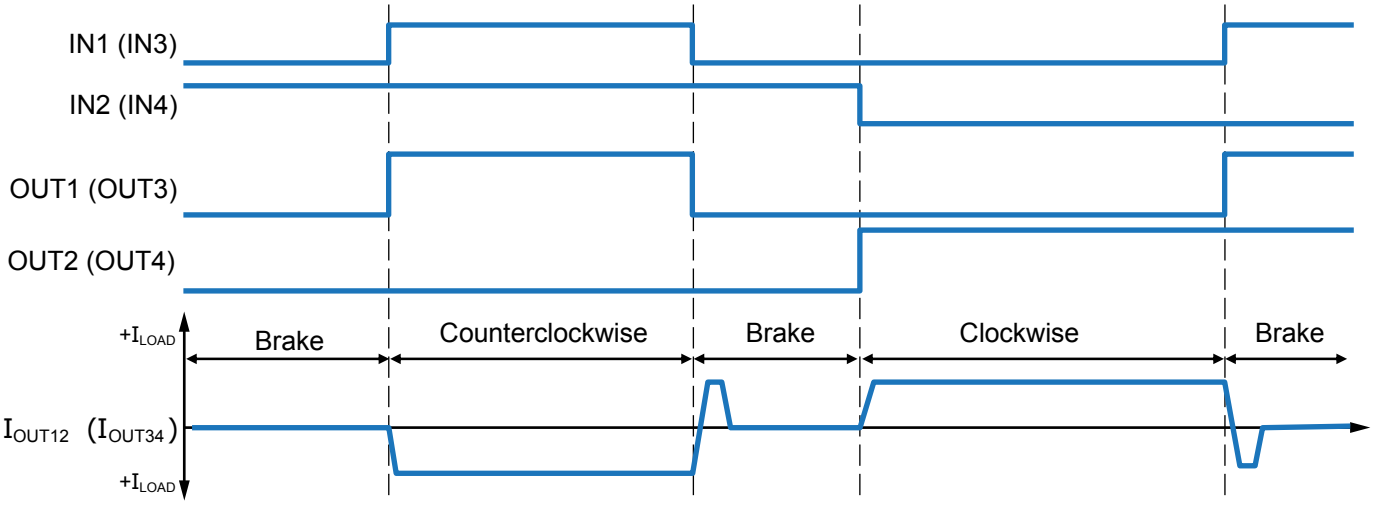

Figure 2. Brush DC Motor Input and Output Sequence Timing Diagram (phase B names shown in parentheses)

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FUNCTIONAL DESCRIPTION

The A4990 is an automotive dual full bridge driver suitable for high temperature applications such as headlamp bending and leveling, throttle control, and fuel recirculation control. It is also suitable for other low-current stepper applications, such as air conditioning and venting.

The device provides two full-bridge drivers for stepper motors and small brush DC motors. Each full-bridge uses DMOS power devices with integrated freewheeling diodes and the control circuit prevents cross-conduction, or shoot-through, when switching between high-side and low-side drives.

The A4990 drives stepper motors with full current, in either direction in each phase, allowing two-phase on, full-step operation. It drives DC motors in both directions and has brake capability. A single input turns-off all bridges, allowing all motors to coast. All control modes can easily be achieved using 3, 4 or 5 outputs from a standard parallel interface of a microcontroller.

The current in each phase of the stepper motor is regulated by a fixed frequency, peak detect PWM current regulator. The motor peak current can be limited by the values selected for external sense resistors, providing higher efficiency, reduced motor heating, and longer motor life.

The outputs are protected from short circuits to supply and to ground, and low load-current detection is included. Chip level protection includes: overtemperature shutdown, and overvoltage and undervoltage lockout. Faults are indicated by two error flags.

Pin Functions

VBB. Main motor supply and chip supply for internal logic, regulators, and charge pump. Both VBB pins must be connected to the main supply and each decoupled to ground with a ceramic capacitor. A low ESR electrolytic capacitor must be connected between the main supply and ground to provide motor switching currents.

CP1 and CP2. Pump capacitor connection for charge pump. Connect a 100 nF / 50 V ceramic capacitor between CP1 and CP2.

VCP. Above-supply voltage for high-side drive. A 100 nF / 16 V ceramic capacitor should be connected between VCP and VBB to provide the pump storage reservoir.

VREG. Regulated supply for bridge gate drives. A 470 nF / 10 V ceramic capacitor should be connected between VREG and ground.

GND. Chip ground. Connect to supply ground.

OUT1 and OUT2. Motor connection for phase A. Positive motor phase current direction is defined as flowing from OUT1 to OUT2.

OUT3 and OUT4. Motor connection for phase B. Positive motor phase current direction is defined as flowing from OUT3 to OUT4.

SENS12. Phase A current sense. Connect sense resistor between SENS12 and GND.

SENS34. Phase B current sense. Connect sense resistor between SENS34 and GND.

IN1. Control input for OUT1 with internal pull-down.

IN2. Inverted control input for OUT2 with internal pull-up.

IN3. Control input for OUT3 with internal pull-down.

IN4. Inverted control input for OUT4 with internal pull-up.

INH. Inhibit control input. Controls activity of bridge outputs. When held low, deactivates the outputs, that is, turns-off all output bridge FETs and the A4990 enters sleep mode.

EF1. Error flag output 1. Combines with EF2 to indicate active fault status. Open drain output requiring an external pull-up resistor to the logic supply voltage.

EF2. Error flag output 2. Combines with EF1 to indicate active fault status. Open drain output requiring an external pull-up resistor to the logic supply voltage.

Operation

The two full-bridges in the A4990 are each controlled by two logic inputs, one input for each half bridge (IN1 for OUT1, and so forth), according to the logic shown in table 1. The two bridges are controlled independently except for the INH input which turns-off all outputs and puts the A4990 into low current sleep mode.

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The two bridges in the A4990 can be used to drive a single, two-phase bipolar stepper motor or two bidirectional brush DC motors:

- *Stepper Motor* – A two-phase stepper motor is made to rotate by sequencing the relative currents in each phase using the four inputs as shown in figure 1. In its simplest form, each phase in turn is fully energized by applying a forward or reverse voltage to each winding in sequence.
- *Brush DC Motor* – A brush DC motor can be driven by each full-bridge, in both directions as shown in figure 2. In addition to controlling rotation direction, the two control inputs for each bridge can be used to provide PWM speed control and motor braking.

The operating modes for each motor type are listed in table 1.

Current Limiting. The A4990 includes a PWM current control function that can be used to limit the phase current with changes in the operating temperature and voltage. This prevents overheating in the motor at high supply voltage or low temperatures. The PWM current control function in the A4990 can be used to limit the current in each phase independently. The current limit function is only active when other factors, such as motor phase R/L, motor speed, or supply voltage do not limit the phase current.

For each of the two phases, the currents are measured in the full-bridge using a sense resistor, RSx, with voltage feedback to the respective SENSx pin. The target current level, I_{PHASEx}, is defined as:

$$I_{PHASEx} = V_{REF} / (16 \times R_{Sx})$$

where

V_{REF} is the internal reference voltage, and

R_{Sx} is the phase sense resistor value.

Table 2 provides some typical currents using E96 series resistor values.

The current comparison is ignored at the start of the PWM on-time for a duration referred to as the *blank time*. The blank time is necessary to prevent any capacitive switching currents from causing a peak current detection.

Cross-Conduction. Each leg (high-side, low-side pair) of a bridge is protected from cross-conduction, or shoot-through, by a fixed dead time, t_{DEAD}. This is the time between switching-off one FET and switching-on the complementary FET. Cross-conduction is prevented by lock-out logic in each driver pair.

Diagnostics

The A4990 integrates a number of diagnostic features to protect the driver and load as far as possible from fault conditions and extreme operating environments. Some of these features automatically disable the current drive to protect the outputs and the load. Others only provide an indication of the likely fault status, by setting the error flags, EF1 and EF2. The full fault table is shown in table 3.

Overcurrent. An overcurrent fault condition is usually caused when an output is shorted to the supply or to ground, or the motor phase terminals are shorted together. An overcurrent condition must exist for longer than the Overcurrent Fault Delay, t_{SCT}, before EF2 is set to low and the outputs are disabled. After the outputs have been disabled they remain latched in this state until the power is switched-off or the INH input is taken low.

The timer for the short detection delay, t_{SCT}, is started when an overcurrent first occurs. If the overcurrent is still present at the end of the short detection delay time, then a short fault will be generated and latched. If the overcurrent goes away before the short detection delay time is complete, then the timer is reset and a fault is generated.

Table 2: Phase Output Current versus Sense Resistor Value

V_{REF} = 1.2 V

R_S (mΩ)	I_{PHASE} (mA)	R_S (mΩ)	I_{PHASE} (mA)
75	1000	150	500
82.5	909	187	401
93.1	806	249	301
107	701	374	201
124	605	750	100

Table 3: Fault Table

EF1	EF2	Fault Condition	Latched	Outputs	Priority
H	H	No fault	–	Active	–
H	H	Undervoltage	No	Disabled	–
H	L	Overcurrent	Yes	Disabled	3
L	H	Open Load	No	Active	2
L	L	Overvoltage or Overtemperature	No	Disabled	1

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The overcurrent fault detection functions are described in detail as follows:

- *Short to Supply* – A short from any of the motor connections to the motor supply (VBB) is detected by monitoring the voltage across the low-side current sense resistor for each phase. This gives a direct measurement of the current through the low side of the bridge.
  When a low-side FET is in the on-state, the voltage across the sense resistor, under normal operating conditions, should never be more than the Maximum Sense Voltage, V_{SMAX}. In this state, an overcurrent is determined to exist when the voltage across the sense resistor exceeds the Low-Side Overcurrent Sense Voltage, V_{OCL}, typically 2 times V_{SMAX}. The actual overcurrent that V_{OCL} represents is determined by the value of the sense resistor and is typically 2 times I_{SMAX}.
- *Short to Ground* – A short from any of the motor connections to ground is detected by directly monitoring the current through each of the high-side FETs in each bridge

  When a high-side FET is in the on-state, the maximum current is typically always less than 1 A. In this state, an overcurrent is determined to exist when the current through the active high-side FET exceeds the High-Side Overcurrent Threshold, I_{OCH}. Note that, when a short to ground is present, the current through the high-side FET is limited to the High-Side Current Limit, I_{LIMH}, during the Overcurrent Fault Delay, t_{SCT}. This prevents large negative transients at the phase output pins when the outputs are switched-off.

Open Load. An open load fault condition is detected if the output current remains below the open load current level, I_{OLP}, for longer than the Open Load Delay, t_{dOLP}, 896 µs (typ).

When an open load fault appears, EF1 will go low indicating the fault but no other action will be taken. If the output current increases above the limit then the fault is removed and EF1 will go high.

Overvoltage. If the motor supply voltage, V_{BB}, rises above the overvoltage threshold, V_{BBOV}, the A4990 will disable the outputs and both EF1 and EF2 will go low indicating the fault. (Note that this setting of the EFx flags also can indicate an overtemperature fault condition.) The overvoltage level has a hysteresis voltage, $V_{BBOVhys}$. When the motor supply voltage goes below the overvoltage threshold by more than $V_{BBOVhys}$, then the outputs will be re-enabled and EF1 and EF2 will go high.

Overtemperature. If the chip temperature rises above the overtemperature threshold, T_{JF}, then EF1 and EF2 will go low and the outputs will be disabled. (Note that this setting of the EFx flags also can indicate an overvoltage fault condition.) Disabling the outputs helps to prevent a further increase in the chip temperature. The overtemperature level has a hysteresis temperature, T_{Jhys}. When the temperature drops below the overtemperature threshold by more than T_{Jhys}, then the outputs will be re-enabled and EF1 and EF2 will go high. If the temperature is not reduced sufficiently, then the A4990 will cycle in and out of overtemperature protection, depending on the thermal time constants of the circuit assembly and its environment.

Undervoltage. If the supply voltage, V_{BB}, goes below its undervoltage threshold, V_{BBUV}, or if the voltage of the internal regulator, V_{REG}, goes below its undervoltage threshold, V_{REGUV}, then the A4990 will disable all the bridge outputs. Note that this fault condition does not affect the fault flag outputs (EF1 and EF2).

The A4990 will re-enable the bridge outputs when both V_{BB} and V_{REG} have risen above the respective undervoltage turn-on voltages, after a short delay. Both V_{BB} and V_{REG} undervoltage detectors have hysteresis, V_{BBhys} and V_{REGhys} respectively, so the turn-on voltage for V_{BB} is $V_{BBUV} + V_{BBhys}$, and for V_{REG} is $V_{REGUV} + V_{REGhys}$.

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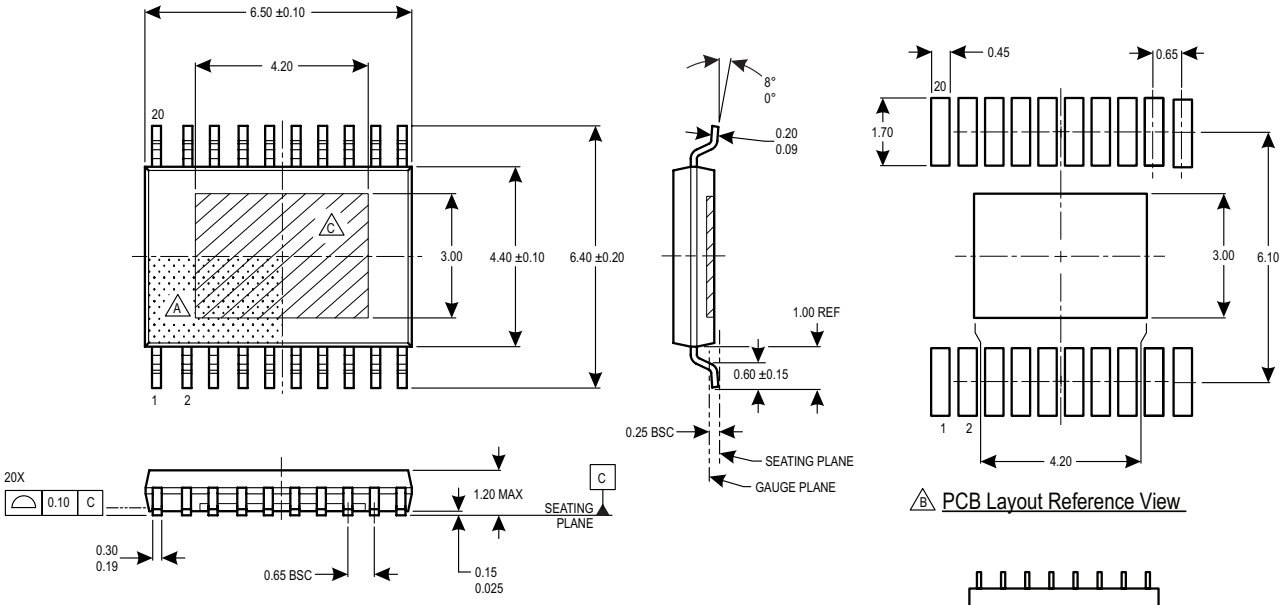
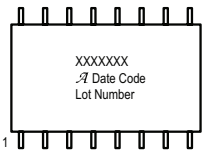
Package LP, 20-Pin TSSOP
with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference JEDEC MO-153ACT; Allegro DWG-0000379, Rev. 3)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



B PCB Layout Reference View



D Standard Branding Reference View

Line 1, 2, 3 = 8 characters

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-21M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface)

D Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
2	April 10, 2020	Minor editorial updates
3	April 5, 2022	Updated package drawing (page 12)

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