A6263

Protected LED Array Driver

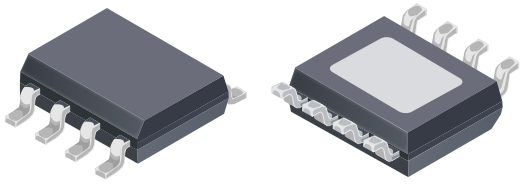
FEATURES AND BENEFITS

- AEC-Q100 qualified
- Total LED drive current up to 400 mA
- Current shared equally up to 100 mA by up to 4 strings
- Wide input voltage range of 6 to 50 V for start/stop, cold crank, and load dump requirements
- Low dropout voltage
- LED current levels set by single reference resistor
- LED string shorted to GND protection
- Overtemperature protection with optional thermal derating function
- Automotive temperature range

APPLICATIONS:

- Automotive interior and exterior lighting

PACKAGE: 8-pin SOICN with exposed thermal pad (suffix LJ)



Not to scale

DESCRIPTION

The A6263 is a linear, programmable current regulator providing up to 100 mA from each of 4 outputs to drive arrays of high brightness LEDs. Outputs can be connected in parallel or left unused, as required. The regulated LED current from each output, accurate to 5%, is set by a single reference resistor. Current matching in each string is better than 10% without the use of ballast resistors. Driving LEDs with constant current ensures safe operation with maximum possible light output.

The IC provides protection against the following common faults:

- LED string shorted to GND
- Single or multiple LED short
- LED string open
- IC pin open/short
- Overtemperature

If one LED string is open or shorted to ground, the offending string is disabled, while other LED strings continue to work.

A temperature monitor is included to reduce the LED drive current if the chip temperature exceeds a thermal threshold. If necessary, this thermal derating threshold can be adjusted or disabled.

The device comes in an 8-pin SOIC (package LJ) with exposed pad for enhanced thermal dissipation. It is lead (Pb) free, with 100% matte tin leadframe plating.

Typical Application Diagram

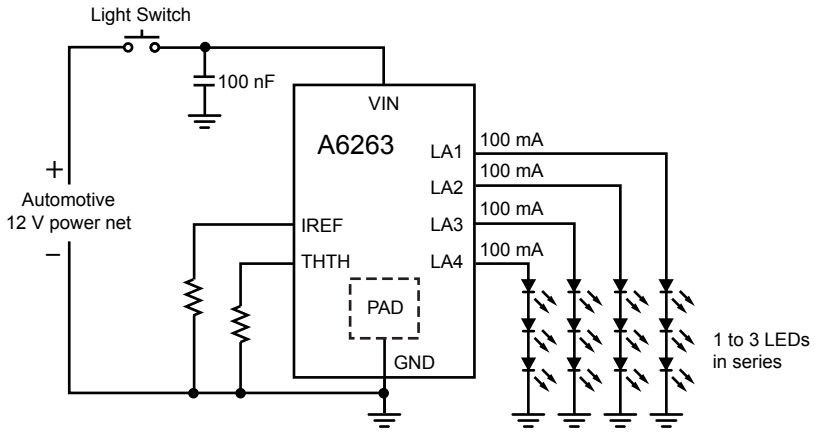


Figure 1. Typical application circuit

SELECTION GUIDE

Part Number	Ambient Operating Temperature, T_A (°C)	Packing*	Package
A6263KLJTR-T	–40 to 125	3000 pieces per 13-in. reel	8-pin SOICN with exposed thermal pad

*Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS*

Characteristic	Symbol	Notes	Rating	Unit
Input Supply Voltage	V_{IN}		–0.3 to 50	V
Pins LA1 through LA2			–0.3 to 50	V
Pins IREF and THTH			–0.3 to 6.5	V
Ambient Operating Temperature Range	T_A	K temperature range	–40 to 125	°C
Maximum Continuous Junction Temperature	T_J(max)		150	°C
Transient Junction Temperature	T_{tJ}	Overtemperature event not exceeding 10 s, lifetime duration not exceeding 10 h, guaranteed by design characterization	175	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

*Stresses beyond those listed in this table may cause permanent damage to the device. The Absolute Maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to Absolute Maximum-rated conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS*: May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard	35	ºC/W
		On 2-layer generic test PCB with 0.8 in.^{2} of copper area each side	62	ºC/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	ºC/W

*Additional thermal information available on the Allegro website.

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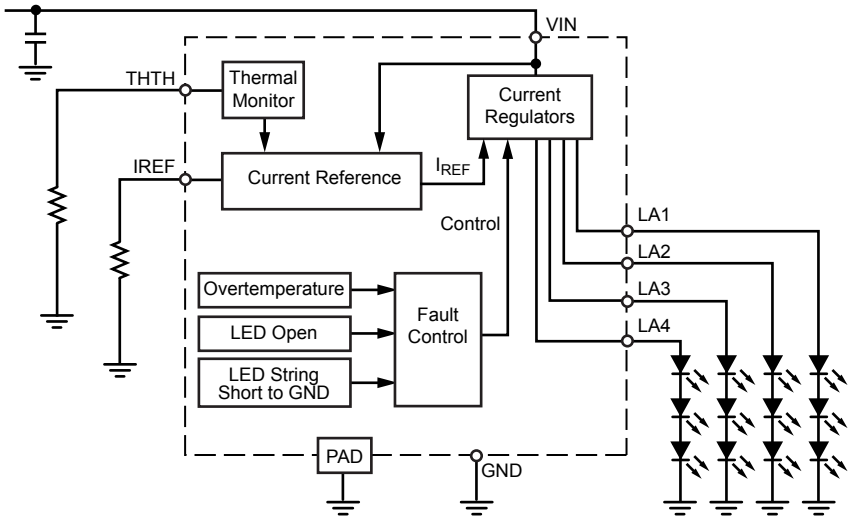
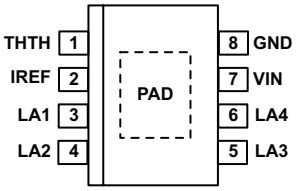
FUNCTIONAL BLOCK DIAGRAM



Pinout Diagram



Terminal List Table

Number	Name	Function
1	THTH	Thermal Threshold. Short this pin to ground to disable thermal derating feature, or leave open to enable. (Thermal shutdown function is always enabled.)
2	IREF	Connect a reference resistor between this pin and GND to set the LED current.
3	LA1	LED anode (+) connection 1*
4	LA2	LED anode (+) connection 2*
5	LA3	LED anode (+) connection 3*
6	LA4	LED anode (+) connection 4*
7	VIN	Input power to the IC. All LED current sources are enabled while V_{IN} is above UVLO level. Decouple with a 0.1 µF capacitor to GND near the IC.
8	GND	IC ground reference. Connect to ground plane(s) of the PCB using the shortest path possible.
–	PAD	Exposed pad of the package providing enhanced thermal dissipation. This pad must be connected to the ground plane(s) of the PCB with at least 8 vias located directly in the solder land for the pad.

* If any LAx pin is unused, tie it to the VIN pin. Do not leave it open or shorted to GND.

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ELECTRICAL CHARACTERISTICS [1]: Valid at T_A = 25°C, V_{IN} = 7 to 40 V; • indicates specifications valid across the full operating temperature range with $T_A = T_J$ = –40°C to 125°C and typical specifications at T_A = 25°C; unless otherwise specified

Characteristics	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
INPUT SUPPLY							
Operating Input Voltage Range [2]	V_{IN}		•	6	–	50	V
V_{IN} Quiescent Current	I_{INQ}	LAx pins connected to VIN	•	–	–	10	mA
Startup Time [3]	t_{ON}	V_{IN} > 7 V to I_{LA1} < –5 mA, R_{REF} = 125 Ω		–	20	–	µs
CURRENT REGULATION							
Reference Voltage	V_{IREF}	0.7 mA < I_{REF} < 8.8 mA	•	1.15	1.2	1.25	V
Reference Current Ratio	G_H	6 V < V_{IN} < 40 V		–	12.5	–	A/A
Current Accuracy [4]	E_{ILAx}	–10 mA > I_{LAx} > –100 mA	•	–5	±4	5	%
Current Matching [5]	E_{IMLAx}	–20 mA > I_{LAx} > –100 mA, V_{LAx} match to within 1 V	•	–	5	10	%
Output Current	I_{LAx}	I_{REF} = 8 mA	•	–105	–100	–95	mA
Maximum Output Current	I_{LAxmax}	I_{REF} = 9.2 mA		–	–	–110	mA
Minimum Drop-out Voltage	V_{DO}	$V_{IN} – V_{LAx}$, I_{LAx} = –100 mA		–	–	800	mV
		$V_{IN} – V_{LAx}$, I_{LAx} = –40 mA		–	–	660	mV
PROTECTION							
Short Detect Voltage	V_{SCD}	Measured at LAx	•	1.2	–	1.8	V
Short Circuit Source Current	I_{SCS}	Short present from LAx to GND	•	–2	–0.8	–0.5	mA
Short Release Voltage	V_{SCR}	Measured at LAx	•	–	–	1.9	V
Short Release Voltage Hysteresis	V_{SChys}	$V_{SCR} – V_{SCD}$	•	200	–	500	mV
Thermal Monitor Activation Temperature	T_{JM}	T_J with I_{SEN} = 90%, THTH open		95	115	130	°C
Thermal Monitor Slope	dI_{SEN}/dT_J	I_{SEN} = 50%		–3.5	–2.5	–1.5	%/°C
Thermal Monitor Low Current Temperature	T_{JL}	T_J at I_{SEN} = 25%, THTH open		120	135	150	°C
Overtemperature Shutdown	T_{JF}	Temperature increasing		–	170	–	°C
Overtemperature Hysteresis	T_{Jhys}	Recovery = $T_{JF} – T_{Jhys}$		–	15	–	°C

[1] For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2] Function is correct but parameters are not guaranteed outside the general limits (7 to 40 V).
[3] Ensured by design and characterization, not production tested.
[4] $E_{ILAx} = 100 \times [(| I_{LAx} | \times R_{REF} / 15) – 1]$, with I_{LAx} in mA and R_{REF} in kΩ.
[5] $E_{IMLA} = 100 \times \max (| I_{LAx} – I_{LA(AV)} |) / I_{LA(AV)}$, where $I_{LA(AV)}$ is the average current of all active outputs.

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FUNCTIONAL DESCRIPTION

The A6263 is a linear current regulator that is designed to provide drive current and protection for parallel strings of series-connected high brightness LEDs. It provides up to 4 matched programmable current outputs at up to 100 mA, with low minimum dropout voltages below the main supply voltage. For 12 V power net applications, optimum performance is achieved when driving 4 strings of 1 to 3 LEDs, at current up to 100 mA per string.

Current regulation is maintained and the LEDs protected during a short-to-ground at any point in the LED string. A short-to-ground on any regulator output terminal disables that offending string only. Similarly, in the case of an open output pin or an open-LED fault, all other LED strings remain in regulation. Individual outputs can be disabled by connecting the output to VIN. Multiple outputs can be connected in parallel to drive higher current LED strings.

Integrated thermal management reduces the regulated current level at high internal junction temperatures to limit power dissipation. This thermal threshold is programmable and can be disabled if necessary.

Pin Functions

VIN Supply to the control circuit and current regulators. A small value ceramic bypass capacitor, typically 100 nF, should be connected from close to this pin to the GND pin.

GND Ground reference connection. Should be connected directly to the ground plane of the circuit board.

IREF 1.2 V reference to set LED current. Connect resistor, R_{REF}, to GND to set reference current and thereby LED current.

THTH Sets the thermal monitor threshold, T_{JM}, where the output current starts to reduce with increasing temperature. Connecting THTH directly to GND will disable the thermal monitor function.

LA[1:4] Current source connected to the anode of the first LED in each string. Connect directly to VIN to disable the respective output. In this document "LAx" indicates any one of the outputs.

LED Current Level

The LED current is controlled by 4 matching linear current regulators, between the VIN pin and each of the LAx outputs. The basic equation that determines the nominal output current at each LAx pin is:

$$I_{LAx} = \frac{15}{R_{REF}} \quad (1)$$

where I_{LAx} is in mA and R_{REF} is in kΩ.

The output current may be reduced from the set level by the thermal monitor circuit.

Conversely the reference resistors may be calculated from:

$$R_{REF} = \frac{15}{I_{LAx}} \quad (2)$$

where I_{LAx} is in mA and R_{REF} is in kΩ.

For example, where the required current is 90 mA for both channels the resistor value will be:

$$R_{REF} = \frac{15}{90} = 0.167\ \text{k}\Omega$$

These equations completely define the output currents with respect to the setting resistors. However, for further reference, a more detailed description of the internal reference current calculations is included below.

It is important to note that because the A6263 is a linear regulator, the maximum regulated current is limited by the power dissipation and the thermal management in the application. All current calculations assume adequate heatsinking for the dissipated power. Thermal management is at least as important as the electrical design in all applications. In high current high ambient temperature applications, the thermal management is the most important aspect of the systems design. The application section below provides further detail on thermal management and the associated limitations.

Operation with Fewer LED Strings or Higher Currents

The A6263 may be configured to use fewer than all four LED strings, either by connecting outputs together for higher currents, or by connecting the output directly to VIN to disable the regulator for that output. It is also acceptable, though not recommended, to leave an unused LAx pin floating.

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Safety Features

The A6263 includes several features to ensure safe operation and to protect the LEDs and the IC:

- The current regulators between VIN and each LAx output provide a natural current limit due to the regulation.
- Each LAx output includes a short-to-ground detector that will disable the output to limit the dissipation.
- An open circuit on any output will disable the affected string only.
- The thermal monitor reduces the regulated current as the temperature rises above a programmable thermal threshold.
- Thermal shutdown completely disables the outputs under extreme overtemperature conditions.

Temperature Monitor

A temperature monitor function reduces the LED current as the silicon junction temperature of the IC increases (see figure 2). By mounting the A6263 on the same thermal substrate as the LEDs, this feature can also be used to limit the dissipation of the LEDs.

As the junction temperature of the A6263 increases, the regulated current level is reduced, reducing the dissipated power in the A6263 and in the LEDs. The current is reduced from the 100% level at typically 2.5% per degree Celsius until the point at which the current drops to 25% of the full value, defined at T_{JL}. Above this temperature the current will continue to reduce at a lower rate until the temperature reaches the overtemperature shutdown threshold temperature, T_{JF}.

The temperature at which the current reduction begins can be adjusted by changing the voltage on the THTH pin. When THTH is left open the temperature at which the current reduction begins is defined as the thermal monitor activation temperature, T_{JM}, and is specified, in the Electrical Characteristics table, at the 90% current level.

Thermal monitor activation temperature can be set to a desired level by setting the voltage on the THTH pin (V_{THTH}). There is an internal 1 V source connected with a series resistor to the

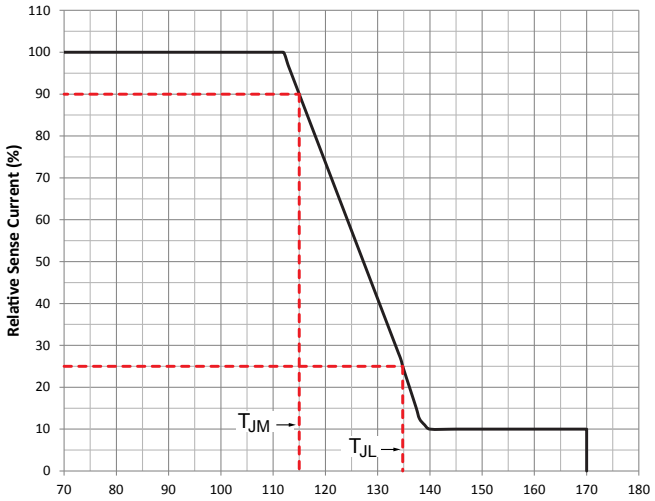

Figure 2. Temperature monitor current reduction.

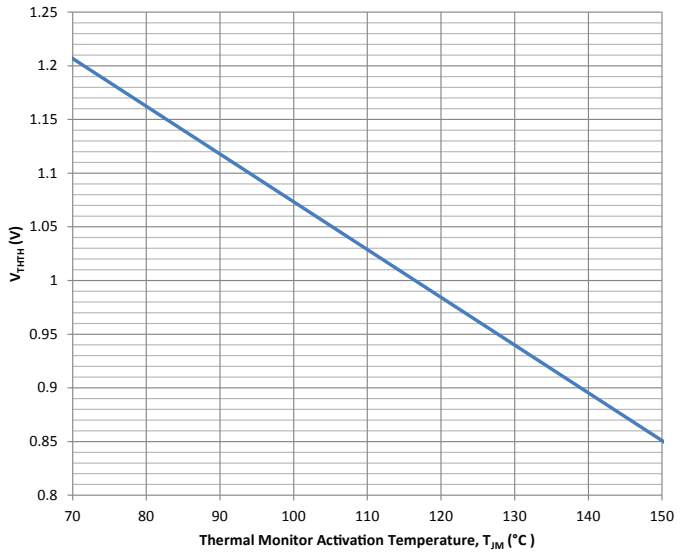

Figure 3a. Relationship between T_{JM} and V_{THTH}.

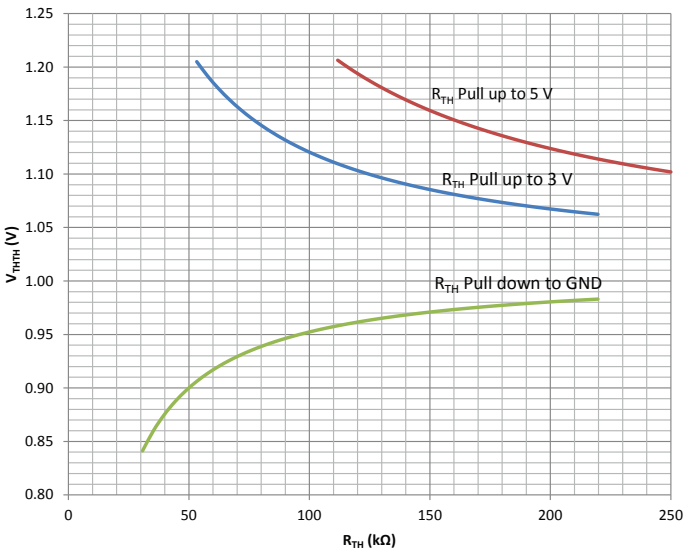

Figure 3b. Typical Resistor Values to Set Voltage on THTH Pin.

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THTH pin inside the IC. A resistor connected between THTH and GND will reduce V_{THTH} and increase T_{JM}. A resistor connected between THTH and a reference supply greater than 1 V will increase V_{THTH} and reduce T_{JM}. Figure 3a shows the relationship between T_{JM} and V_{THTH} while Figure 3b shows typical resistor values, either pull up or pull down, to set the voltage on THTH pin. Now, based on the T_{JM} requirement, estimate the required V_{THTH} voltage from Figure 3a, and then, depending on the V_{THTH} value, decide the THTH pin resistor from Figure 3b. THTH pin resistor may either pull up or pull down depending on V_{THTH}. As an example, if T_{JM} of 90°C is required, then from Figure 3a, V_{THTH} should be 1.115 V. To achieve this voltage, use Figure 3b to estimate THTH pin resistor (R_{TH}). If the pull-up voltage is 5 V, then a 211 kΩ resistor should be used. If the pull-up voltage is 3 V, use a 100 kΩ resistor.

In extreme cases, if the chip temperature exceeds the overtemperature limit, T_{JF}, all regulators will be disabled. The temperature will continue to be monitored and the regulators reactivated when the temperature drops below the threshold provided by the specified hysteresis.

Note that it is possible for the A6263 to transition rapidly between thermal shutdown and normal operation. This can happen if the thermal mass attached to the exposed thermal pad is small and T_{JM} is increased to close to the shutdown temperature. The period of oscillation will depend on T_{JM}, the dissipated power, the thermal mass of any heatsink present, and the ambient temperature.

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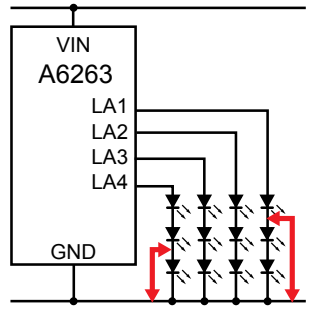
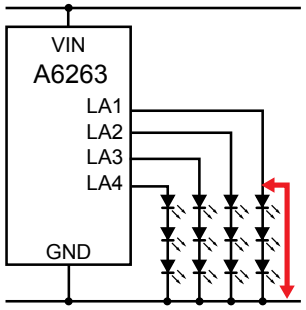
Fault Cases



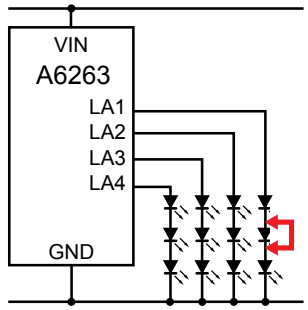
Case A: Any LED cathode short to GND

Outcome: IC continues to regulate current through all LED strings. Current matching may suffer.



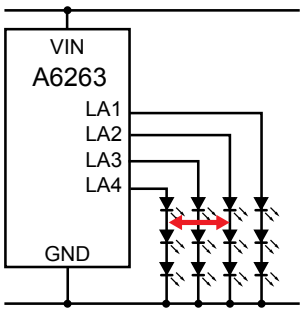
Case B: LAx pin or high-side of LED string shorted to GND

Outcome: IC detects pin-to-GND short before enabling current regulators. Offending LED string disabled. All other strings remain active.



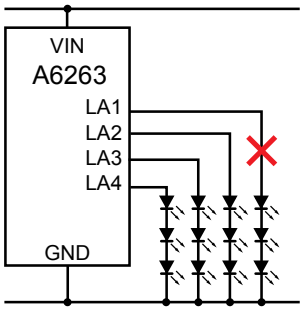
Case C: Single LED in a string shorted

Outcome: IC continues to regulate current through all LED strings. Current matching may suffer.



Case D: Short between LED strings

Outcome: LED current regulators continue to operate normally, but current matching between LED strings will be affected.



Case E: LAx pin or high-side of LED string open

Outcome: No current through the offending LED string. All other strings remain active.

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APPLICATION INFORMATION

Power Dissipation

The most critical design considerations when using a linear regulator such as the A6263 are the power produced internally as heat and the rate at which that heat can be dissipated.

There are three sources of power dissipation in the A6263:

- The quiescent power to run the control circuits
- The power in the reference circuit
- The power due to the regulator voltage drop

The elements relating to these dissipation sources are illustrated in figure 4.

Quiescent Power The quiescent power is the product of the quiescent current, I_{INQ}, and the supply voltage, V_{IN}, and is not related to the regulated current. The quiescent power, P_Q, is therefore defined as:

$$P_Q = V_{IN} \times I_{INQ} \quad (3)$$

Reference Power The reference circuit draws the reference current from the supply and passes it through the reference resistor to ground. The reference current is 8% of the output current on any one active output. The reference circuit power is the product of the reference current and the difference between the supply voltage and the reference voltage, typically 1.2 V. The reference power, P_{REF}, is therefore defined as:

$$P_{REF} = \frac{(V_{IN} - V_{REF}) \times V_{REF}}{R_{REF}} \quad (4)$$

Regulator Power In most application circuits the largest dissipation will be produced by the output current regulators. The power dissipated in each current regulator is simply the product of the output current and the voltage drop across the regulator.

The total current regulator dissipation is the sum of the dissipation in each output regulator. The regulator power for each output is defined as:

$$P_{REGx} = (V_{IN} - V_{LEDx}) \times I_{LEDx} \quad (5)$$

where x is 1, 2, 3, or 4.

Note that the voltage drop across the regulator, V_{REG}, is always greater than the specified minimum drop-out voltage, V_{DO}. The output current is regulated by making this voltage large enough to provide the voltage drop from the supply voltage to the total forward voltage of all LEDs in series, V_{LED}.

The total power dissipated in the A6263 is the sum of the quiescent power, the reference power, and the power in each of the four regulators:

$$P_{DIS} = P_Q + P_{REF} + P_{REGA} + P_{REGB} + P_{REGC} + P_{REGD} \quad (6)$$

The power that is dissipated in each string of LEDs is:

$$P_{LEDx} = V_{LEDx} \times I_{LEDx} \quad (7)$$

where x is A, B, C, or D, and V_{LEDx} is the voltage across all LEDs in the string.

From these equations it can be seen that, if the power in the A6263 is not limited, then it will increase as the supply voltage increases but the power in the LEDs will remain constant.

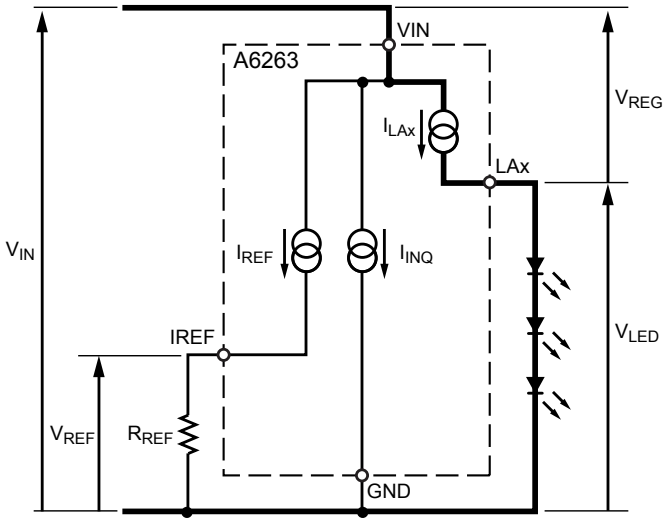

Figure 4. Internal power dissipation sources.

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Binning Resistor Arrangement

An external binning resistor can be connected in series with the IREF pin to set appropriate current through various LED batches. A filter capacitor of 100 nF should be placed after R_{REF1} as shown in Figure 5.

$$I_{LAx}(min) = (15) \div (R_{REF1} + R_{REF2}) \quad (8)$$

$$I_{LAx}(max) = (15) \div R_{REF1} \quad (9)$$

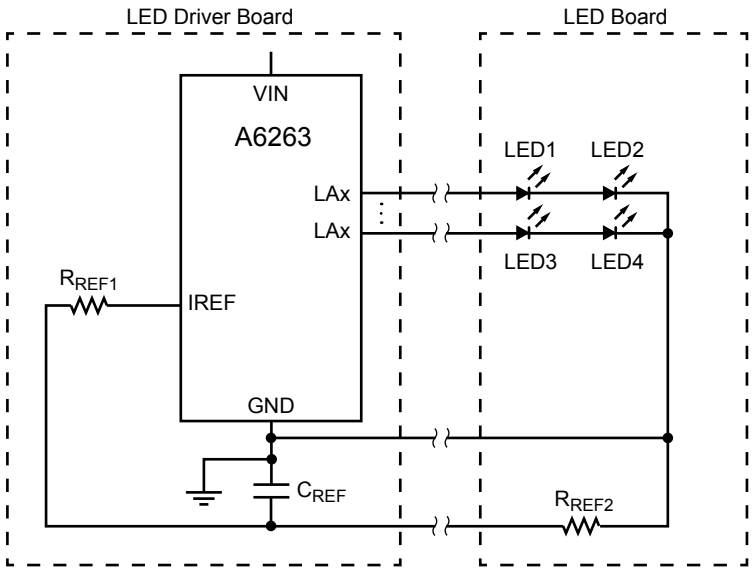

Figure 5. Application Circuit for Binning – Current-setting resistor (R_{REF2}) can be placed on LED board for different bins of LEDs

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Dissipation Limits

There are two features limiting the power that can be dissipated by the A6263: thermal shutdown and thermal foldback.

Thermal Shutdown. If the thermal foldback feature is disabled by connecting the THTH pin to GND, or if the thermal resistance from the A6263 to the ambient environment is high, then the silicon temperature will rise to the thermal shutdown threshold and the current will be disabled. After the current is disabled the power dissipated will drop and the temperature will fall. When the temperature falls by the hysteresis of the thermal shutdown circuit, then the current will be re-enabled and the temperature will start to rise again. This cycle will repeat continuously until the ambient temperature drops or the A6263 is switched off. The period of this thermal shutdown cycle will depend on several electrical, mechanical, and thermal parameters, and could be from a few milliseconds to a few seconds.

Thermal Foldback. If there is a good thermal connection to the A6263, then the thermal foldback feature will have time to act. This will limit the silicon temperature by reducing the regulated current and therefore the dissipation. The thermal monitor will reduce the LED current as the temperature of the A6263 increases above the thermal monitor activation temperature, T_{JM}.

Thermal Dissipation

The amount of heat that can pass from the silicon of the A6263 to the surrounding ambient environment depends on the thermal resistance of the structures connected to the A6263. The thermal resistance, $R_{\theta JA}$, is a measure of the temperature rise created by power dissipation and is usually measured in degrees Celsius per watt (°C/W).

The temperature rise, ΔT, is calculated from the power dissipated, P_D, and the thermal resistance, $R_{\theta JA}$, as:

$$\Delta T = P_D \times R_{\theta JA} \quad (10)$$

A thermal resistance from silicon to ambient, $R_{\theta JA}$, of approximately 35°C/W can be achieved by mounting the A6263 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the A6263. Additional improvements in the range of 20% may be achieved by optimizing the PCB design.

Optimizing Thermal Layout

The features of the printed circuit board, including heat conduction and adjacent thermal sources such as other components, have a very significant effect on the thermal performance of the device. To optimize thermal performance, the following should be taken into account:

- The device exposed thermal pad should be connected to as much copper area as is available.
- Copper thickness should be as high as possible (for example, 2 oz. or greater for higher power applications).
- The greater the quantity of thermal vias, the better the dissipation. If the expense of vias is a concern, studies have shown that concentrating the vias directly under the device in a tight pattern, as shown in figure 6, has the greatest effect.
- Additional exposed copper area on the opposite side of the board should be connected by means of the thermal vias. The copper should cover as much area as possible.
- Other thermal sources should be placed as remote from the device as possible

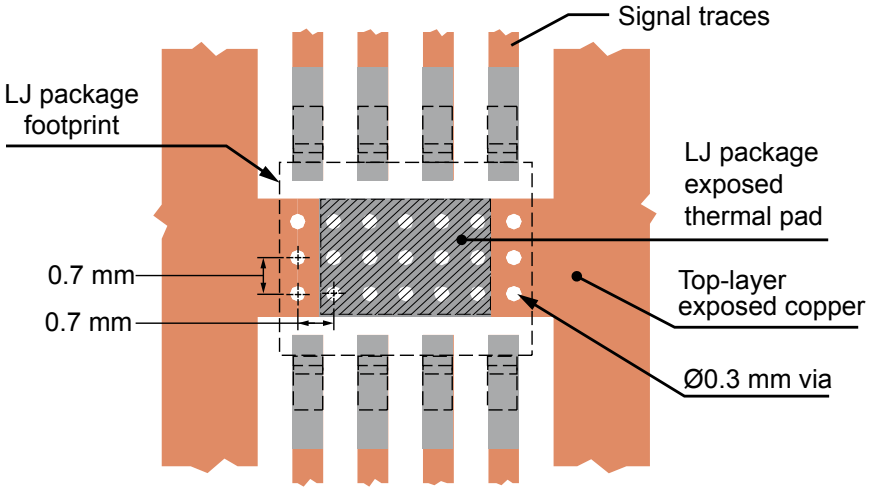

Figure 6. Suggested PCB layout for thermal optimization (maximum available bottom-layer copper recommended)

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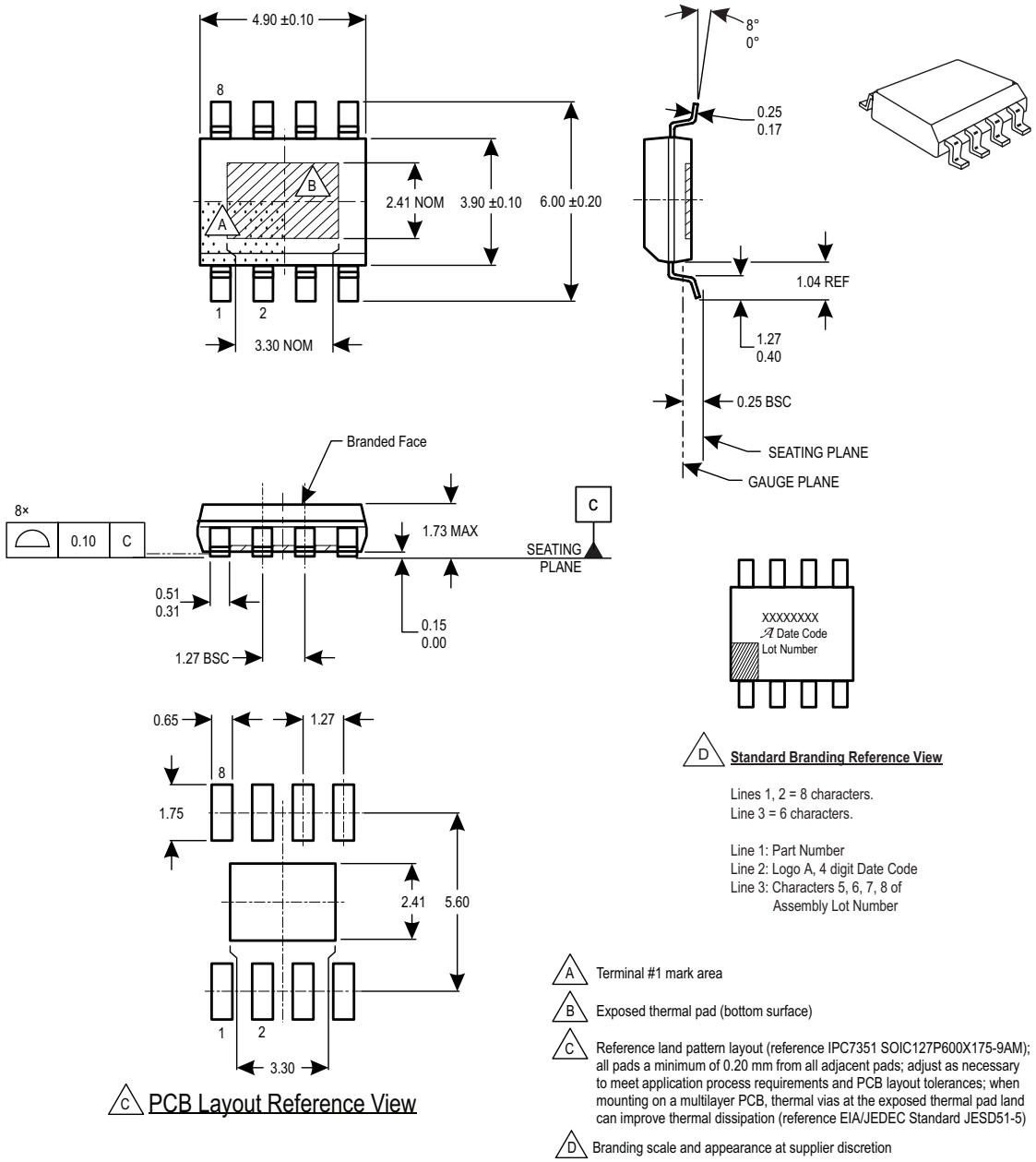
Package LJ, 8-Pin SOICN with Exposed Thermal Pad

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000380, Rev. 2 and JEDEC MS-012BA)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



C PCB Layout Reference View

D **Standard Branding Reference View**

Lines 1, 2 = 8 characters.
Line 3 = 6 characters.

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Characters 5, 6, 7, 8 of
Assembly Lot Number

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Branding scale and appearance at supplier discretion

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Revision History

Number	Date	Description
1	June 25, 2015	Temperature Monitor text on page 6 updated to match EC table: derating slope is -2.5% per °C
2	July 27, 2016	Revised Temperature Monitor section (page 6-7) and added Binning Resistor Arrangement section (page 10)
3	May 29, 2020	Minor editorial updates
4	June 2, 2022	Updated package drawings (page 12) and minor editorial updates

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