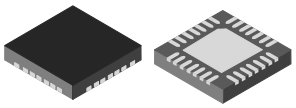
Automotive Three-Phase and Battery Isolator MOSFET Driver

FEATURES AND BENEFITS

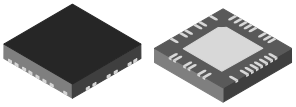
- Five floating N-channel MOSFET drives
- Maintains V_{GS} with 100 kΩ gate-source resistors
- Integrated charge pump controller
- 4.5 to 85 V supply voltage operating range
- Supports source-to-source and drain-to-drain battery MOSFET isolation
- V_{CP} and V_{GS} undervoltage protection
- 150°C ambient (165°C junction) continuous
- Fully integrated diagnostics for safe motor phase and battery disconnect
- Extensive programmable diagnostics
- Diagnostic verification
- Automotive AEC-Q100 qualified
- ASIL-Compliant: ASIL B safety element out-of-context (SEooC) developed in accordance with ISO 26262, when used as specified in the safety manual

ISO 26262 ASIL Compliant

PACKAGES



28-contact QFN with wettable flanks and exposed pad (suffix ET)



28-contact QFN with wettable flanks and exposed pad (suffix EV)

Not to scale

DESCRIPTION

The A89103 is an N-channel power MOSFET driver capable of controlling five MOSFETs to provide motor-phase isolation and supply isolation in three-phase BLDC applications. Three floating gate-drive outputs maintain phase-isolator power MOSFETs in the on state, over the full supply range, with high-phase voltage and high dv/dt on the motor-phase connection for 12 V and 48 V systems. Two additional floating gate drivers are provided to isolate the battery supply voltage during reverse-battery or short-circuit conditions. The A89103 supports both source-to-source and drain-to-drain battery MOSFET isolation. An integrated charge-pump regulator provides the above-battery-supply voltage necessary to continuously maintain the power N-channel MOSFETs in the on state. The charge pump maintains sufficient gate drive power (> 7.5 V) for battery voltages down to 4.5 V with 100 kΩ gate source resistors.

The five floating gate drives can be configured, monitored, and controlled through the SPI interface. When not in use, the A89103 can be placed in a low-power sleep mode.

Undervoltage monitors check that the pumped supply voltage and the gate drive outputs are high enough to ensure that the MOSFETs are maintained in a safe conducting state.

The A89103 is supplied in a 28-contact wettable-flank quad flat no-lead (QFN) package (suffix ET), and 28-contact wettable-flank QFN (suffix EV), both with exposed pads for enhanced thermal dissipation. They are lead (Pb) free, with 100% matte tin leadframe plating.

TYPICAL APPLICATIONS

- Three-phase and battery isolation for ASIL systems up to level B
- Electric power steering (EPS)
- Electric braking (EMB)
- Redundant motor-control systems

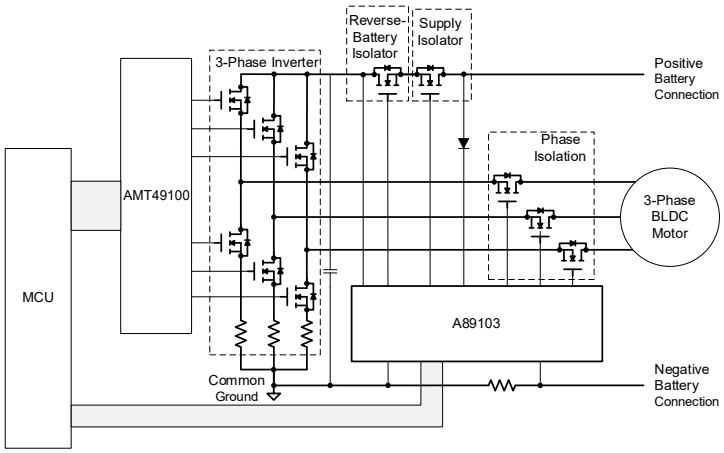


Figure 1: Typical Application Diagram

SPECIFICATIONS

SELECTION GUIDE

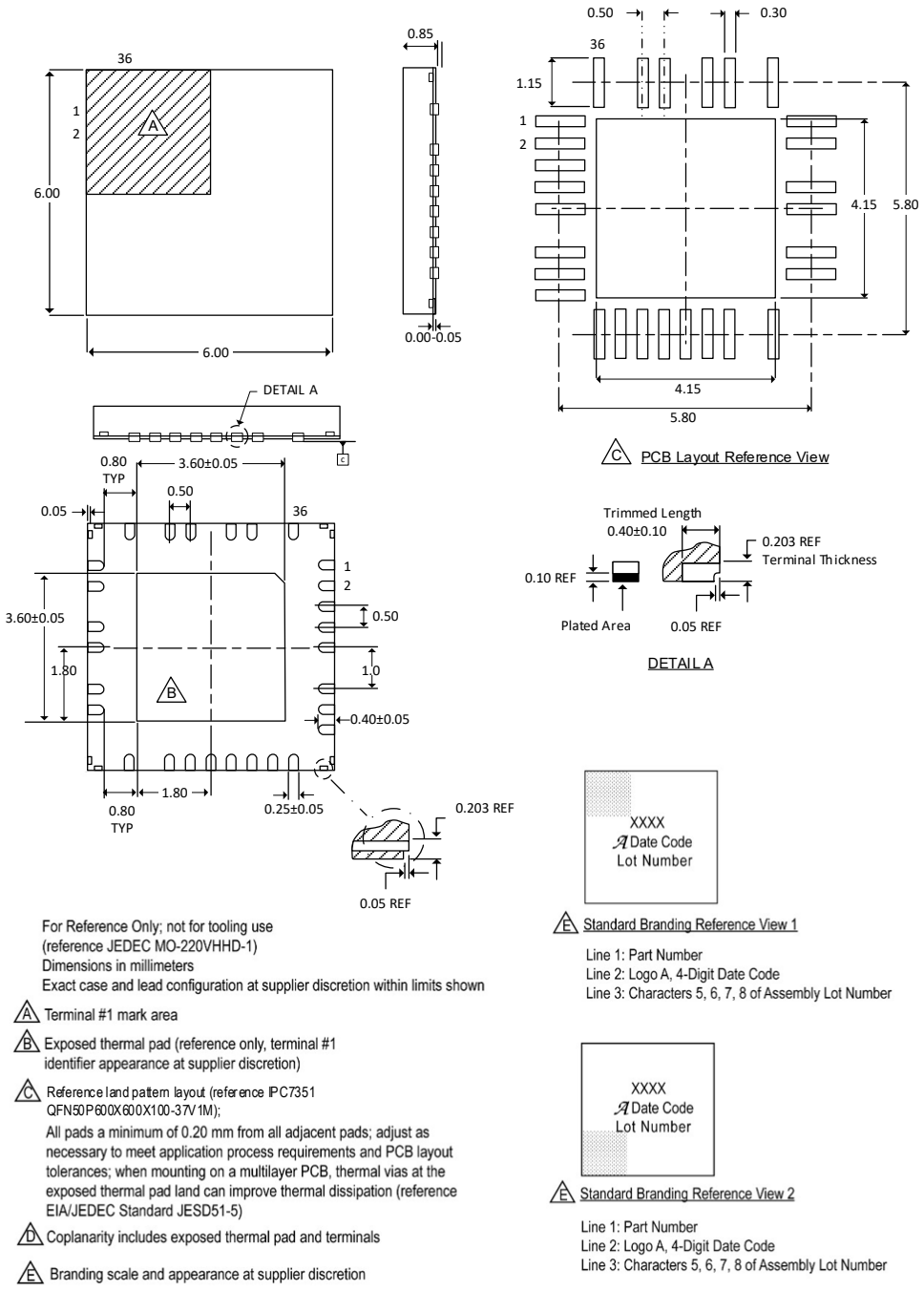
Part Number	I/O Logic	Packing	Package
A89103KETSR-3	3.3 V	1500 pieces per 13-inch reel	5 mm × 5 mm × 0.75 mm 28-contact QFN with exposed thermal pad
A89103KETSR-5	5 V		
A89103KEVSR-3	3.3 V	1500 pieces per 13-inch reel	6 mm × 6 mm × 0.9 mm 28-contact QFN with exposed thermal pad
A89103KEVSR-5	5 V		

ESD RATINGS

ESD Information for Handling of ESDS in an ESD Protected Area
CDM (AEC-Q100-011JS-002: CDM withstand threshold of 1000 V; CDM Class C3
HBM (AEC-Q100-002/JS-00102017): HBM withstand threshold of 2000 V; HBM Class 2

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWINGS



For Reference Only; not for tooling use
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P600X600X100-37V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 2: Package EV, 28-Contact QFN with Exposed Pad

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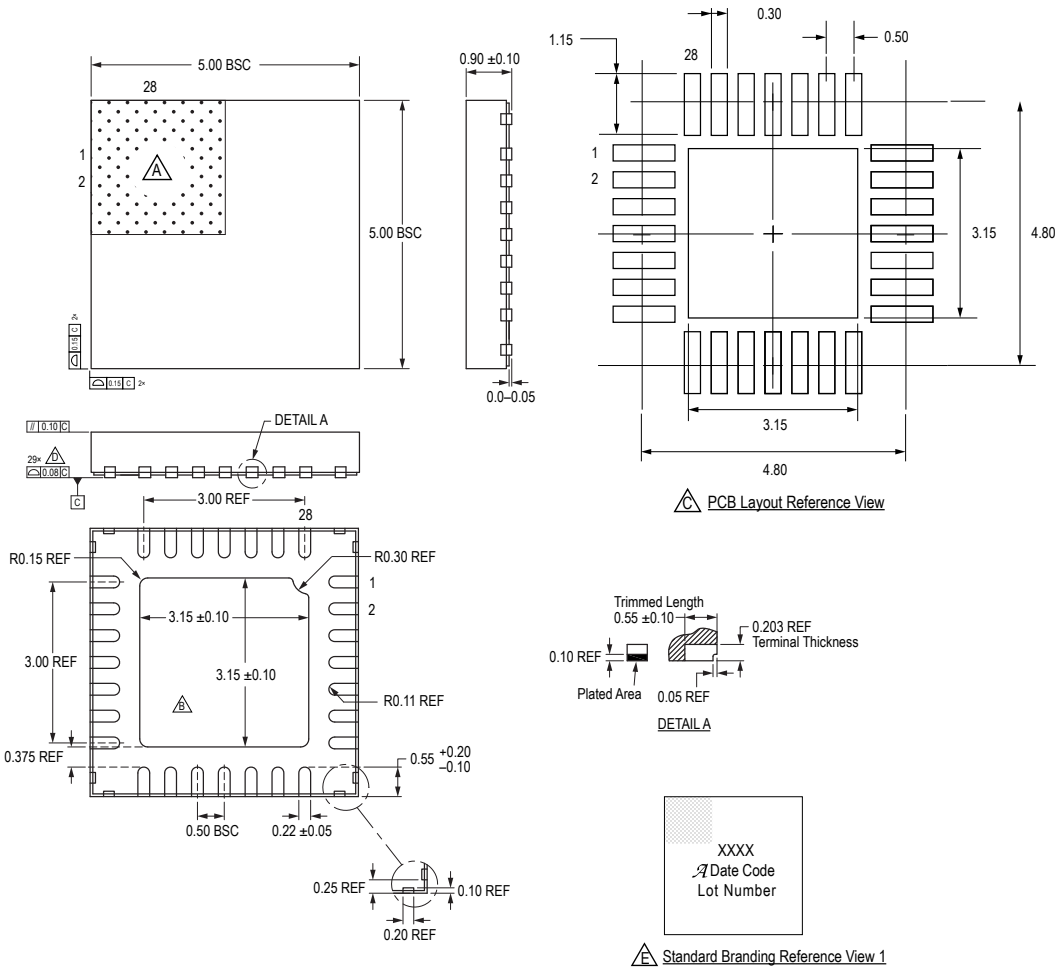
(Reference Allegro DWG-0000378, Rev. 3 or JEDEC MO-220VHHD-1)
NOT TO SCALE
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

Figure 3: Package ET, 28-Contact QFN with Exposed Pad

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Revision History

Number	Date	Description
–	October 31, 2023	Preliminary
1	January 3, 2024	Updated datasheet status to Final; updated Charge Pump Regulator section (page 17) and Package Drawing (page 74).
2	February 1, 2024	Removed “pending assessment” wording (page 1).
3	May 7, 2024	Minor editorial updates (pages, 11, 28, 40, 46), Updated Charge Pump Regulator wording (page 17), Cyclic Redundancy Check (pages 68, 69)
4	September 27, 2024	Corrected SPI watchdog timeout in WDT [2:0] configuration register (pages 42 and 46), corrected enable/disable serial register (page 45), and added errata appendix (pages 76 and 77).
5	February 13, 2025	Added packing information to selection guide (page 3); errata appendix removed.
	April 23, 2025	Changed long-form datasheet to limited distribution and created short-form datasheet; modified ASIL description for clarity (page 1); updated table of contents (page 2); updated packing information and ESD specifications (page 3); updated specification for VBB sleep current at 85°C, divider off-state leakage current (noted as guaranteed by design and characterization), VBRG comparator positive threshold, and footnote numbering (pages 9 through 12); added overtemperature shutdown (page 25); added comment for application limitation for OCP deglitch timings (pages 26 and 27); and reformatted document for interactive PDF capability (all pages)

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