A89211/12

MCU with 90 V MOSFET Driver

FEATURES AND BENEFITS

- 5.5 to 90 V supply voltage operating range
- 60 V part variant available (A89211)
- 32-bit ARM Cortex-M4 CPU core
  - □ Up to 40 MHz clock frequency
  - □ On-chip ±1% accurate oscillator
  - □ Programmable clock generator
  - □ One clock per machine cycle architecture
  - □ Direct memory access (DMA)
  - □ 16-level interrupt handler
  - □ SW-DP 2-wire debug

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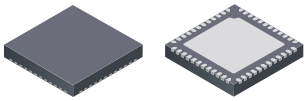
APPLICATIONS

- Optimized for 12 to 56 V battery BLDC motor modules
- Cordless power tools
- 48 V e-bike

PACKAGE



48-pin 7 mm × 7 mm QFN with exposed thermal pad and wettable flank (suffix EV)

Not to scale

DESCRIPTION

The A89211/12 is a high-performance processor with integrated three-phase gate drive and precision current sense capability. The A89211/12 is designed for use with advanced stand-alone three-phase BLDC and PMSM motor control applications.

The processor uses an ARM Cortex-M4 CPU core running at 40 MHz, giving up to 50 MIPS performance. The processor capability is further enhanced by peripheral functions specifically designed for motor control applications. These include a PWM generator and sense current capture systems capable of providing up to 12-bit control precision at up to 20 kHz PWM frequency.

Sixteen general purpose I/O ports provide access to programmable serial communication interfaces and analog and digital inputs and outputs.

The gate driver is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a three-phase bridge arrangement and is specifically designed for power applications with high-power inductive loads, such as BLDC motors.

A unique charge pump regulator provides the supply for the

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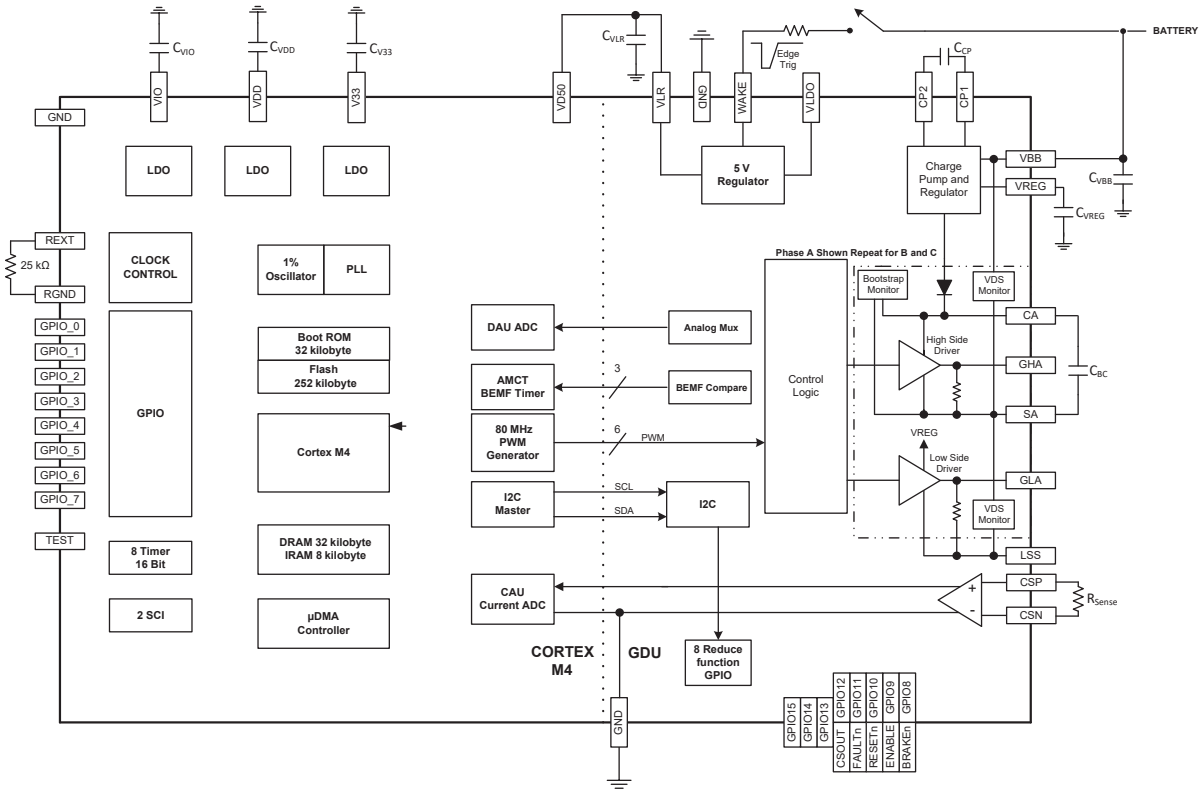

Figure 1: A89211/12 Block Diagram

FEATURES AND BENEFITS (continued)

- On-chip memory
  - □ Up to 252 kB flash
  - □ 32 kB DRAM
  - □ 8 kB IRAM
  - □ 32 kB boot ROM
- 3-phase bridge MOSFET driver with bootstrap gate drive for N-channel MOSFET bridge
- Charge pump for low supply voltage operation.
- 3.3 V or 5 V CMOS compatible logic I/O
- 80 MHz PWM generator
  - □ 12-bit PWM at 20 kHz
  - □ Programmable bemf and current sample control
- Programmable high-performance current sense amplifier
  - □ 3 × 11 bit, 1 µs ADC for current measurement
- 12-bit 1 µs data acquisition ADC with 16-channel mux
- 8 general purpose I/O ports (GPIO)
- 8 general purpose timers
- 2 serial communication interfaces (SCI)
- 3-phase BEMF detector
- Integrated power management
- VDS, UVLO, and thermal shutdown diagnostic
- Latched TSD with fault output

DESCRIPTION (continued)

MOSFET gate drive for battery voltages down to 7 V and allows the A89211/12 to operate with a reduced gate drive voltage down to 5.5 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs.

The power supply unit provides and manages all internal supplies from a single 5.5 to 60 V supply. The MCU section can also operate with an independent single 5 V supply.

Integrated programmable diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions.

The A89211/12 is supplied in a 48-lead QFN package with exposed thermal pad and wettable flank. This package is lead (Pb) free with 100% matte-tin leadframe plating.

SELECTION GUIDE

Part Number	Rated Voltage (V)	GPIO Voltage(V)	Flash Size (kB)	Package	Packing
A89211GEVSR [1]	60	5	252	7 mm × 7 mm, 0.9 mm nominal height 48-terminal QFN with exposed thermal pad and wettable flank	4000 pieces per 13-in. reel
A89212GEVSR [1]	90	5	252		

[1] The following variants are also offered:

Part Number	Rated Voltage (V)	GPIO Voltage (V)	Flash Size (kB)
• A89211GEVSR-A	60	3.3	128
• A89212GEVSR-A	90	3.3	128

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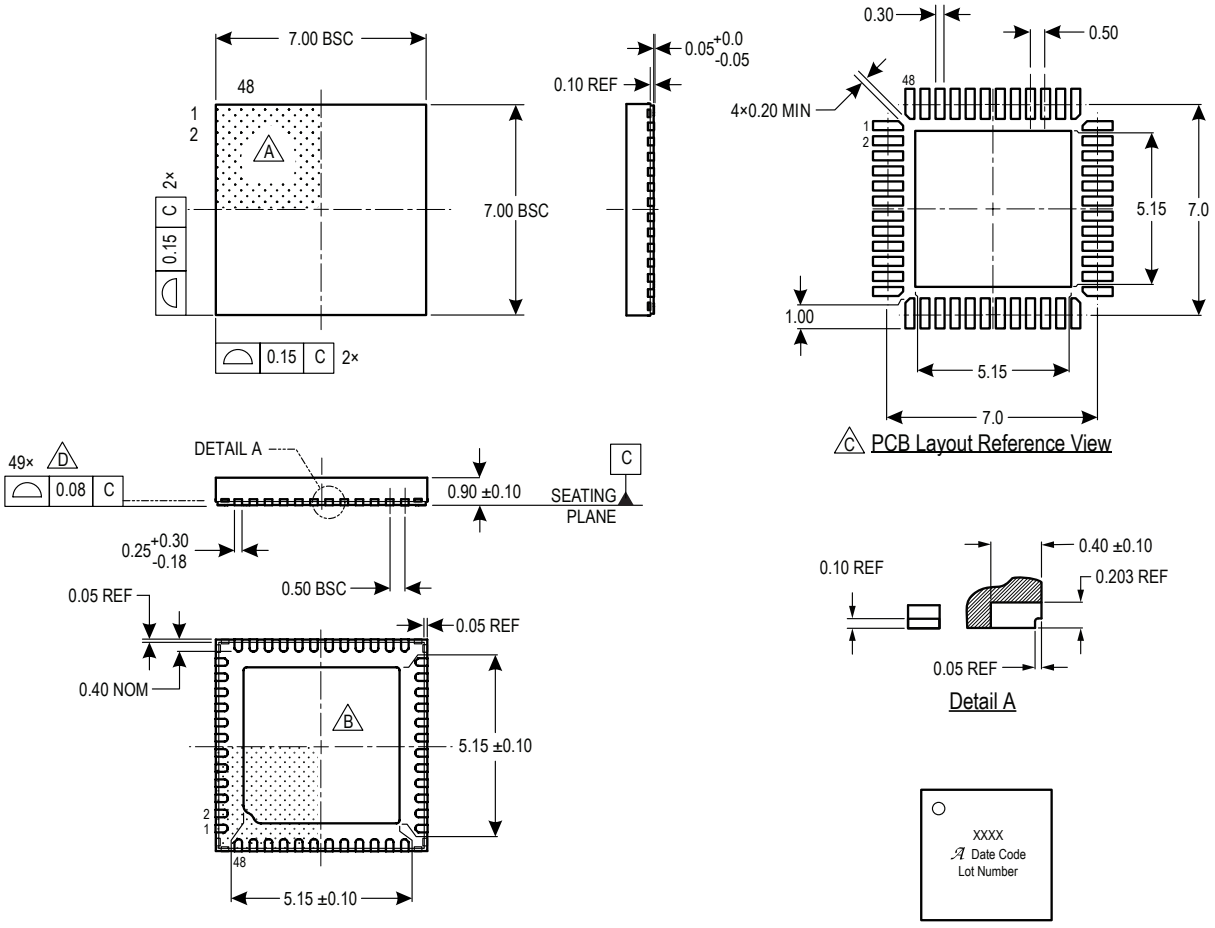
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000378, Rev. 3)
Dimensions in millimeters
NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P700X700X100-49M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion

E Standard Branding Reference View
Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Figure 2: 48-Lead QFN With Exposed Pad (Suffix EV)

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REVISION HISTORY

Number	Date	Description
–	December 6, 2024	Initial release
1	March 25, 2025	Updated block diagram (page 1), Selection Guide table (page 2), GPIO Terminals and Logic Inputs notes and footnotes (page 4), VREG Output Voltage min value and VLR Output Overcurrent Limit test conditions (page 8), CAU diagram (page 9), Boot ROM, RAM, and Flash sections (page 9), AOUT Divider Ratio and AOUT Accuracy characteristic names (page 19), Gate Drive Pull-Up Resistance maximum value (page 25), and VLR Undervoltage minimum value (page 26).

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