ACS37611

Coreless, High Precision, Hall-Effect Current Sensor IC
with Common-Mode Field Rejection, Overcurrent and Overtemperature Detection

FEATURES AND BENEFITS

- Eliminates need for concentrator core or shield
- Contactless, lossless, noninvasive current sensing
- Suited for applications where current flows through busbar or PCB
- High operating bandwidth: DC to 250 kHz
- Overcurrent (OCF) and overtemperature (OTF) detection on the fault pin
- Differential Hall sensing rejects common-mode magnetic fields
- Very fast response time (<2 µs typ)
- Wide sensing range (3 to 28 mV/G)
  - □ Ideal for sensing currents from 100 A to >4000 A
- Factory-programmed segmented linear temperature compensation (TC) provides low thermal drift
  - □ Sensitivity ±1% (typ)
  - □ Offset ±3 mV (typ)
- Customer-programmable, high-resolution offset and sensitivity trim
- Wide spacing of Hall elements for improved SNR and thermal performance
- Ultra-sensitive Hall elements for improved noise performance

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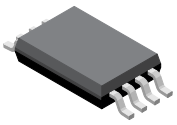
PACKAGE:

8-pin TSSOP package (suffix LU)



Not to scale

DESCRIPTION

The Allegro ACS37611 current sensor IC enables low-cost solutions for AC and DC current sensing without the need for an external field concentrator core or a U-shaped magnetic shield. It is designed for applications where hundreds or thousands of amperes flow through a busbar or PCB.

Current flowing through a busbar or PCB trace generates a magnetic field that is sensed by the monolithic, low-offset, linear Hall IC. The differential sensing topology virtually eliminates all types of error caused by common-mode stray magnetic fields. The wide spacing between the differential Hall elements (2.58 mm) coupled with the increased sensitivity of each Hall element enable the ACS37611 to achieve a superior signal-to-noise ratio (SNR) and improved resolution. While not mandatory, a notch or slit in the current-carrying busbar or PCB copper trace provides further improvements to system SNR. High isolation is achieved via the no-contact nature of this simple assembly.

The ACS37611 is offered with regular and low-power mode, enabling customers to achieve optimal SNR and power consumption. A dedicated user-programmable overcurrent and overtemperature fault pin and a slew of built-in diagnostics, including broken-ground and VCC detection, make it ideal

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TYPICAL APPLICATIONS

- High-voltage traction motor inverter
- 48 V/12 V auxiliary inverter
- Heterogeneous redundant battery monitoring
- Overcurrent detection
- DC-to-DC converter
- Smart fuse
- Power distribution unit (PDU)
- Power supply

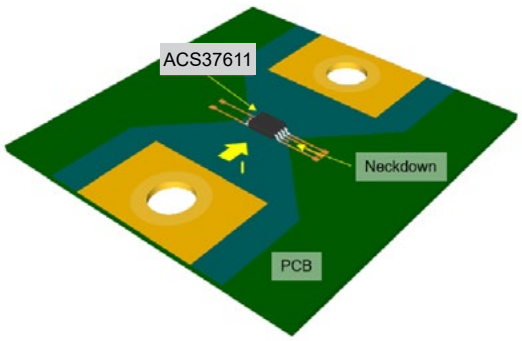


Figure 1: Current Through PCB

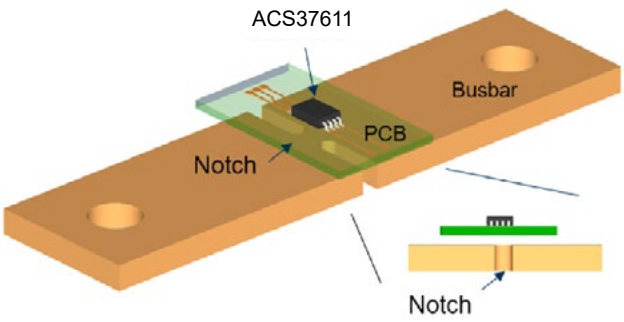


Figure 2: Current Through Busbar

FEATURES AND BENEFITS (continued)

- Wide ambient temperature range: –40°C to 150°C
- 5 V single supply operation
- Programmable through output pin or through dedicated programming pin for easier device programming
- AEC-Q100 Grade 0, automotive qualified
- Monolithic Hall IC for high reliability
- Surface-mount, small-footprint, low-profile TSSOP-8 package

DESCRIPTION (continued)

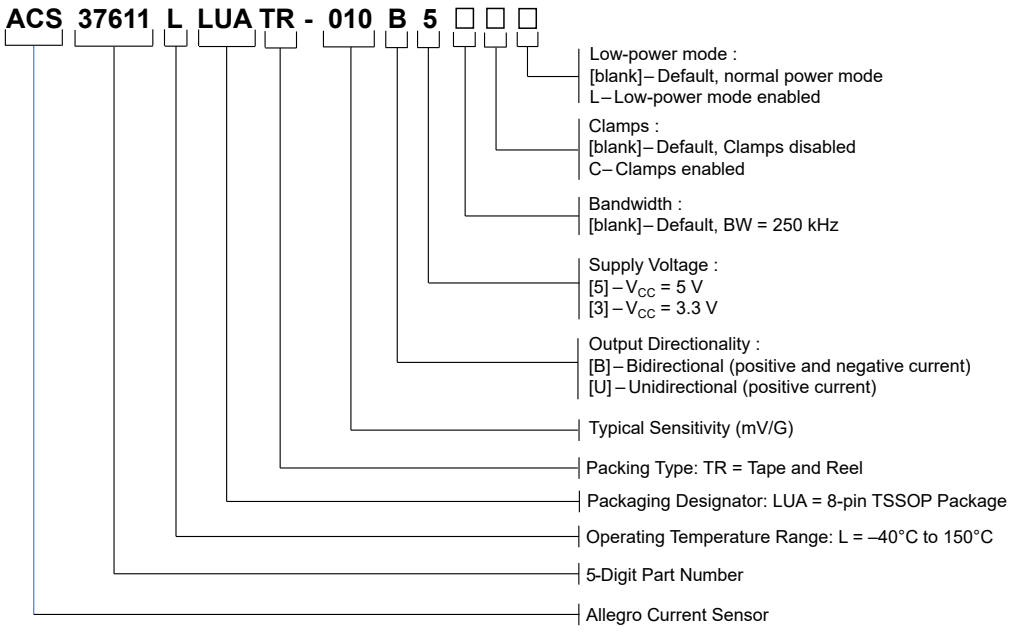
for safety-critical applications. The accuracy and flexibility of this device is enhanced by user programmability, performed via the output pin or through the dedicated programming pin, which allows the device to be optimized in the application and cancels errors caused by mechanical assembly tolerances on the PCB. Device specifications apply across an extended ambient temperature range: –40°C to 150°C.

The ACS37611 is suitable for space-constrained applications because of its low-profile eight-pin surface-mount thin-shrink small-outline package (TSSOP) package (Allegro part number suffix -LU) that is lead (Pb) free, with 100% matte tin leadframe plating. The sensor can be mounted in a horizontal or vertical orientation relative to the busbar, providing superior flexibility in mechanical assemblies.

SELECTION GUIDE

Part Number	Nominal Supply Voltage (V)	Differential Magnetic Input Range, (G)	Sensitivity Sens (Typ.) (mV/G) [1]	Sensitivity Trim Range (mV/G) [1]	T_A (°C)	Packing
ACS37611LLUATR-005B5	5	±400	5	3.5 to 6.5	–40 to 150	4000 pieces per 13-inch reel
ACS37611LLUATR-010B5	5	±200	10	7 to 13	–40 to 150	4000 pieces per 13-inch reel

[1] Measured at nominal supply voltage. Contact Allegro for other sensitivity options.



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	For a maximum duration of 1 minute	7.5	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Output Voltage	V_{OUT}		6.5	V
Reverse Output Voltage	V_{ROUT}		–0.5	V
Fault Voltage	V_F		6.5	V
Reverse Fault Output Voltage	V_{FR}		–0.5	V
Output Source Current	$I_{OUT(Source)}$	VOUT to GND	25	mA
Output Sink Current	$I_{OUT(Sink)}$	Maximum survivable sink or source current on the output	10	mA
Nominal Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

THERMAL CHARACTERISTICS: May require derating at maximum conditions; see application information

Characteristic	Symbol	Test Conditions	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	TSSOP-8 on 4-layer PCB based on JEDEC standard	145	°C/W

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TYPICAL APPLICATION CIRCUITS

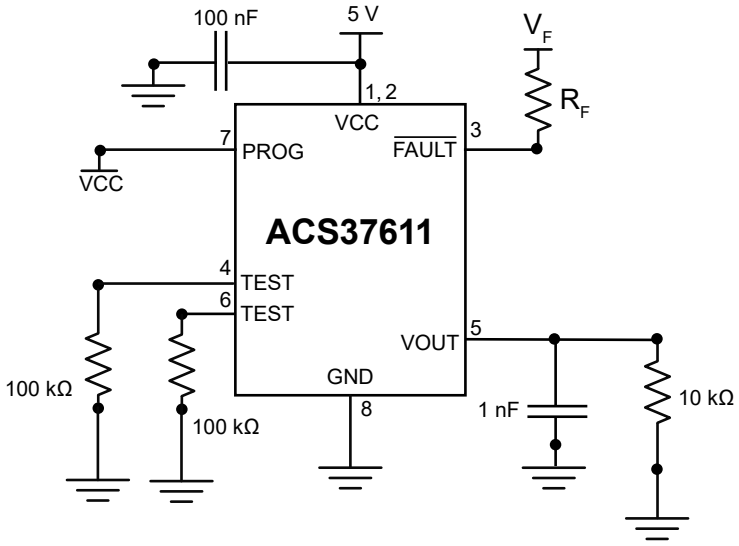
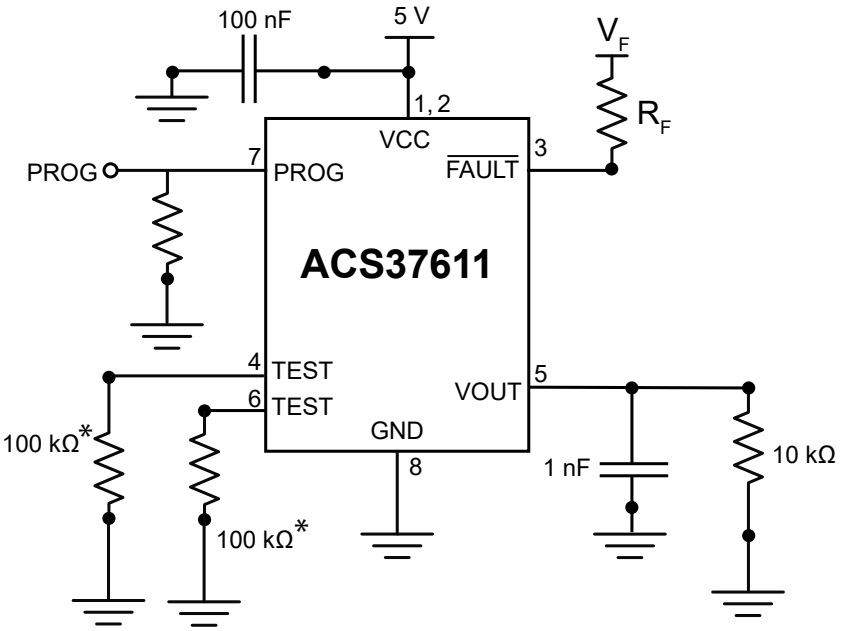


Figure 3: Typical Application Circuit (Programming Pin Not Used)



**For optimal broken ground and EMC performance*

Figure 4: Typical Application Circuit (Programming Pin Used)

The ACS37611 outputs an analog signal, V_{OUT}, that varies linearly with the bidirectional AC or DC field sensed, within the range specified. C_L is for optimal noise management, with values that depend on the application. R_L is an optional pulldown to GND or pullup to VCC for broken-wire detection. For broken-GND function, it is recommended to tie PROG pin to VCC when not used. R_F is an optional pull-up resistor to V_F, to be used when disabling the device internal pull-up in memory.

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PINOUT DIAGRAM AND PINOUT LIST

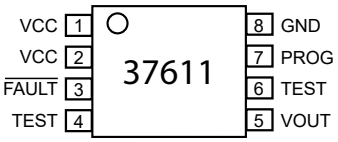

Figure 5: Pinout Diagram

Pinout List

Number	Name	Description
1,2	VCC	Input power supply; also used for programming
3	$\overline{\text{FAULT}}$	Fault output; overcurrent, overtemperature
4,6	TEST	Used for factory calibration, tie to ground in application for best EMC performance
5	VOUT	Analog output signal; also used for programming
7	PROG	Bidirectional programming pin
8	GND	Ground pin

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FUNCTIONAL BLOCK DIAGRAM

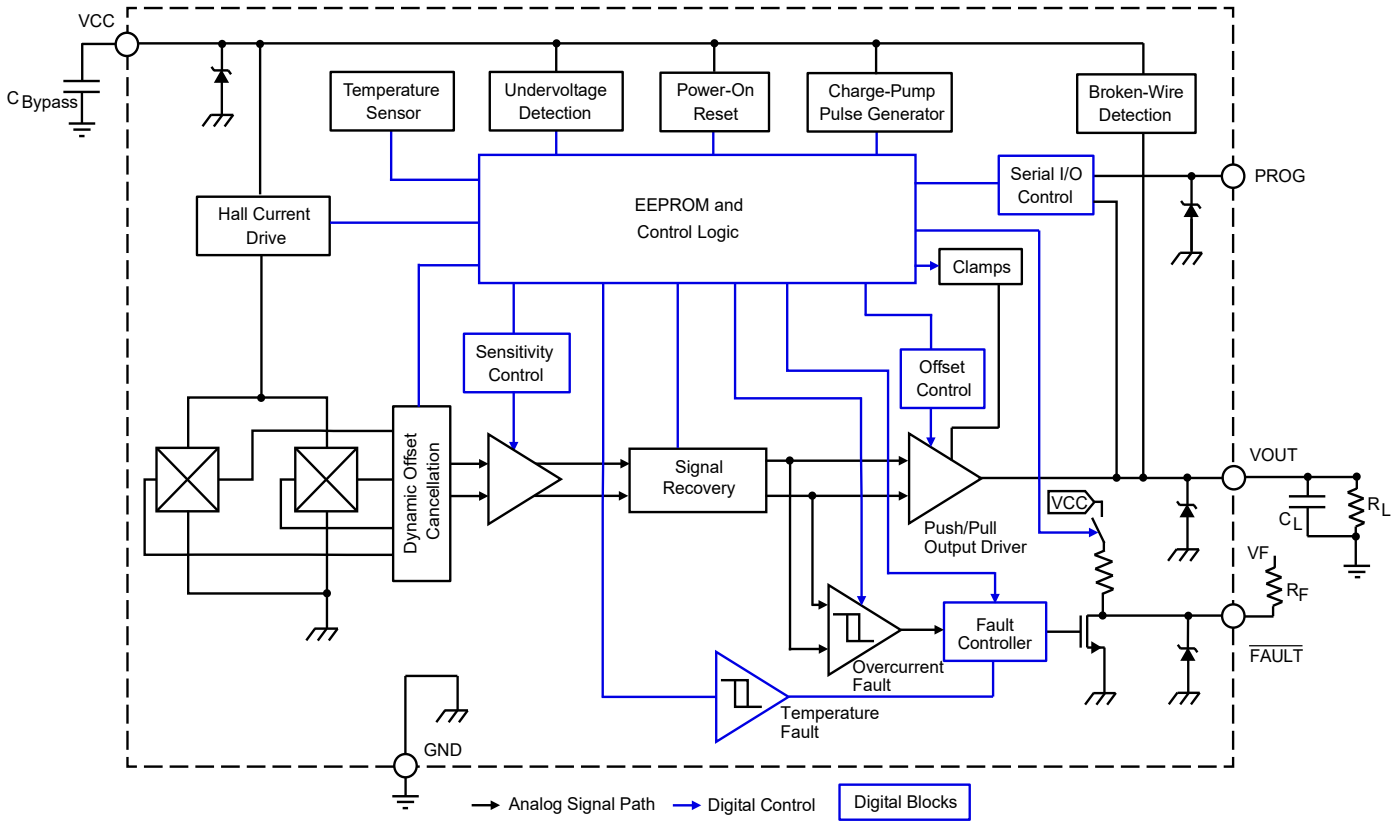

Figure 6: Functional Block Diagram

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COMMON OPERATING CHARACTERISTICS: Valid through full range of T_A and V_{CC}, C_{BYPASS} = 100 nF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage	V_{CC}	5 V nominal supply voltage	4.5	5	5.5	V
Supply Current	I_{CC}	5 V nominal supply voltage; $V_{CC}(min) \le V_{CC} \le V_{CC}(max)$, no load on output	–	16.5	21	mA
		5 V nominal supply voltage; low-power mode, no load on output	–	13.5	18	mA
Power-On Time	t_{PO}	T_A = 25°C, C_L (of test probe) = 10 pF, C_{BYPASS} = open	–	70	–	µs
Temperature Compensation Power-On Time	t_{TC}	Time after power-on time (t_{PO}) required to obtain valid temperature-compensated output; T_A = 150°C, C_{BYPASS} = open, C_L = 1 nF	–	45	–	µs
Fault Power-On Time	$t_{PO(FAULT)}$	Time from when $V_{CC} > V_{UVLOD}$ to when OCF reacts to overcurrent event	–	270	–	µs
Overvoltage Detection Threshold	V_{OVDE}	T_A = 25°C, V_{CC} rising and device function disabled	6.25	6.9	7.3	V
	V_{OVDD}	T_A = 25°C, V_{CC} falling and device function enabled	5.65	6	6.5	V
	V_{OVHYS}	T_A = 25°C	–	450	–	mV
OVD Enable/Disable Delay Time	t_{OVDE}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	60	–	µs
	t_{OVDD}	T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	3	–	µs
Undervoltage Lockout (UVLO) Threshold	V_{UVLOD}	V_{CC} rising	3	4.1	4.4	V
	V_{UVLOE}	V_{CC} falling	3.45	3.75	–	V
Undervoltage Lockout (UVLO) Hysteresis	$V_{UVLO(HYS)}$		–	450	–	mV
UVD Enable/Disable Delay Time	t_{UVLOE}	Time measured from falling $V_{CC} < V_{UVLOE}$ to UVLO enabled; T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	65	–	µs
	t_{UVLOD}	Time measured from rising $V_{CC} > V_{UVLOD}$ to UVLO disabled; T_A = 25°C, C_{BYPASS} = open, C_L = 1 nF	–	8	–	µs
Power-On Reset Voltage	V_{PORH}	V_{CC} rising	2.7	2.9	3	V
	V_{PORL}	V_{CC} falling	2.5	2.7	2.9	V
Power-On Reset Hysteresis	$V_{HYS(POR)}$		50	150	–	mV
Power-On Reset Release Time	t_{PORR}	Time V_{CC} must be held above V_{PORH} to start counting for t_{UVLOD} after $V_{CC} > V_{UVLOD}$ and transition from high impedance to regular operation; T_A = 25°C, V_{CC} rising	–	65	–	µs
Internal Bandwidth [1]	BW_i	–3 dB, C_L = 1 nF, T_A = 25°C	–	250	–	kHz
Rise Time [1]	t_r	T_A = 25°C, C_L= 1 nF, 1 V step on output, BW_i = 250 kHz	–	2.4	–	µs

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COMMON OPERATING CHARACTERISTICS (continued): Valid through full range of T_A and V_{CC}, C_{BYPASS} = 100 nF, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Propagation Delay [1]	t_{PD}	T_A = 25°C, C_L = 1 nF, 1 V step on output, BW_i = 250 kHz	–	1.1	–	µs
Response Time [1]	$t_{RESPONSE}$	T_A = 25°C, C_L = 1 nF, 1 V step on output, BW_i = 250 kHz	–	1.6	–	µs
DC Output Impedance	R_{OUT}		–	< 1	–	Ω
Output Load Resistance	R_L	VOUT to GND	4.7	10	–	kΩ
Output Load Capacitance	C_L	VOUT to GND	–	1	10	nF
Delay to Clamp	t_{CLP}	T_A = 25°C; C_L = 1 nF; Step from 75% output range to 150%	–	5	–	µs
Output Full-Scale Range	$V_{OUT(FSR)}$	Full-scale output, bidirectional	–	±2	–	V
Output Voltage Clamp [2]	$V_{CLP(HIGH)}$	V_{CC} = 5 V, $R_{L(PULLDOWN)}$ = 10 kΩ to GND	4.48	–	4.75	V
	$V_{CLP(LOW)}$	V_{CC} = 5 V, $R_{L(PULLUP)}$ = 10 kΩ to VCC	0.25	–	0.5	V
Output Saturation Voltage	$V_{SAT(HIGH)}$	$R_{L(PULLDOWN)}$ = 10 kΩ to GND	V_{CC} – 0.2	–	–	V
	$V_{SAT(LOW)}$	$R_{L(PULLUP)}$ = 10 kΩ to VCC	–	–	200	mV
Broken Wire Voltage	$V_{BRK(High)}$	$R_{L(PULLUP)}$ = 10 kΩ to VCC; refer to figure 5	V_{CC} – 0.1	V_{CC}	V_{CC}	V
	$V_{BRK(Low)}$	$R_{L(PULLDOWN)}$ = 10 kΩ to GND; refer to figure 5	0	0	100	mV
ERROR COMPONENTS						
Clamp Ratiometry Error	Rat_{ERRCLP}	V_{CC} = ±3% variation of nominal supply voltage	–	< ±0.5	–	%
Common Mode Field Rejection Ratio	CMFRR	Measured at 100 G uniform magnetic field	–	40	–	dB
Noise Density	B_{ND}	Normal power mode, 5 V, T_A = 25°C, C_L = 1 nF	–	0.9	–	mG /√(Hz)
		Low-power mode, 5 V, T_A = 25°C, C_L = 1 nF	–	1.2	–	mG /√(Hz)

[1] Timing specified does not include potential effect of skin effect on conductor; value depends on busbar/PCB design.
[2] Clamps are disabled by default.

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FAULT CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Positive Field Fault Switch Point Range [1]	$OCFP_{THRESH}$	Programmable using OCF positive threshold bits. In percent of full-scale positive output (2.5 to 4.5 V) on bidirectional variant.	50	–	200	% FS(+)
		Programmable using OCF positive threshold bits. In percent of full-scale output (0.5 to 4.5 V) on unidirectional variant.	50	–	200	% FS
Negative Field Fault Switch Point Range [1]	$OCFN_{THRESH}$	Programmable using OCF negative threshold bits. In percent of full-scale negative output (2 V typical, 2.5 to 0.5 V) on bidirectional variant	50	–	200	% FS(-)
Overcurrent Fault Switch Point Step Size	OCF_{STEP}	Overcurrent fault threshold programming step size	–	1.6	–	% FS
Overcurrent Fault Accuracy	OCF_{ACC}	Overcurrent fault threshold accuracy through full range of T_A	–10	±2	+10	% FS
Overcurrent Fault Response Time	t_{OCF}	$R_{F(PULLUP)}$ = 10 kΩ from FAULT to V_F, VOUT step from $V_{OUT(Q)}$ to V_{OUT} = ($V_{OUT(Q)}$ + $OCF_{PTHRESH}$ [V]); BW_i = 250 kHz, OCF qualifier = 0	–	2.5	–	µs
Overtemperature Fault Sampling Rate	OTF_S	Rate at which the temperature is sampled	–	8	–	ms
Fault Clear Time	$t_{C(F)}$	Time to release FAULT pin (return to V_F) when fault condition is no longer present. R_F = 10 kΩ, external 100 pF from FAULT to VCC	–	8	–	µs
		Time to release FAULT pin (return to V_{CC}) when fault condition is no longer present. Internal fault pull-up enabled	–	15	–	µs
Fault Jitter	OCF_{JITT}	T_A = 25°C, 1 sigma	–	100	–	ns
Overcurrent Fault Hysteresis Level Range [1]	OCF_{HYST}	Hysteresis in percent of trip level, T_A = 25°C, OCF_HYST = 0	–	11	–	%
		Hysteresis in percent of trip level, T_A = 25°C, OCF_HYST = 1	–	22	–	%
		Hysteresis in percent of trip level, T_A = 25°C, OCF_HYST = 2	–	45	–	%
		Hysteresis in percent of trip level, T_A = 25°C, OCF_HYST = 3	–	75	–	%
Overtemperature Fault Accuracy [1]	OTF_{ACC}		–10	±3	+10	°C
Overtemperature Fault Threshold Range [1]	OTF_{THRESH}		80	160	165	°C
Overtemperature Fault Step size			–	7	–	°C
Overtemperature Fault Hysteresis [1]	OTF_{HYST}	Overtemperature fault fixed hysteresis value	10	15	20	°C
FAULT Pin Low Output Voltage	V_{FAULT}	$R_{F(PULLUP)}$ = 4.7 kΩ from FAULT to VCC	–	–	0.4	V
FAULT Pin Leakage Current	I_{FLeak}	$R_{F(PULLUP)}$ = 4.7 kΩ from FAULT to VCC	–	–	1.3	µA
External Pull-Up Supply Voltage [1]	$V_{F(PULLUP)}$		1.65	V_{CC}	V_{CC}	V
External FAULT Pull-Up Resistor [1]	$R_{F(PULLUP)}$		4.7	–	500	kΩ
External FAULT Capacitance [1]	C_F		–	–	10	nF
Internal FAULT Pull-Up Resistor	$R_{IF(PULLUP)}$	Internal pull-up to V_{CC}; set FaultR_dis bit to 1 in EEPROM to disable.	–	10	–	kΩ

[1] Limits guaranteed by design and characterization data, not tested in production.

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-05B5 PERFORMANCE CHARACTERISTICS: Valid over full range of T_A and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	–400	–	400	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; T_A = 25°C	4.94	5	5.06	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; T_A = 25°C	2.495	2.5	2.505	V
Noise [1]	V_N	T_A = 25°C, C_L = 1 nF, BW_i = 250 kHz, initial sensitivity	–	2.5	–	mV_{RMS}
Nonlinearity [2]	E_{LIN}	Tested up to full-scale output	–0.55	±0.15	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2],[3]	$Rat_{ErrSens}$	V_{CC} = ±3% variation of nominal supply voltage	–0.75	±0.25	0.75	%
Sensitivity Drift Over Temperature [4]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C; ±20% sensitivity change	–1.2	±0.7	1.2	%
		T_A = –40°C to 25°C; ±20% sensitivity change	–1.2	±0.7	1.2	%
QUIESCENT VOLTAGE OUTPUT ERROR						
QVO Ratiometry Error [2],[3]	$V_{RatErrQVO}$	V_{CC} = ±3% variation of nominal supply voltage	–5	±2	5	mV
Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	T_A = 25°C to 150°C; ±20% sensitivity change	–5	±3	5	mV
		T_A = –40°C to 25°C; ±20% sensitivity change	–5	±3	5	mV
LIFETIME DRIFT CHARACTERISTICS [5]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	–	±2	–	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	–	±0.3	–	%

[1] Noise scales with sensitivity.
[2] Guaranteed by characterization.
[3] For lower V_{CC} variations than test conditions, ratiometry error scales linearly with V_{CC}; e.g., ±1.5% variations on V_{CC} instead of ±3% leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.
[4] Adjustments made to fine sensitivity may effect performance.
[5] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case mean drift observed during AEC-Q100 qualification from any of the –40°C, 25°C, or 150°C temperatures.

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Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
NOMINAL PERFORMANCE						
Differential Magnetic Range	B_{DIFF}	Corresponding full-scale magnetic range based on typical sensitivity	–200	–	200	G
Initial Factory-Programmed Sensitivity	Sens	Factory-programmed sensitivity; T_A = 25°C	9.88	10	10.12	mV/G
Initial Quiescent Output Voltage	$V_{OUT(Q)}$	Factory-programmed quiescent output voltage; T_A = 25°C	2.495	2.5	2.505	V
Noise [1]	V_N	T_A = 25°C, C_L = 1 nF, BW_i = 250 kHz, initial sensitivity	–	5	–	mV_{RMS}
Nonlinearity [2]	E_{LIN}	Tested up to full-scale output	–0.55	±0.15	0.55	%
SENSITIVITY ERROR						
Sens Ratiometry Error [2],[3]	$Rat_{ErrSens}$	V_{CC} = ±3% variation of nominal supply voltage	–0.75	±0.25	0.75	%
Sensitivity Drift Over Temperature [4]	$\Delta Sens_{TC}$	T_A = 25°C to 150°C; ±20% sensitivity change	–1.2	±0.7	1.2	%
		T_A = –40°C to 25°C; ±20% sensitivity change	–1.2	±0.7	1.2	%
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Quiescent Voltage Output Temperature Error	$V_{OUT(Q)TC}$	T_A = 25°C to 150°C; ±20% sensitivity change	–5	±3	5	mV
		T_A = –40°C to 25°C; ±20% sensitivity change	–5	±3	5	mV
LIFETIME DRIFT CHARACTERISTICS [5]						
QVO Lifetime Drift	$V_{OUT(Q)LIFE}$	Initial sensitivity	–	±2	–	mV
Sens Lifetime Drift	$Sens_{LIFE}$	Initial sensitivity	–	±0.3	–	%

[1] Noise scales with sensitivity.
[2] Guaranteed by characterization.
[3] For lower V_{CC} variations than test conditions, ratiometry error scales linearly with V_{CC}; e.g., ±1.5% variations on V_{CC} instead of ±3% leads to $Rat_{ErrSens}$ and $V_{RatErrQVO}$ to be divided by 2.
[4] Adjustments made to fine sensitivity may effect performance.
[5] Lifetime drift characteristics are based on the AEC-Q100 qualification results from zero-hour reads. Typical values are the worst-case mean drift observed during AEC-Q100 qualification from any of the –40°C, 25°C, or 150°C temperatures.

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FUNCTIONAL DESCRIPTION

Principle of Operation

When AC or DC current flows through a PCB copper trace or a busbar, as shown in Figure 7, the ACS37611 device senses the magnetic-field difference induced between its two Hall elements, HL and HR, represented by the field components B_L and B_R. The device output is proportional to the differential field sensed, B_{diff}, which is proportional to the applied current. The relationship between applied current and generated field is described as:

$$B_{diff} = CF \times I,$$

where B_{diff} is the differential field (HL – HR), CF is the differential coupling factor (G/A), and I is the current through the busbar/PCB trace. As can be observed from this equation, the differential coupling factor (CF) is the linear relationship between the differential field sensed and the current flowing in the conductor. Different busbar shapes can be used to best answer application requirements; for more details, refer to the Typical Application—PCB Sensing section.

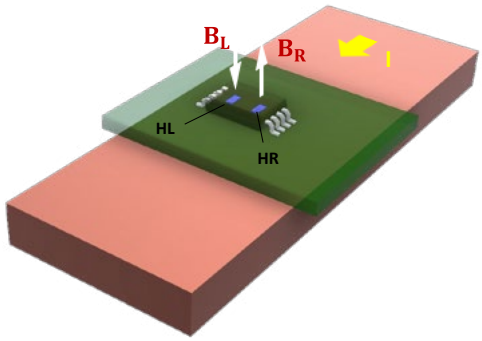

Figure 7: Current-Sensing Principle

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Device Diagnostics

The ACS37611 device offers multiple built-in diagnostics which effects and programmability are described in Table 1.

Table 1: Device Diagnostics Table

Diagnostic	Effect on V_{OUT}	Effect on FAULT	Note
Overvoltage Detection	If V_{CC} is higher than V_{OVDE} for more than t_{OVDE} (64 µs typ.), V_{OUT} goes to the high-impedance state.	FAULT remains in the high-impedance state (or goes to high-impedance in case of FAULT pin asserted), pulled-up to $V_{F(PULLUP)}$	NOTE 1: When V_{OUT} goes to the high-impedance state, the voltage on V_{OUT} is pulled down to GND or pulled up to V_{CC}, depending on application wiring. If the COM_LOCK bit is set, the OVD feature is disabled.
Undervoltage Detection	If V_{CC} drops below V_{UVLOE} for more than t_{UVLOE} (64 µs typ.), V_{OUT} is pulled to GND. If V_{CC} drops further below V_{POR}, V_{OUT} goes to the high-impedance state.	FAULT remains in the high-impedance state (or goes to high-impedance in case of FAULT pin asserted), pulled-up to $V_{F(PULLUP)}$.	See NOTE 1.
Broken Wire	V_{OUT} goes to the high-impedance state.	FAULT remains in the high-impedance state (or goes to high-impedance in case of FAULT pin asserted), pulled-up to $V_{F(PULLUP)}$.	See NOTE 1.
Overcurrent	No effect.	FAULT pin is pulled to GND.	Overcurrent threshold is programmable and can be enabled/disabled in EEPROM.
Overtemperature	No effect.	FAULT pin is pulled to GND.	Overtemperature threshold is programmable and can be enabled/disabled in EEPROM.
Clamps	V_{OUT} can range from $V_{CLP(Low)}$ to $V_{CLP(High)}$.	No effect.	Clamps can be enabled/disabled in EEPROM.
EEPROM Error Checking and Correction	If an uncorrectable error occurs in EEPROM, V_{OUT} goes to the high-impedance state.	FAULT goes to the high-impedance state.	See NOTE 1.

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Broken-Wire Detection

If the GND pin is disconnected, node A becoming open (Figure 9), the VOUT pin and FAULT pin goes to a high-impedance state. If a load resistor $RL_{(PULLUP)}$ is connected to VCC, the output voltage goes to $VBRK_{(HIGH)}$. If a load resistor $RL_{(PULLDOWN)}$ is connected to GND, the output voltage goes to $VBRK_{(LOW)}$.

If the VCC pin is disconnected, node B becoming open (Figure 9), the VOUT pin and FAULT pin goes to a high-impedance state. If a load resistor $RL_{(PULLDOWN)}$ is connected to GND, the output voltage goes to $VBRK_{(LOW)}$.

Detection for broken VCC can only be guaranteed when a pull-down resistor is used.

Following a broken-wire event, the device does not respond to any applied magnetic field. If a load resistor $RF_{(PULLUP)}$ is connected to the FAULT pin, the fault voltage goes to the $VF_{(PULLUP)}$ voltage.

If the disconnected wire is reconnected, the device resumes typical operation.

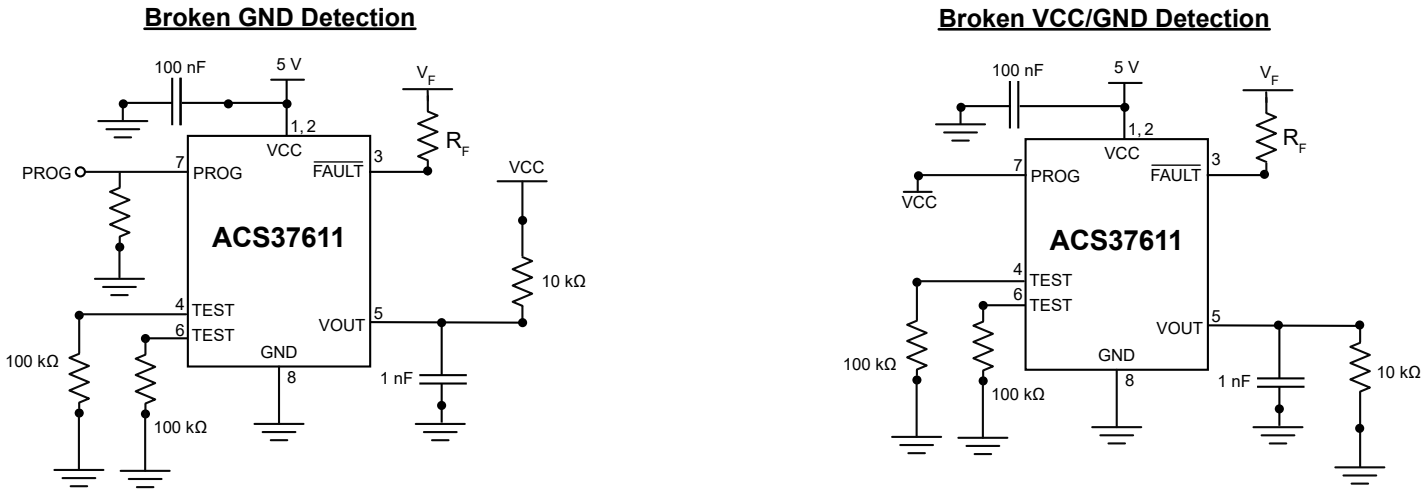

Figure 8: Connection for Detecting Broken Ground Wire

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DEVICE PROGRAMMING

- The serial interface uses Manchester protocol to communicate.
- Device programming can be achieved with bidirectional communication on VOUT or on the dedicated PROG pin.
- The device has an internal charge pump to generate the EEPROM pulses.
- When not used, the PROG pin can be left unconnected or tied to GND or VCC.

Serial Communication

The serial interface allows an external controller to read from and write to registers, including EEPROM, in the device using a point-to-point command/acknowledge protocol. The device does not initiate communication; it only responds to commands from the external controller. Each transaction consists of a command from the controller. If the command is a write, there is no acknowledgement from the device. If the command is a read, the device responds by transmitting the requested data. Two modes are available for device communication.

Mode 1, Programming on VOUT pin (see Figure 9):
To enable bidirectional programming on VOUT, voltage is raised on V_{CC} (V_{OVDE}) for at least t_{OVDE}, then the access code is transmitted on VOUT. If the COM_LOCK bit is set (value = 1), bidirectional programming on VOUT is disabled. If the COM_LOCK bit is not set (value = 0), there is no timeout limit to send the access code as long as V_{CC} stays above V_{OVDE} for at least t_{OVDE}. To ensure a reset of the Manchester state machine, the start of any Manchester command should begin by holding the output low for t_{BIT}. If an incorrect access code is sent, VOUT remains in the typical analog mode (responds to magnetic stimulus) and the device remains locked for communication on VOUT until a power reset occurs.

To ensure safe writing to EEPROM when writing to nonvolatile memory (EEPROM), V_{CC} must not exceed 5 V. To achieve this, two methods can be used:

Method 1 (to write to EEPROM in Mode 1):

Locking VOUT into communication mode such that VCC can be returned to typical supply voltage (5 V):

1. Set V_{CC} to V_{OVDE} (OVD)
2. Send access code + COMM_EN
3. Set V_{CC} back to typical level (5 V)
4. Send EEPROM write commands
5. Power-cycle the device to re-enable analog output on VOUT

Method 2 (to write to EEPROM in Mode 1):

Reducing VCC back to typical supply voltage (5 V) after sending the EEPROM write sequence:

1. Set V_{CC} to V_{OVDE} (OVD)
2. Send access code
3. Send EEPROM write commands
4. Set V_{CC} to typical level (5 V)
5. Wait 20 ms for EEPROM write

With method 2, the PROG pin must not be connected to GND (can be left floating or connect to VCC).

For more details, refer to the Write Access Code (Controller to Device) section and the figures in the Manchester Protocol section. When not used, it is recommended to tie the PROG pin to VCC (for the broken GND feature).

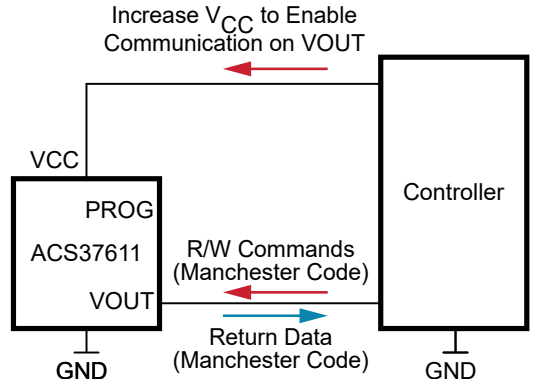

Figure 9: Programming Connection—Mode 1

Mode 2, Programming on PROG Pin (see Figure 10):
V_{CC} remains 5 V (below V_{OVDE}), and bidirectional programming is achieved on PROG pin by sending an access code (independently of COM_LOCK value). No pull-up is required on PROG pin.

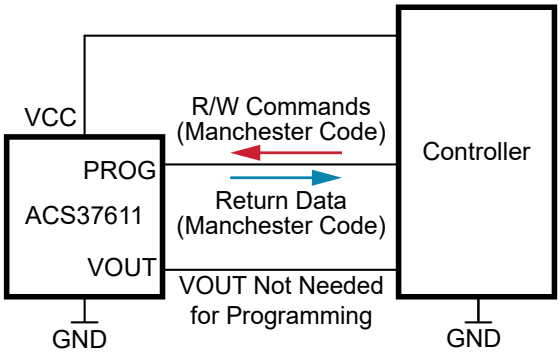

Figure 10: Programming Connections—Mode 2

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Manchester Protocol

The serial interface uses a Manchester-encoding-based protocol per G.E. Thomas (0 = rising edge, 1 = falling edge), with address and data transmitted MSB first. Four commands are recognized by the device: write access code, write to volatile memory, write to nonvolatile memory (EEPROM), and read. In response to a read command, one frame type, read acknowledge, is sent by the device.

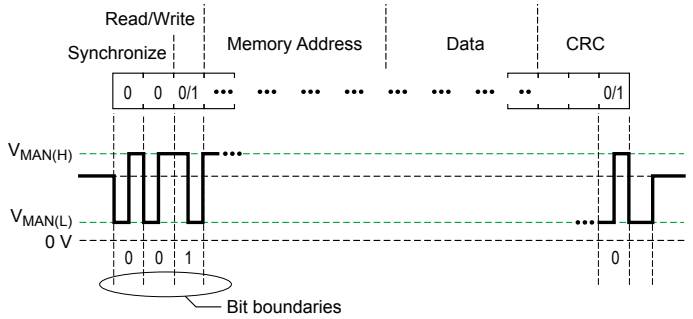

Figure 11: General Format for Serial Interface Commands

Read (Controller to Device)

The fields for the read command are:

- Sync (2 bits, both with the value 0)
- Read/Write (1 bit; for read, this value must be 1)
- CRC (3 bits)

The sequence for a read command is shown in Figure 12.

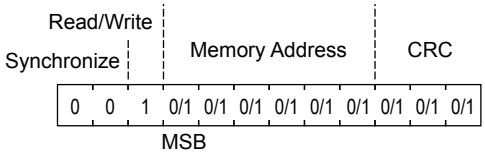

Figure 12: Read Sequence

Read Acknowledge (Device to Controller)

The fields for the data return frame are:

- Sync (2 bits, both with the value 0)
- Data (32 bits):
  - □ [31:28] Not Relevant
  - □ [27:26] ECC Pass/Fail
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a read acknowledge is shown in Figure 13. For instructions about how to detect read/write synchronize memory address data (32 bits) and ECC failure, refer to the Detecting ECC Error section.

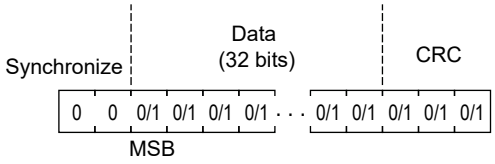

Figure 13: Read Acknowledge Sequence

Write (Controller to Device)

The fields for the write command are:

- Sync (2 bits, both with the value 0)
- Read/Write (1 bit; for write, this value must be 0)
- Address (6 bits)
- Data (32 bits):
  - □ [31:26] Not Relevant
  - □ [25:0] Data
- CRC (3 bits)

The sequence for a write command is shown in Figure 14. Bits [31:26] are not relevant because the device automatically generates 6 ECC bits based on the content of bits [25:0]. These ECC bits are stored in EEPROM at locations [31:26].

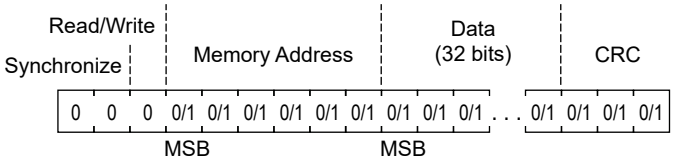

Figure 14: Write Sequence

Write Access Code (Controller to Device)

The fields for the access code command are:

- Sync (2 bits, both with the value 0)
- Read/Write (1 bit; for write, this value must be 0)
- Address (6 bits)
- Data (32 bits)
- CRC (3 bits)

The sequence for an access code command is shown in Figure 15.

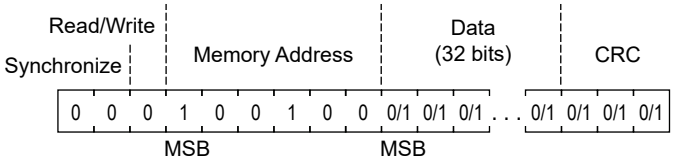

Figure 15: Write Access Code

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The controller must open the serial communication with the device by sending an access code. To enable communication on PROG pin, the access code can be sent on the PROG pin at any time. For VOUT communication, an OVD event must be sent followed by the access code on VOUT. The OVD event must be maintained during the first full transaction.

Register Address	Address(Hex)	Data(Hex)
Customer Access	0x31	0x2C413736
Customer Access + COM_ENABLE	0x31	0x2C413737

The LSB of the 32-bit customer access code is used to disable the output and leave the device in communication mode until a reset occurs. When the output is disabled, V_{CC} can be restored to a level inferior to V_{OVDE} without altering the Manchester communication and thus until a reset occurs.

Using the COM_LOCK bit

This bit prevents VOUT from changing state following an unwanted OVD event in the application. If the COM_LOCK bit is set, the OVD is disabled and the device can only be programmed using the PROG pin (communication Mode 2).

WRITE_LOCK bit

Lock bit after EEPROM has been programmed by the user. The Write_lock bit can be set to 1 and VCC power-cycled to permanently disable the ability to write any EEPROM register. Writing to the volatile register can still occur.

EEPROM Error Checking and Correction (ECC)

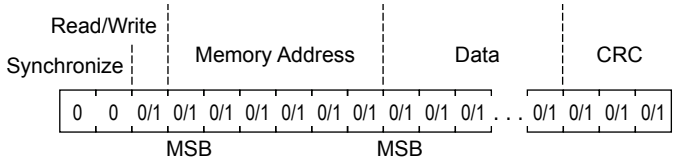
Hamming code methodology is implemented for EEPROM checking and correction. The device has ECC enabled after power-up. The device always returns 32 bits. The message received from the controller is analyzed by the device EEPROM driver, and ECC bits are added. The first 6 bits received from device to controller are dedicated to ECC.

The Manchester serial interface uses a 3-bit cyclic redundancy check (CRC) for data-bit error checking (synchronized bits are ignored during the check). The CRC algorithm is based on the polynomial $g(x) = x^3 + x + 1$ and is initialized to 111 when first powered up. Write commands written to the peripheral controller are checked against the embedded CRC field.

Detecting ECC Error

If an uncorrectable error has occurred, bits [29:28] are set to 10, the VOUT pin goes to a high-impedance state, and the device does not respond to the applied magnetic field.

Bits	Name	Description
31:28	–	No meaning
29:28	ECC	00 = No Error 01 = Error detected and message corrected 10 = Uncorrectable error 11 = No meaning
25:0	Data [25:0]	EEPROM data



Quantity of Bits	Name	Values	Description
2	Synchronization	00	Used to identify the beginning of a serial interface command
1	Read/Write	0	[As required] Write operation
		1	[As required] Read operation
6	Address	0/1	[Read/Write] Register address (volatile memory or EEPROM)
32	Data	0/1	26 data bits and 6 ECC bits. For a read command frame, the data consists of 32 bits: [31:28] not relevant, [27:26] ECC pass/fail, and [25:0] data, where bit 0 is the LSB. For a write command frame, the data consists of 32 bits: [31:26] not relevant and [25:0] data, where bit 0 is the LSB.
3	CRC	0/1	Bits to check the validity of the frame.

Figure 16: Command Frame General Format

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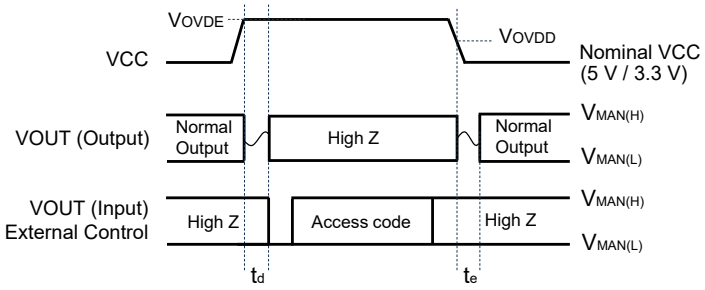

Figure 17: VOUT Programming (Mode 1)
Write Access Code

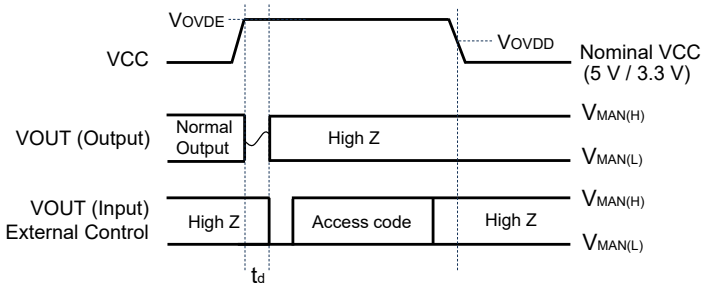

Figure 18: VOUT Programming (Mode 1)
Write Access Code + COMM_EN

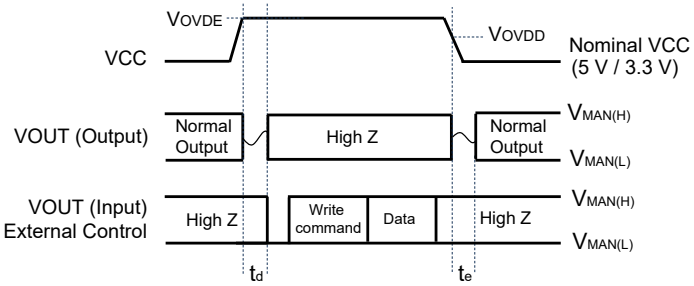

Figure 19: VOUT Programming (Mode 1)
Write Volatile Memory

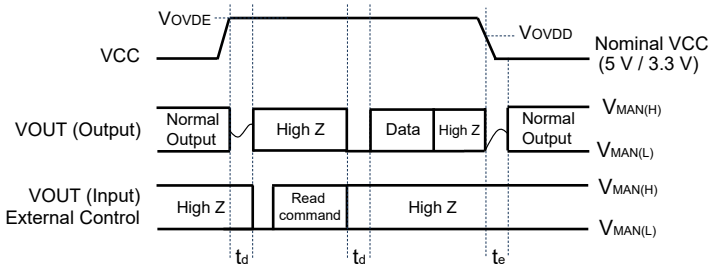

Figure 20: VOUT Programming (Mode 1)
Read Memory

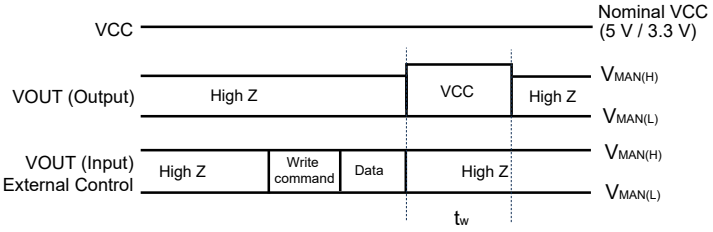

Figure 21: VOUT Programming (Mode 1)
Write to EEPROM (Method 1, COMM_EN = 1)

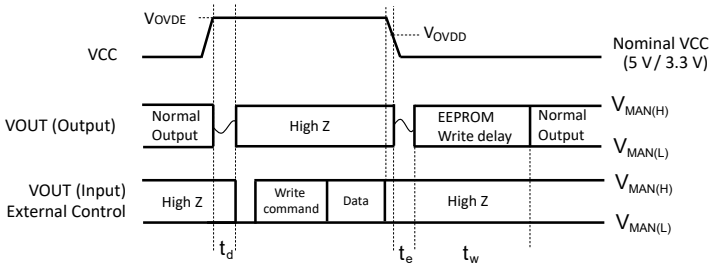

Figure 22: VOUT Programming (Mode 1)
Write to EEPROM (Method 2)

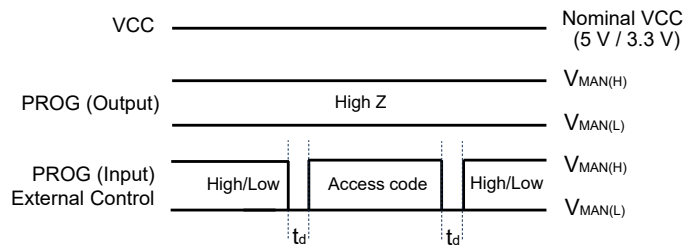

Figure 23: PROG Programming (Mode 2)
Write Access Code

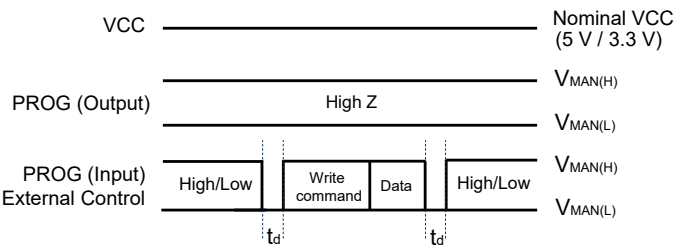

Figure 24: PROG Programming (Mode 2)
Write Volatile Memory

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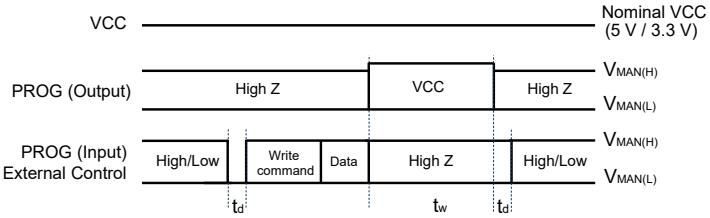

Figure 25: PROG Programming (Mode 2) Write to EEPROM

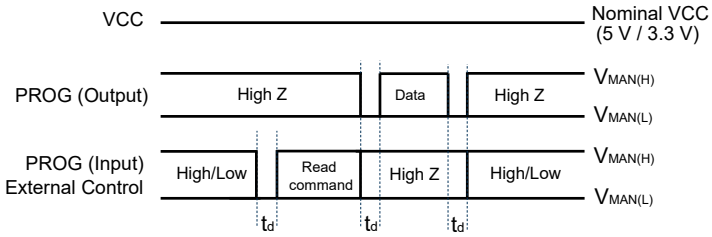

Figure 26: PROG Programming (Mode 2) Read Memory

Table 2: Programming Parameters, C_{BYPASS} = 0.1 µF, V_{CC} = 5 V

Characteristics	Symbol	Note	Min.	Typ.	Max. [1]	Unit
Program Time Delay	t_d	Delay between consecutive read/writes during same Manchester event	–	74	–	µs
Program Write Delay	t_w	Delay between EEPROM writes	–	25	35	ms
Manchester High Voltage	$V_{MAN(H)}$	Data pulses on VOUT/PROG pin, V_{CC} = 5 V	4	5	V_{CC}	V
Manchester Low Voltage	$V_{MAN(L)}$	Data pulses on VOUT/PROG pin, V_{CC} = 5 V	0	–	1	V
Bit Rate	t_{BITR}	Communication rate	1	30	133	kbps
Bit Time	t_{BIT}	Data bit pulse width	1000	33	7.5	µs
Output Enable Delay	t_e	External capacitance (CLX) on VOUT may increase the output enable delay	–	125	–	µs

[1] Limit guaranteed by design and characterization.

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EEPROM and Programming Parameters

EEPROM PROGRAMMABLE PARAMETERS: Valid through full range of T_A and V_{CC}, unless otherwise specified

Parameter	Symbol	Description	Min.	Default Value	Max.	Unit	Bit	Typ. Step Size
Overcurrent Positive Fault [1]	OCF_P_THRES	Programmable overcurrent/field fault positive	50	110	200	% FS	7	1.6 %
Overcurrent Negative Fault [1]	OCF_N_THRES	Programable overcurrent/field fault negative	50	110	200	% FS	7	1.6 %
Sensitivity Fine [2]	SENS_FINE	Sensitivity fine adjustment; signed 2's complement	7	10	13	mV/G	9	30 µV/G
QVO [2]	QVO	Quiescent output voltage adjustment ($V_{OUT(Q)}$); signed 2's complement V_{CC} = 5 V, bidirectional	2.4	2.5	2.6	V	9	1 mV
		Quiescent output voltage adjustment ($V_{OUT(Q)}$); signed 2's complement V_{CC} = 5 V, Unidirectional	0.4	0.5	0.6	V	9	1 mV
Fault Pull-Up Disconnect	FAULTR_DIS	Disconnect fault pull-up resistor	0	0	1	–	1	–
Polarity	POL	Output polarity	0	0	1	–	1	–
OCF Qualifier [1]	OCF_QUAL	Overcurrent fault qualifier delay, typical programmable values	0	0	12.7	µs	3	–
Fault Latch	FAULT_LATCH	Fault latch enable	0	0	1	–	1	–
OCF Hysteresis [1]	OCF_HYST	Overcurrent fault hysteresis, typical programmable values	11	11	75	%	2	–
OCF Disable	OCF_DIS	Overcurrent fault disable	0	0	1	–	1	–
OTF Threshold [1]	OTF_THRESH	Overtemperature fault threshold	80	155	165	°C	4	7
OTF Fault Disabled	OTF_DIS	Overtemperature fault disable	0	1	1	–	1	–
Communication Lock	COM_LOCK	Used to disable Manchester communication	0	0	1	–	1	–
Disabled Positive OCF Trip Point	OCF_P_DIS	Disable the positive overcurrent fault trip point	0	0	1	–	1	–
Disabled Negative OCF Trip Point	OCF_N_DIS	Disable the negative overcurrent fault trip point	0	0	1	–	1	–
Clamp Enable	CLAMP_EN	Enable clamps on the output	0	0	1	–	1	–
Customer Scratch	SCRATCH_C	Customer scratch pad	–	–	–	–	26	–

[1] Limits guaranteed by design and characterization data, not tested in production.
[2] Although device programming range may be larger, programming sensitivity beyond ±40% of change from initial value causes $V_{OUT(Q)TC}$ and $\Delta Sens_{TC}$ drift to deteriorate beyond the specified values.

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Lock Bits Mechanism (WRITE_LOCK/COM_LOCK)

The device has two lock bits to disable communication and EEPROM programming. The achieved behavior is summarized Table 3.

Table 3: Lock Bit Mechanism

WRITE_LOCK	COM_LOCK	EEPROM Write	EEPROM Read
0	0	Yes: PROG pin or VOUT with OVD	Yes: PROG pin or VOUT with OVD
0	1	Yes: PROG pin	Yes: PROG pin
1	0	No	Yes: PROG pin or VOUT with OVD
1	1	No	Yes: PROG pin

Programming Sensitivity (SENS_FINE) and Quiescent Voltage Output (QVO)

Sensitivity and $V_{OUT(Q)}$ can be adjusted by programming the SENS_FINE and QVO bits, as illustrated in Figure 27 and Figure 28. The SENS_FINE and QVO codes use a 2's complement encoding to either reduce or increase sensitivity and $V_{OUT(Q)}$. Neither program sensitivity nor $V_{OUT(Q)}$ should be programmed beyond the maximum or minimum programming ranges specified in the Common Operating Characteristics table. Exceeding the specified limits causes the sensitivity and $V_{OUT(Q)}$ drift over the temperature range (E_{Drift} and V_{OED}) to deteriorate beyond the specified values. Programming sensitivity might cause a small drift in $V_{OUT(Q)}$. As a result, it is recommended to program sensitivity first, then $V_{OUT(Q)}$.

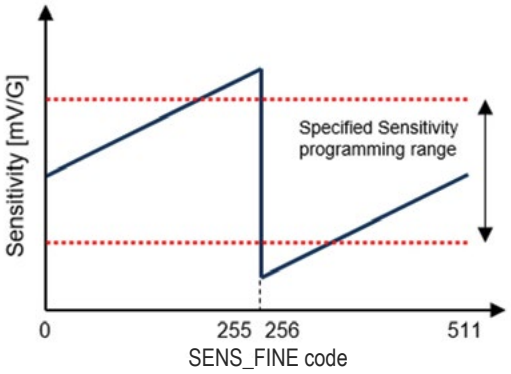

Figure 27: Sensitivity Trim Range

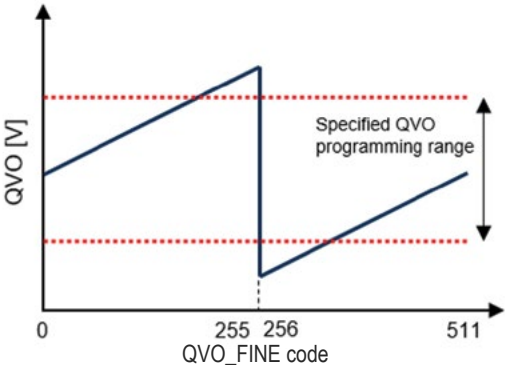

Figure 28: QVO Trim Range

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Polarity (POL)

Device output polarity is programmable to 1 (default) or 0; this allows output polarity to be reversed. Default polarity (POL bit set to 1) corresponds to an increasing output from 2.5 to 4.5 V typical (0.5 to 4.5 V on unidirectional versions) when positive current flows from pin 1 to pin 4 (or pin 8 to pin 5), as shown in Figure 29 and Figure 30. Note that changing device polarity from its initial programmed value can cause offset error $V_{OUT(Q)TC}$ to exceed specification limits.

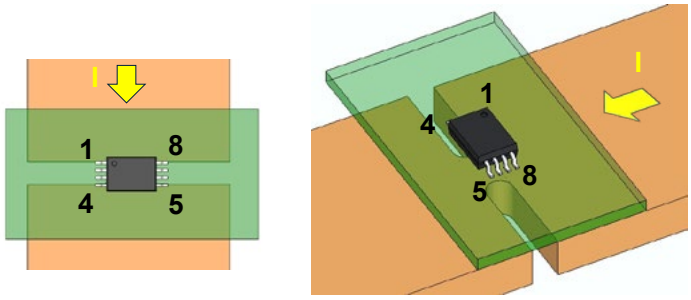

Figure 29: Polarity Definition in Planar Configuration

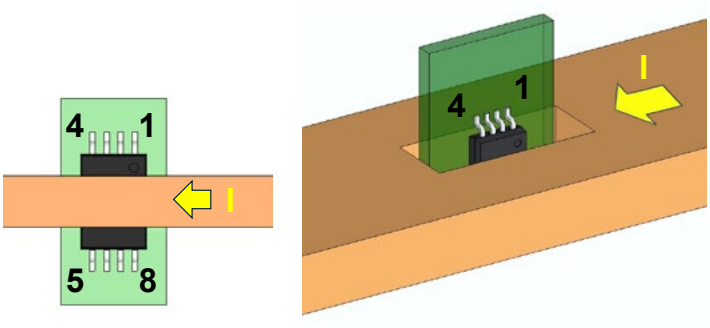

Figure 30: Polarity Definition in Vertical Configuration

Positive Overcurrent Fault Threshold (OCF_P_THRES)

This sets the threshold for the overcurrent fault (OCF) when current induces a positive output response on VOUT (increasing V_{OUT} value from 2.5 to 4.5 V for the 5 V bidirectional variant or 0.5 to 4.5 V for the 5 V unidirectional variant); see Figure 31. Threshold can be set independently of OCF_N_THRES and can be disabled in device memory by setting OCF_P_DIS to 1.

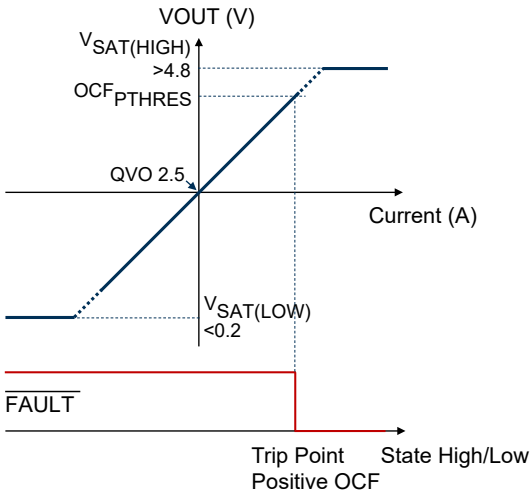

Figure 31: Positive OCF Threshold

Negative Overcurrent Fault Threshold (OCF_N_THRES)

The negative overcurrent fault threshold (OCF_N_THRES) bit sets the threshold for the OCF when current induces a negative output response on VOUT (decreasing V_{OUT} value from 2.5 to 0.5 V for the 5 V bidirectional variant); see Figure 32. Threshold can be set independently of OCF_P_THRES and can be disabled in device memory by setting the OCF_N_DIS bit to 1. The negative overcurrent fault threshold feature is only usable in the bidirectional variant.

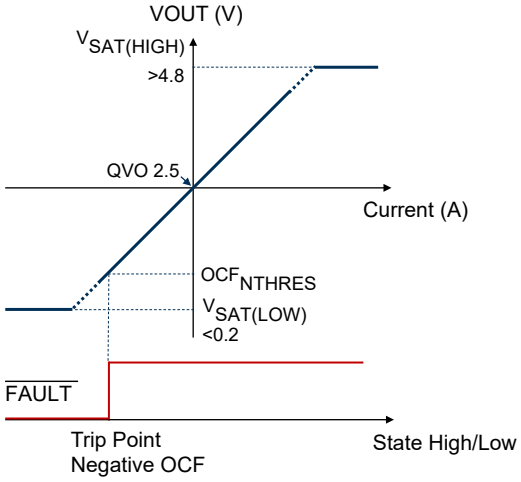

Figure 32: Negative OCF Threshold

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Fault Latch (FAULT_LATCH)

When the fault latch (FAULT_LATCH) bit is set to 1, the device needs to be power-cycled to release the fault condition (following an overcurrent or overtemperature event). By default, this is set to 0 (disabled).

When the FAULT_LATCH bit is disabled, the device relies on the programmed hysteresis value to release the fault.

Fault output behavior following an overcurrent condition is shown in Figure 33. When the FAULT_LATCH bit is set to 1, the fault remains activate (low state) until the device is power-cycled.

Fault output behavior following an overcurrent condition is shown in Figure 34. When the FAULT_LATCH bit set to 0, the fault is released once the current is reduced below the overcurrent threshold hysteresis level (OCF_{PTHRES} minus OCF_{HYST} for positive OCF threshold; OCF_{NTHRES} minus OCF_{HYST} for negative OCF threshold).

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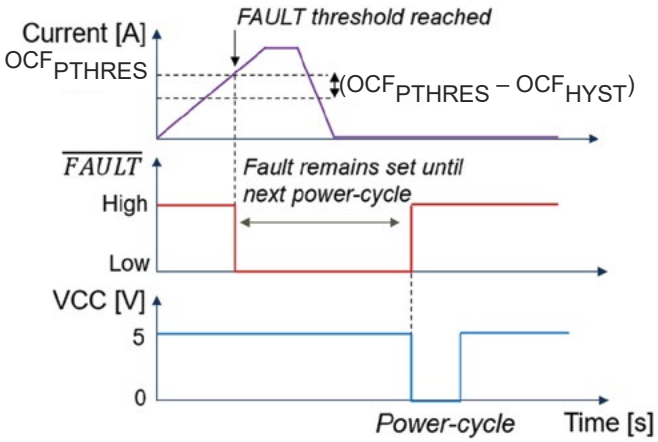

Figure 33: Fault Behavior with FAULT_LATCH = 1

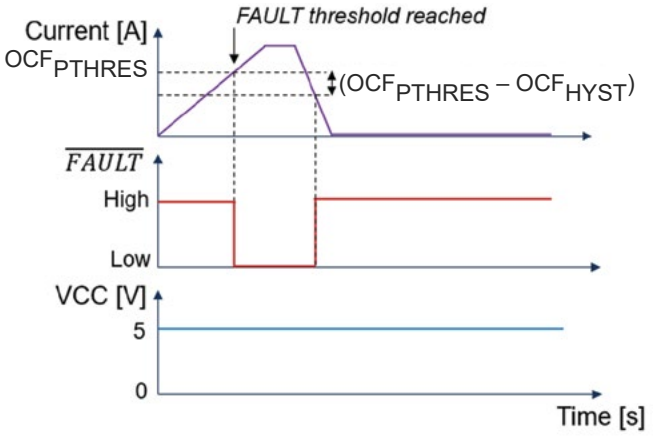

Figure 34: Fault Behavior with FAULT_LATCH = 0

Overcurrent Fault Qualifier (OCF_QUAL)

The overcurrent fault qualifier (OCF_QUAL) bit sets the amount of time the overcurrent condition must be detected before triggering the fault output. This acts as a filter on the fault condition to prevent incorrect triggering of the fault output in case of quick current spikes or ripples.

Overcurrent must exceed the specified threshold for the duration of the fault qualifier (OCF_{QUAL}) in order to be flagged, as shown in Figure 35 and Figure 36.

This delay does not apply to the condition for releasing the fault; once the hysteresis condition is fulfilled and $t_{C(F)}$ has elapsed, the fault is released.

The range of settings for the OCF_QUAL bit is described in Table 4.

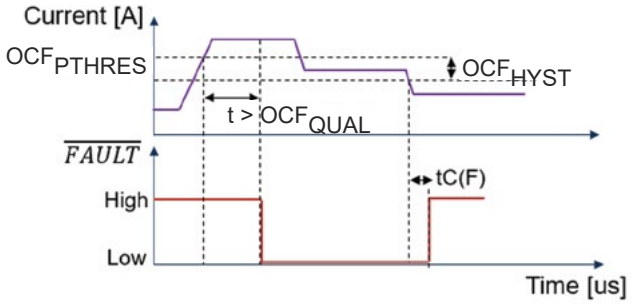

Figure 35: Fault not triggered if current exceeds OCF threshold for less than OCF_{QUAL}

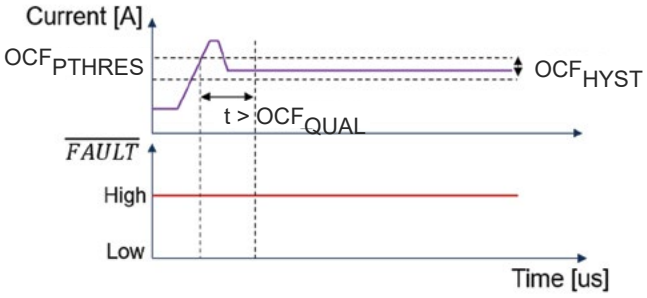

Figure 36: Fault triggered when current exceeds OCF threshold for more than OCF_{QUAL}; the fault is then released when current is below the hysteresis level

Table 4: Overcurrent Fault Qualifier

Setting	Typ. Delay to Fault	Units
0	2.3	µs
1	2.9	µs
2	5	µs
3	7.6	µs
4	10.1	µs
5	12.6	µs
6	15.3	µs
7	17.9	µs

Overcurrent Fault Hysteresis (OCF_HYST)

The overcurrent fault hysteresis (OCF_HYST) bit sets the hysteresis value applied to the OCF threshold such that, once triggered, the current must return below the hysteresis level to release the fault output. This feature prevents chattering of the FAULT pin due to noise.

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The hysteresis principle is shown in Figure 37; e.g., OCF_{PTHRES} = 110%, where OCF_{HYST} = 12.5% corresponds to a fault trip point at 110% (2.2 V output sweep if V_{CC} = 5 V) and a release point at 97.5% (1.95 V output sweep if V_{CC} = 5 V).

Programming values for the OCF_HYST bit are shown Table 5.

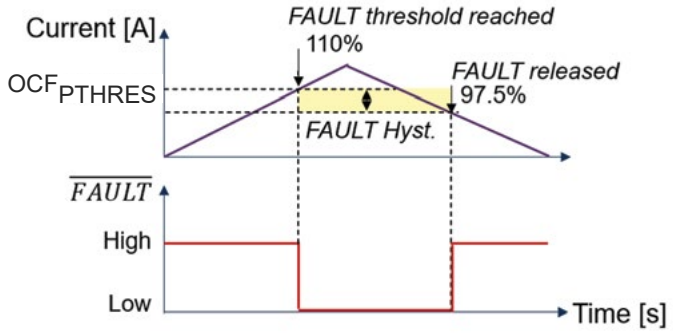

Figure 37: Hysteresis Effect on Fault

Table 5: Overcurrent Fault Hysteresis

Setting	Typ. Value [1]	Units
0	11	%
1	22	%
2	42	%
3	75	%

[1] Hysteresis value cannot be greater than the minimum OCF threshold specified minus 25%; e.g., if OCF_P is set at 50%, the maximum hysteresis value is 50 – 25 = 25%, such that OCF_HYST = 2 or 3 results in a maximum hysteresis value of 25%.

Temperature Output (TEMP_OUT)

This feature allows reading of the device temperature stored as a 12-bit digital value.

Digital temperature can be converted to ambient temperature in degree Celsius using:

$$Temp_{AMBIENT}\,[°C] = (Temp_{OUT} - 0.0734) - 125.5$$

NOTE: Due to device self-heating, the temperature reaches 90% of its steady state approximately 10 seconds after power-on.

Temperature accuracy is indicated in the Fault Characteristics table and is guaranteed by characterization only.

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MEMORY MAP

Register Name	Address	Parameter Name	Description	Access	Size	MSB	LSB
EEPROM: (EE_CUST0)	EEPROM: (0x09)	WRITE_LOCK	Lock the device	R/W	1	25	25
		COM_LOCK	Disable communication on VOUT/disable OVD	R/W	1	24	24
		SPARE	n/a	R/W	1	23	23
		OTF_DIS	Disable overtemperature fault	R/W	1	22	22
		POL	Change output polarity	R/W	1	21	21
Shadow Register [1]: (SH_CUST0)	Shadow Register [1]: (0x19)	CLAMP_EN	Enable output clamps	R/W	1	20	20
		FAULT_DIS	Disable fault	R/W	1	19	19
		FAULTR_DIS	Disconnect fault internal pull-up resistor	R/W	1	18	18
		QVO	Offset adjustment	R/W	9	17	9
		SENS_FINE	Sensitivity fine adjustment	R/W	9	8	0
EEPROM: (EE_CUST1)	EEPROM: (0x0A)	OCF_HYST	Overcurrent fault hysteresis	R/W	2	25	24
		FAULT_LATCH	Enable fault latch	R/W	1	23	23
		OCF_P_DIS	Disable positive overcurrent fault	R/W	1	22	22
		OCF_N_DIS	Disable negative overcurrent fault	R/W	1	21	21
		OCF_QUAL	Overcurrent fault qualifier/short-pulse filter	R/W	3	20	18
		OTF_THRESH	Overtemperature fault threshold	R/W	4	17	14
Shadow Register [1]: (SH_CUST1)	Shadow Register [1]: (0x1a)	OCF_N_THRES	Negative overcurrent fault threshold	R/W	7	13	7
		OCF_P_THRES	Positive overcurrent fault threshold	R/W	7	6	0
EEPROM: (EE_CUST2)	EEPROM: (0x0B)	C_SPARE	Customer scratchpad No effect on device functionality	R/W	26	25	0
Volatile Register: (FAULT_STATUS)	Volatile Register: (0x20)	TEMP_OUT	Temperature output	R	12	27	16
		UV_STAT	Undervoltage status	R	1	12	12
		OV_STAT	Overvoltage status	R	1	11	11
		OC_STAT	Overcurrent status	R	1	10	10
		OT_STAT	Overtemperature status	R	1	9	9
		FP_STAT	FAULT pin status	R	1	8	8
		UV_EV	Undervoltage event	R	1	4	4
		OV_EV	Overvoltage event	R	1	3	3
		OC_EV	Overcurrent event	R	1	2	2
		OT_EV	Overtemperature event	R	1	1	1
		FP_EV	FAULT pin event	R	1	0	0

[1] Shadow registers are volatile memory; upon startup, device loads EEPROM memory into shadow registers. Shadow registers can be used to test different programming options without erasing EEPROM (e.g., finding sensitivity and QVO codes before writing into EEPROM).

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DEFINITIONS OF ACCURACY CHARACTERISTICS

SENSITIVITY (Sens)

The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied. This proportionality is specified as the magnetic sensitivity, Sens (mv/G), of the device, and it is defined as:

$$Sens = \frac{V_{OUT(B1)} - V_{OUT(B2)}}{B1 - B2}$$

where B1 and B2 are two different magnetic field levels.

SENSITIVITY ERROR

The sensitivity error is the percent difference between the measured sensitivity and the ideal sensitivity. For example, in the case of V_{CC} = 5 V:

$$E_{Sens} = \frac{Sens_{Meas(5V)} - Sens_{Ideal(5V)}}{Sens_{Ideal(5V)}} \times 100\ (\%)$$

SENSITIVITY ERROR RELATIVE TO SENSITIVITY AT 25°C ($\Delta SENS_{TC}$)

The sensitivity error relative to sensitivity at 25°C is the percent difference between the measured sensitivity at a given temperature and the sensitivity measured at 25°C. For example, in the case of V_{CC} = 5 V:

$$\Delta SENS_{TC} = \frac{Sens_{Meas(5V)} - Sens_{Meas25C(5V)}}{Sens_{Meas25C(5V)}} \times 100\ (\%)$$

NONLINEARITY (E_{LIN})

Nonlinearity is a measure of how linear the output of the sensor IC is over the full current measurement range. The nonlinearity is calculated as:

$$E_{LIN} = \left\{1 - \left[\frac{Sens_{BPRMax}}{Sens_{BPRHalf}}\right]\right\} \times 100\ (\%)$$

where $Sens_{BPRMax}$ is the sensitivity measured at the full range output level, and $Sens_{BPRHalf}$ is the sensitivity measured at half of the full range output level.

RATIOMETRY

The device features a ratiometric output. This means that the quiescent voltage output, $V_{OUT(Q)}$, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.

The ratiometric change in the quiescent voltage output is defined as:

$$V_{RatERRQVO} = \left[\left(V_{OUTQ(5V)} \times \frac{V_{CC}}{5\ V}\right) - V_{OUTQ(VCC)}\right] \times 1000\ (mV)$$

The ratiometric change (%) in sensitivity is defined as:

$$Rat_{ERRSens} = \left[1 - \frac{\left(\frac{Sens_{(VCC)}}{Sens_{(5V)}}\right)}{\left(\frac{V_{CC}}{5\ V}\right)}\right] \times 100\ (\%)$$

The ratiometric change (%) in clamp voltage is defined as:

$$Rat_{ERRCLP} = \left[1 - \frac{\left(\frac{V_{CLP(VCC)}}{V_{CLP(5V)}}\right)}{\left(\frac{V_{CC}}{5\ V}\right)}\right] \times 100\ (\%)$$

QUIESCENT OUTPUT VOLTAGE—QVO (ZERO FIELD OUTPUT VOLTAGE)

The quiescent output voltage is the output of the sensor when the sensed differential field is zero (in typical applications when no current is flowing in the busbar/PCB). It nominally remains at 0.5 × V_{CC} for a bidirectional device and 0.1 × V_{CC} for a unidirectional device. For example, in the case of a bidirectional output device, V_{CC} = 5 V translates into $V_{OUT(Q)}$ = 2.5 V. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

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POWER-ON RESET VOLTAGE (V_{POR})

On power-up, to initialize to a known state and avoid current spikes, the device is held in the reset state. The reset signal is disabled when V_{CC} reaches V_{PORH} and time t_{PORR} has elapsed, allowing the output voltage to go from a high-impedance state into typical operation. After t_{PORR}, the output remains high impedance until V_{CC} exceeds V_{UVLOD} for more than t_{UVLOD}. During power-down, the reset signal is enabled when V_{CC} reaches V_{PORL}, causing the output voltage to go into a high-impedance state.

POWER-ON RESET RELEASE TIME (t_{PORR})

When V_{CC} rises to V_{PORH}, the power-on reset counter starts. The device output voltage transitions from a high-impedance state to typical operation only when the power-on reset counter has reached t_{PORR} and V_{CC} has been maintained above V_{PORH}.

OVERVOLTAGE DETECTION (V_{OVD})

When V_{CC} is raised above the overvoltage detection enable voltage (V_{OVDE}), the ACS37611 output stage enters high impedance. V_{OUT} floats to V_{CC} with a pull-up R_L or to GND with a pull-down R_L when (V_{OVDE}) is reached. When programming the ACS37611 using V_{OUT} (Mode 1), overvoltage detection must be active for communication. The device output resumes typical operation after V_{CC} is below the overvoltage detection disable voltage (V_{OVDD}).

If the COM_LOCK bit is set, overvoltage detection becomes disabled and the device output does not respond to the overvoltage condition.

Note that supply voltage limits still apply for operating characteristics. Following an overvoltage condition, the supply voltage should not exceed 7.5 V for more than 1 minute. For more details, refer to the Overvoltage Detection (V_{OVD}) section.

OUTPUT SATURATION VOLTAGE (V_{SAT})

When output voltage clamps are disabled, the output voltage can swing to a maximum of $V_{SAT(HIGH)}$ and to a minimum of $V_{SAT(LOW)}$.

BROKEN-WIRE VOLTAGE (V_{BRK})

If the GND pin is disconnected (broken-wire event), the output voltage goes to $V_{BRK(HIGH)}$ (if a load resistor is connected to VCC) or to $V_{BRK(LOW)}$ (if a load resistor is connected to GND).

UNDERVOLTAGE DETECTION (V_{UVLO})

When V_{CC} drops below the undervoltage detection enable voltage (V_{UVLOE}), the ACS37611 output stage drops close to GND, beyond the clamp or saturation voltage. The device output resumes typical operation after V_{CC} exceeds the undervoltage detection disable voltage (V_{UVLOD}).

Undervoltage detection is only active on the 5 V variant.

For more details, refer to the Undervoltage Detection (V_{UVLO}) section.

LOW-POWER MODE

The device is available in a low-power-mode variant, where the current draw by the IC is reduced through factory programing. In this variant, the output noise is increased by ~30% compared to the full-power-mode variant.

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DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-on time, t_{PO}, is defined as the time it takes for the output voltage to settle within ±10% of its steady-state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in Figure 38.

Temperature Compensation Power-On Time (t_{TC}). After Power-on time (t_{PO}) elapses, t_{TC} is also required before a valid temperature-compensated output.

Response Time ($t_{RESPONSE}$). The time interval between a) when the sensed current reaches 90% of its final value, and b) when the sensor output reaches 90% of its full-scale value, as shown in Figure 40.

Rise Time (t_r). The time interval between a) when the sensor reaches 10% of its full-scale value, and b) when it reaches 90% of its full-scale value, as shown in Figure 39.

Propagation Delay (t_{pd}). The time interval between a) when the sensed current reaches 20% of its full-scale value, and b) when the sensor output reaches 20% of its full-scale value, as shown in Figure 39.

Delay to Clamp (t_{CLP}). A large magnetic input step may cause the clamp to overshoot its steady-state value. The delay to clamp, t_{CLP}, is defined as: the time it takes for the output voltage to settle within ±1% of the clamp voltage dynamic range, after initially passing through its steady-state voltage, as shown in Figure 41.

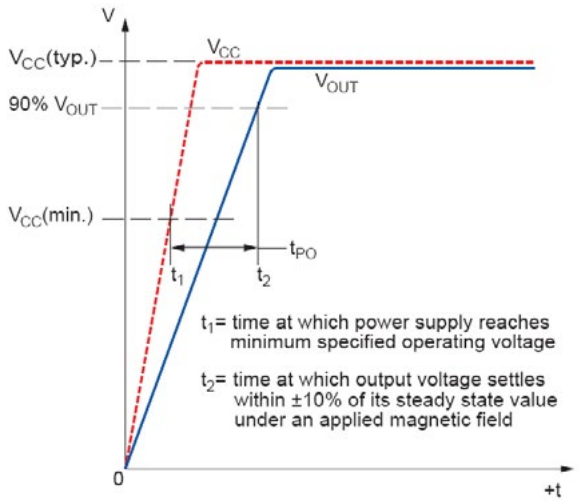

Figure 38: Power-On Time (t_{PO})

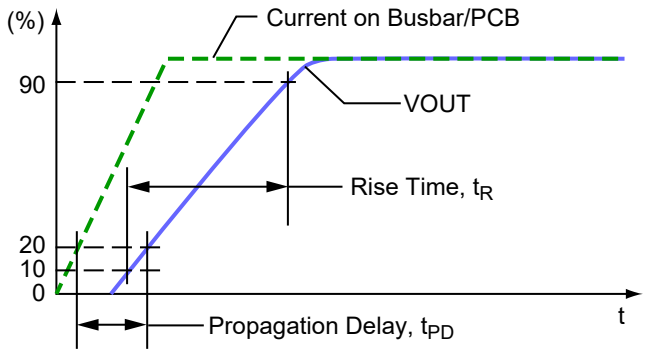

Figure 39: Propagation Delay (t_{PD}) and Rise Time (t_r)

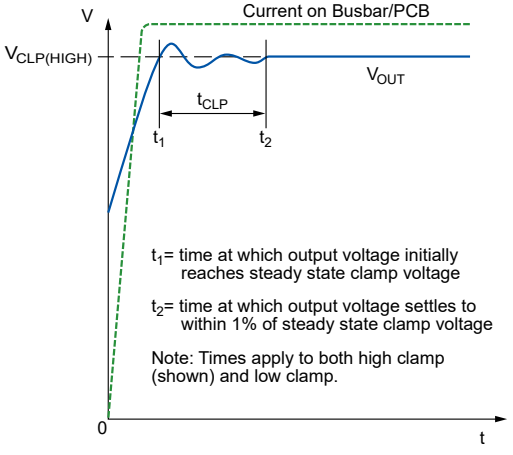

Figure 41: Delay to Clamp

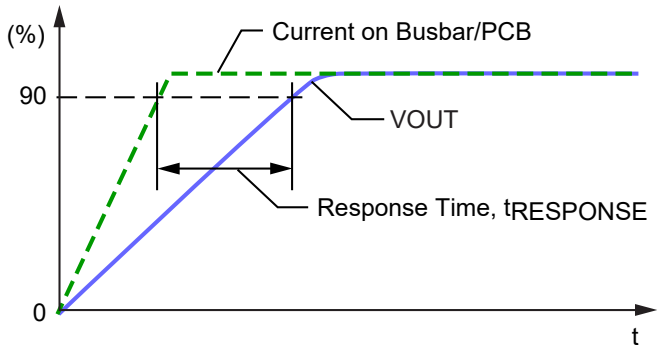

Figure 40: Response Time ($t_{RESPONSE}$)

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POWER-ON RESET, UNDERVOLTAGE AND OVERVOLTAGE DETECTION OPERATION

The descriptions in this section assume: temperature = 25°C, no output load (R_L, C_L), and no significant magnetic field is present.

Power-Up. At power-up, as V_{CC} ramps up, the output is in a high-impedance state. When V_{CC} crosses V_{PORH} (location [1] in Figure 42 and [1'] in Figure 43), the POR release counter starts counting for t_{PORR}. At this point, if V_{CC} exceeds V_{UVLOD} [2'], the output goes to V_{CC} / 2 after t_{UVLOD} [3'].
If V_{CC} does not exceed V_{UVLOD} [2], the output stays in the high-impedance state until V_{CC} reaches V_{UVLOD} [3], then goes to V_{CC}/2 after t_{UVLOD} [4].

V_{CC} drops below V_{CC}(min) = 4.5 V. If V_{CC} drops below V_{UVLOE} [4', 5], the UVLO enable counter starts counting. If V_{CC} is still below V_{UVLOE} when the counter reaches t_{UVLOE}, the UVLO function becomes enabled and the output is pulled near GND [6]. If V_{CC} exceeds V_{UVLOE} before the UVLO enable counter reaches t_{UVLOE} [5'], the output continues to be V_{CC}/2.

Coming out of UVLO. While UVLO is enabled [6], if V_{CC} exceeds V_{UVLOD} [7], UVLO becomes disabled after t_{UVLOD}, and the output becomes V_{CC}/2 [8].

Power-Down. As V_{CC} ramps down below V_{UVLOE} [6', 9], the UVLO enable counter starts counting. If V_{CC} exceeds V_{PORL} when the counter reaches t_{UVLOE}, the UVLO function becomes enabled and the output is pulled near GND [10]. The output enters a high-impedance state as V_{CC} goes below V_{PORL} [11]. If V_{CC} falls below V_{PORL} before the UVLO enable counter reaches t_{UVLOE}, the output transitions directly to a high-impedance state [7'].

Overvoltage. If V_{CC} rises beyond V_{OVDE}, the OVD enable counter starts counting. If the internal pull-up mode is used, the fault pull-up voltage follows V_{CC}; otherwise, it remains at the V_F level. If V_{CC} remains above V_{OVDE} when the counter reaches t_{OVDE}, the OVD function becomes enabled and the output goes to a high-impedance state. The FAULT pin becomes disabled when going to a high-impedance state.

Coming Out of OVD. While OVD is enabled, if V_{CC} drops below V_{OVDD}, OVD becomes disabled after t_{OVDD}, and the output returns to typical operation in analog mode V_{CC}/2. The FAULT pin becomes active, and the device recovers to typical operation.

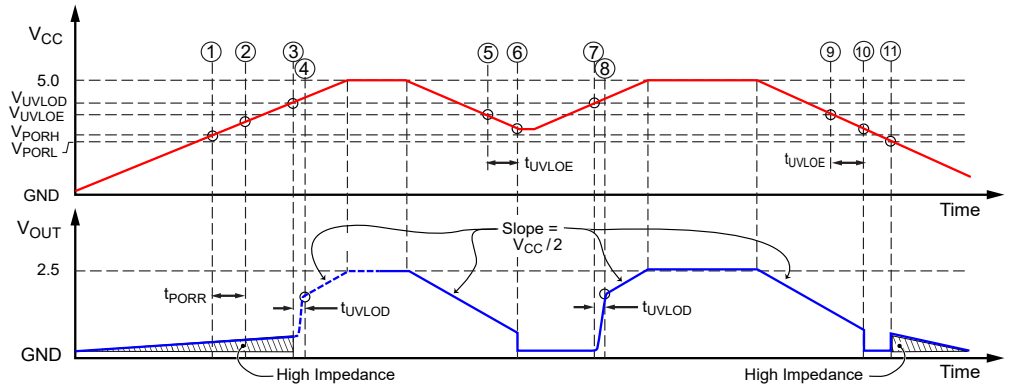

Figure 42: POR and UVLO Operation—Slow Rise Time Case

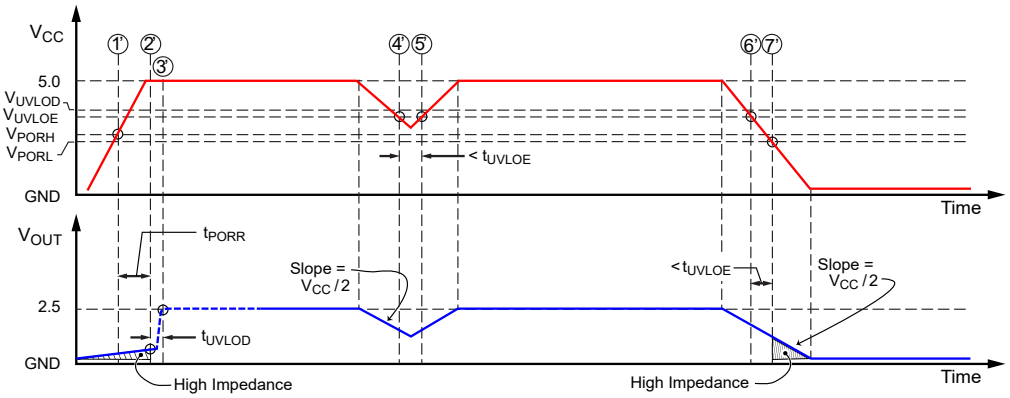

Figure 43: POR and UVLO Operation—Fast Rise Time Case

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APPLICATION INFORMATION

Typical Application—Busbar Current Sensing

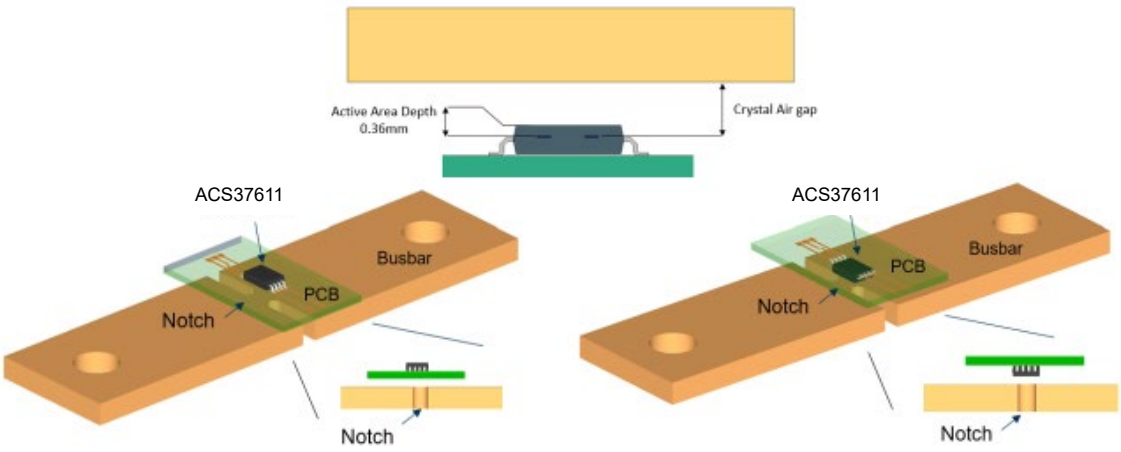

Figure 44: Busbar Current-Sensing Application—Reference Busbar Design with Notch

The ACS37611 is ideal for busbar current-sensing applications. For a given current flowing through the busbar, the magnitude of the differential magnetic field sensed by the IC depends on the air gap between the busbar and the IC. Adding a notch (width reduction) to the busbar at the location where the sensor is placed significantly increases the magnitude of the magnetic field, improving SNR.

Keeping the notch length short (2 to 3 mm) results in virtually no increase in the resistance of the busbar or degradation of its thermal performance.

Different busbar and notch dimensions can be used to optimize system performance and respond to application constraints. The dimensions of an Allegro evaluation board designed to measure ±1000 A are highlighted in Figure 44 and Table 6.

NOTE: Comparing the busbar described in Figure 44 to a bare busbar (without notch), the busbar with the 3 mm notch increases the overall impedance by less than 10 μΩ, increasing busbar temperature by only few degrees during testing.

Skin-Effect Consideration

Skin effect in the conductor tends to reduce the magnitude of the differential magnetic field measured by the IC at high frequencies (coupling factor) and therefore influences the bandwidth of the system and response time to transient current.

Skin effect depends on busbar dimensions, sensor mounting orientation, and distance between the busbar and the IC. A short notch width (~3 mm) and a busbar thickness of 4 mm provides the best response over frequency.

Table 6: Current Range Based on Reference Busbar Design

Busbar Application	Cross Section [mm²]	Notch Cross Section [mm²]	Max. Current [2] [A]	Coupling Factor [1] [G/A]	Diff. Field [1] [G]	IC Sensitivity [1] [mV/G]
16 × 4 mm Busbar + 4.5 mm Notch	64	18	±1100	0.17	±200	10

[1] Considering a distance from Hall elements to busbar of 3 mm.
[2] Full-scale current is required to cover the full-scale output range (bidirectional = ±2 V).

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Multiple Busbar Design Options

The ACS37611 offers many different mounting possibilities, addressing different needs (bandwidth, mounting tolerances, and crosstalk). The figures below show different mounting options.

For application notes explaining the tradeoffs between different topologies, refer to Allegro's website (https://www.allegromicro.com).

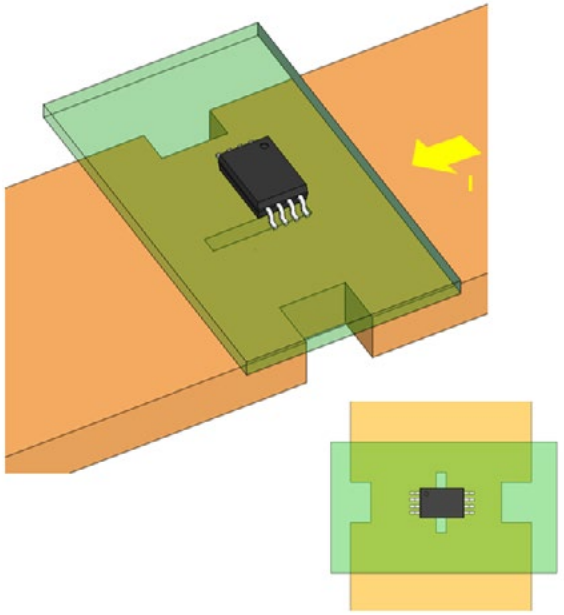

Figure 45: Rift Busbar Design
High mounting tolerances, medium coupling factor, high skin effect.
For DC to low-frequency AC applications <1 kHz.

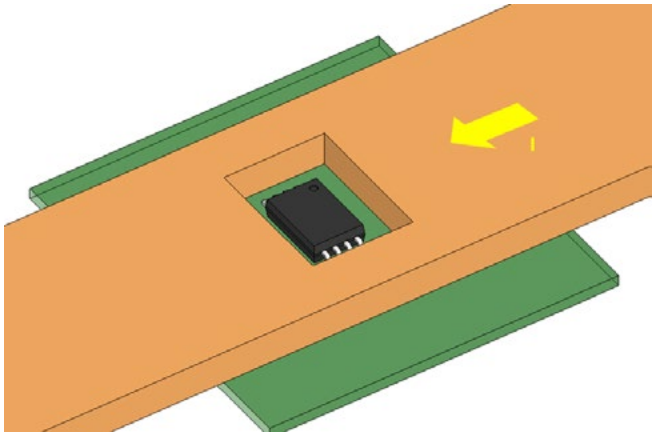

Figure 46: Slit Busbar Design
High mounting tolerances, medium coupling factor, medium skin effect.
For DC to medium-frequency AC applications <100 kHz.

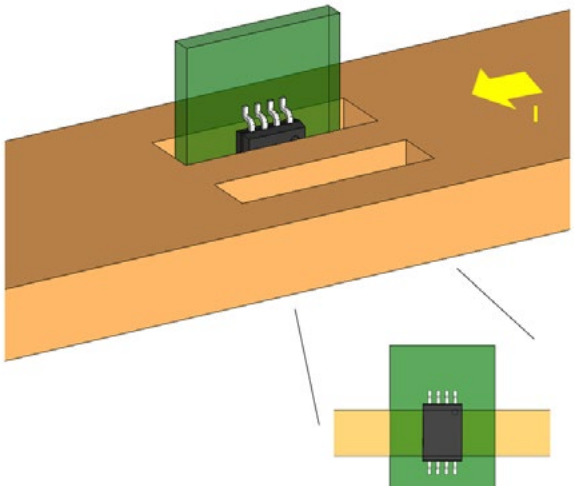

Figure 47: Dual-Vertical-Slit Busbar Design
High mounting tolerances, high coupling factor, low skin effect.
For DC to high-frequency AC applications >100 kHz.

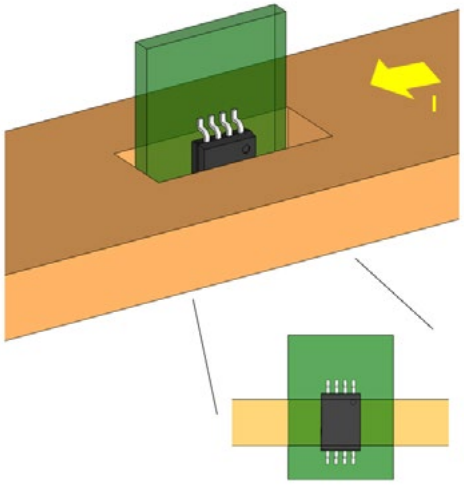

Figure 48: Vertical-Slit Busbar Design
High mounting tolerances, high coupling factor, low skin effect.
For DC to high-frequency AC applications >100 kHz.

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Typical Application—PCB Sensing

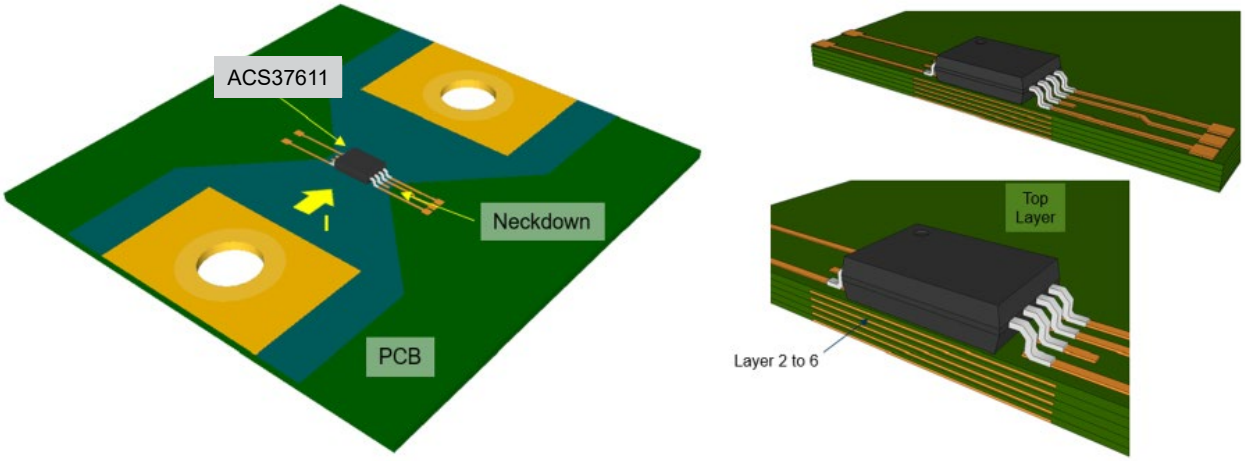

Figure 49: PCB Current-Sensing Application—Six-Layer Reference PCB Example

The ACS37611 can also be used in PCB applications where the current flows directly in the PCB instead of on a busbar.

Multiple copper layers can be used to carry the current. Reducing the width of the copper traces under the sensor (neck-down) increases the magnitude of the differential magnetic field measured by the IC.

Different copper layer dimensions and stack-ups can be used to optimize performance and are specific to the constraints of the application. For example, in higher-voltage applications, the top layer is only used for signal routing in order to use the PCB replaced by the dielectric layer for isolation.

The dimensions of three Allegro evaluation boards designed to measure a wide current range are highlighted in Figure 49 and Table 7.

Care must be taken when routing the device signal to prevent noise coupling to the supply or output lines.

The power plane in the neck-down area should also be avoided to prevent disturbing the magnetic field measured.

Skin-Effect Consideration

The skin effect in the PCB current-carrying traces tends to reduce the differential magnetic field measured by the IC at high frequencies (coupling factor) and therefore influences the bandwidth of the system and the response time to transient current.

The skin effect is generally limited in the PCB application due to the thin copper-layer thickness, but the effect depends on PCB copper trace dimensions, number of layers, and layer thickness.

Table 7: Current range based on reference PCB design:

PCB Application [1]	Maximum Current (A) [2]	Coupling Factor (G/A) [1]	Differential Field (G) [1]	IC Sensitivity (mV/G) [1]
8 Layers—Reference Designs [3]	±100	0.9	±90	22.2
	±200	0.9	±180	11.1

[1] Typical values, not including device placement and PCB manufacturing tolerances.
[2] Full-scale current required to cover the full-scale output range (bidirectional = ±2 V).
[3] Maximum continuous current without proper cooling on this Allegro evaluation PCB design should not exceed 150 A.

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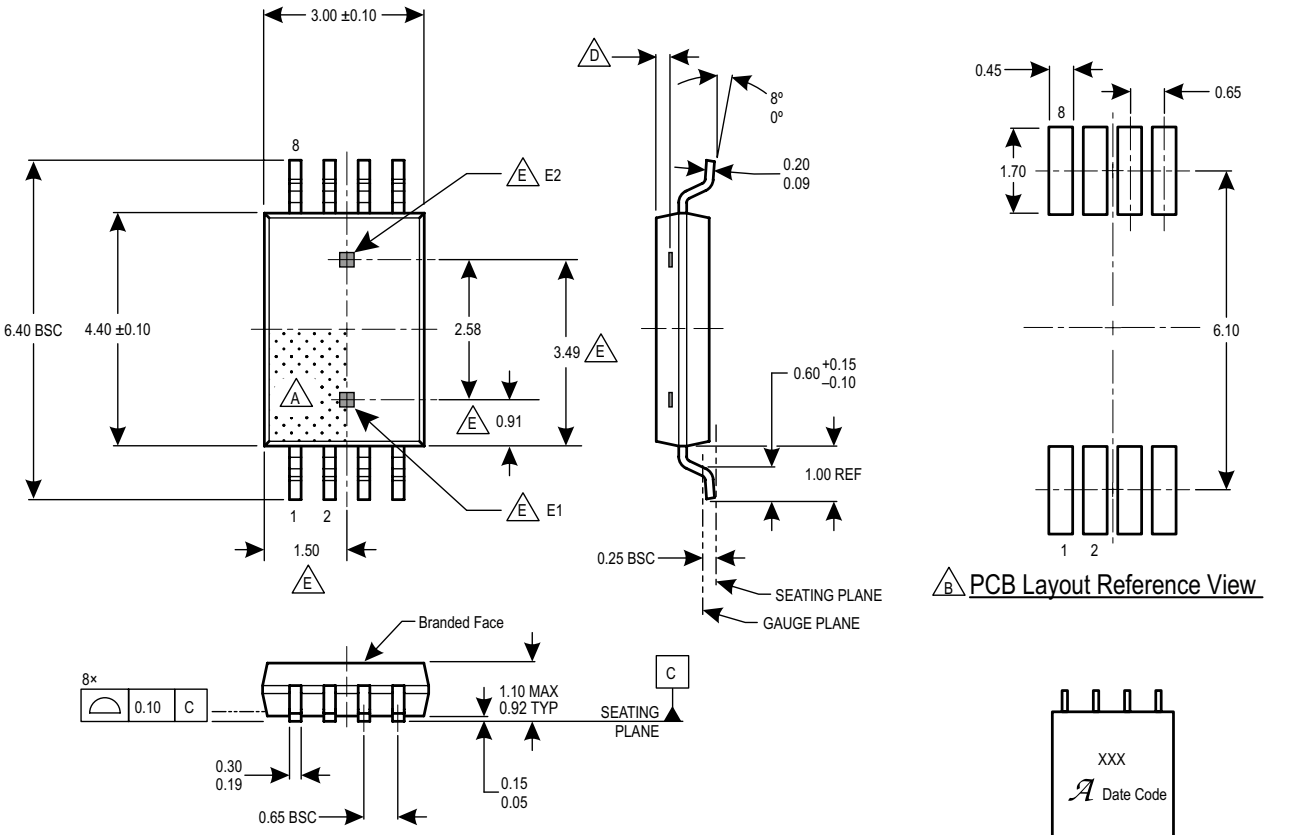
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000381, Rev. 1 and JEDEC MO-153AA)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOP65P640X110-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Branding scale and appearance at supplier discretion

D Active Area Depth 0.38 mm REF

E Hall elements (E1, E2); not to scale.

Figure 50: Package LU, 8-Pin TSSOP Package

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Revision History

Number	Date	Description
–	March 15, 2025	Initial Release
1	May 22, 2025	Added info about -005B5 variant (pages 1, 11); updated Thermal Characteristics table (page 4); updated Common Operating Characteristics (pages 8, 9); updated -010B5 Operating Charactertistics (page 12); updated Detecting ECC Error bits (page 18); minor editorial updates throughout

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