High-Bandwidth, Fast Fault Response Current Sensor IC in Thermally Enhanced Package

Not for New Design

The ACS709 is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available.

Date of status change: March 14, 2025

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, refer to ACS724.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

ACS709

High-Bandwidth, Fast Fault Response Current Sensor IC in Thermally Enhanced Package

FEATURES AND BENEFITS

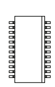
- Industry-leading noise performance with 120 kHz bandwidth through proprietary amplifier and filter design techniques
- Integrated shield greatly reduces capacitive coupling from current conductor to die due to high dV/dt, and prevents offset drift in high-side applications
- Small-footprint, surface-mount, 24-lead quarter-size small-outline package (QSOP-24)
- High isolation voltage, suitable for line-powered applications
- 1.1 mΩ primary conductor resistance for low power loss
- User-settable overcurrent fault level
- Overcurrent fault signal typically responds to an overcurrent condition in < 2 µs
- Filter pin capacitor sets analog signal bandwidth
- ±2% typical output error
- 3 to 5.5 V, single-supply operation
- Factory-trimmed sensitivity, quiescent output voltage, and associated temperature coefficients
- Chopper stabilization results in extremely stable quiescent output voltage
- Ratiometric output from supply voltage

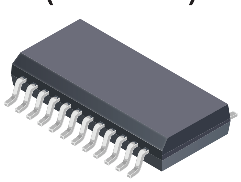
APPLICATIONS

- Motor control and protection
- Load management and overcurrent detection
- Power conversion and battery monitoring/ uninterruptible power-supply (UPS) systems

PACKAGE: 24-pin QSOP (suffix LF)

Approximate Footprint





DESCRIPTION

The Allegro™ ACS709 current sensor IC provides economical and precise means for current sensing applications in industrial, automotive, commercial, and communications systems. The device is offered in a small-footprint surface-mount package that allows easy implementation in customer applications.

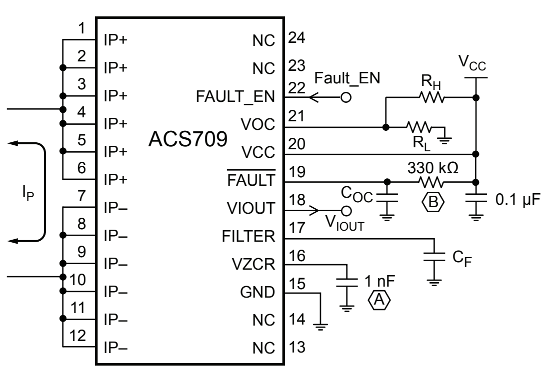
The ACS709 consists of a precision linear Hall sensor integrated circuit with a copper conduction path located near the surface of the silicon die. Applied current flows through the copper conduction path. The analog output voltage from the Hall sensor IC linearly tracks the magnetic field generated by the applied current. The accuracy of the ACS709 is maximized with this patented packaging configuration because the Hall element is situated in extremely close proximity to the current to be measured.

High-level immunity to current conductor dV/dt and stray electric fields, offered by Allegro proprietary integrated shield technology, provides low output ripple and low offset drift in high-side applications.

The voltage at the overcurrent input (VOC pin) allows customers to define an overcurrent fault threshold for the device. When the current flowing through the copper conduction path (between the IP+ and IP– pins) exceeds this threshold, the open-drain overcurrent fault pin transitions to a logic-low state. Factory programming of the linear Hall sensor IC inside of the ACS709 results in exceptional accuracy in both the analog and digital output signals.

The internal resistance of the copper path used for current sensing is typically 1.1 mΩ, for low power loss. Also, the current conduction path is electrically isolated from the low-voltage device inputs and outputs. This allows the ACS709 family of sensor ICs to be used in applications requiring electrical isolation, without the use of opto-isolators or other costly isolation techniques.

Typical Application



R_H, R_L	Sets resistor divider reference for V_{OC}
C_F	Noise- and bandwidth-limiting filter capacitor
C_{OC}	Fault delay setting capacitor, 22 nF maximum
(A)	Use of capacitor required
(B)	Use of resistor optional

SELECTION GUIDE

Part Number	$I_{P(LIN)}$ (A)	Sens (Typ) (mV/A)	T_A (°C)	Packing
-T VARIANT [1]				
ACS709LLFTR-35BB-T [2]	75	28	–40 to 150	Tape and Reel, 2500 pieces per reel
ACS709LLFTR-20BB-T	37.5	56		
ACS709LLFTR-10BB-T [2]	24	85		

[1] -T denotes Pb-contained construction with Pb-based solder bumps. -T devices are RoHS compliant using allowed exemptions provided in Annex III and IV of Directive 2011/65/EU [Exemptions 7(a), 15, 15(a), as applicable].

[2] Part variants ACS709LLFTR-35BB-T and ACS709LLFTR-10BB-T are in production but have been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of these devices is currently restricted to existing customer applications. These devices should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Date of status change: September 29, 2023.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{CC}		8	V
Filter Pin	V_{FILTER}		8	V
Analog Output Pin	V_{IOUT}		32	V
Overcurrent Input Pin	V_{OC}		8	V
Overcurrent $\overline{\text{FAULT}}$ Pin	$V_{\overline{FAULT}}$		8	V
Fault Enable (FAULT_EN) Pin	$V_{FAULTEN}$		8	V
Voltage Reference Output Pin	V_{ZCR}		8	V
DC Reverse Voltage: Supply Voltage, Filter, Analog Output, Overcurrent Input, Overcurrent Fault, Fault Enable, and Voltage Reference Output Pins	V_{Rdcx}		–0.5	V
Output Current Source	$I_{IOUT(Source)}$		3	mA
Output Current Sink	$I_{IOUT(Sink)}$		1	mA
Operating Ambient Temperature	T_A	Range L	–40 to 150	°C
Junction Temperature	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 170	°C

ISOLATION CHARACTERISTICS

Characteristic	Symbol	Notes	Rating	Unit
Dielectric Strength Test Voltage [1]	V_{ISO}	Agency type-tested for 60 seconds per UL standard 1577	1750	VAC
Working Voltage for Basic Isolation	V_{WFSI}	For basic (single) isolation per UL standard 1577; for higher continuous voltage ratings, contact Allegro	277	VAC

[1] Allegro does not conduct 60-second testing. It is done only during the UL certification process.

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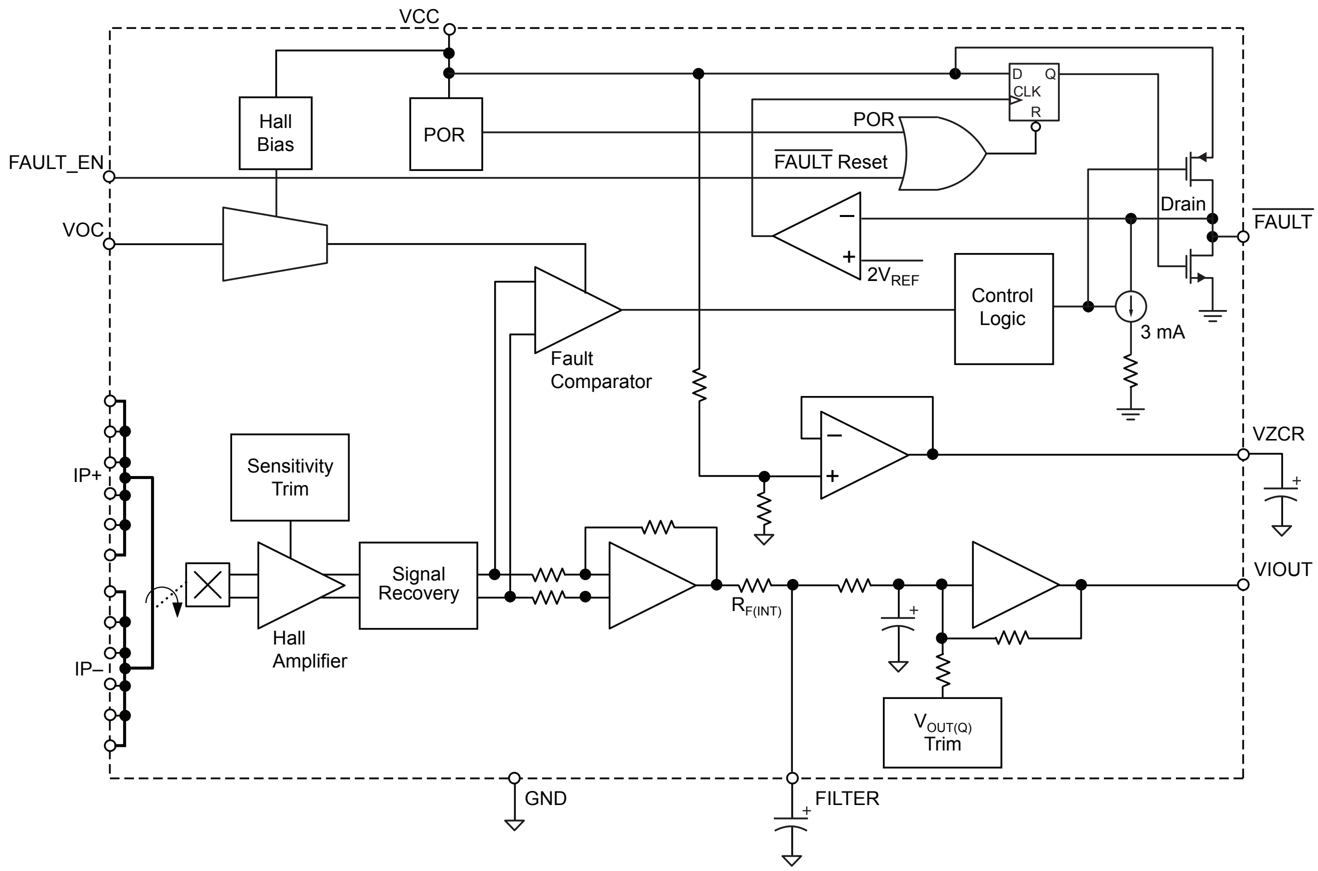
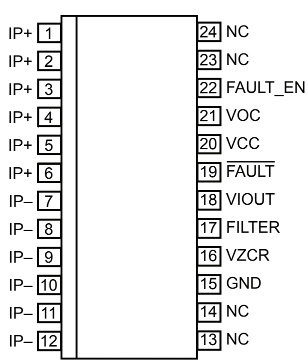
Functional Block Diagram



Pinout Diagram



Terminal List

Number	Name	Description
1 through 6	IP+	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP– pins; unidirectional or bidirectional current flow.
7 through 12	IP–	Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to IP+ pins; unidirectional or bidirectional current flow.
13, 14, 23, 24	NC	No connection
15	GND	Device ground connection.
16	VZCR	Voltage reference output pin. Zero-current (0 A) reference; output voltage on this pin scales with V_{CC}.
17	FILTER	Filter pin. Terminal for an external capacitor connected from this pin to GND to set the device bandwidth.
18	VIOUT	Analog output pin. Output voltage on this pin is proportional to current flowing through the loop between the IP+ pins and IP– pins.
19	$\overline{\text{FAULT}}$	Overcurrent fault pin. When current flowing between IP+ pins and IP– pins exceeds the overcurrent fault threshold, this pin transitions to a logic-low state.
20	VCC	Supply voltage.
21	VOC	Overcurrent input pin. Analog input voltage on this pin sets the overcurrent fault threshold.
22	FAULT_EN	Enables overcurrent faulting when high. Resets $\overline{\text{FAULT}}$ when low.

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COMMON OPERATING CHARACTERISTICS: Valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS						
Supply Voltage [1]	V_{CC}		3	–	5.5	V
Nominal Supply Voltage	V_{CCN}		–	5	–	V
Supply Current	I_{CC}	VIOUT open, FAULT pin high	–	11	14.5	mA
Output Capacitance Load	C_{LOAD}	VIOUT pin to GND	–	–	10	nF
Output Resistive Load	R_{LOAD}	VIOUT pin to GND	10	–	–	kΩ
Magnetic Coupling from Device Conductor to Hall Element	MC_{HALL}	Current flowing from IP+ to IP– pins	–	9.5	–	G/A
Internal Filter Resistance [2]	$R_{F(INT)}$		–	1.7	–	kΩ
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.1	–	mΩ
ANALOG OUTPUT SIGNAL CHARACTERISTICS						
Full Range Linearity [3]	E_{LIN}	$I_P = \pm I_{P0A}$	–0.75	±0.25	0.75	%
Symmetry [4]	E_{SYM}	$I_P = \pm I_{P0A}$	99.1	100	100.9	%
Bidirectional Quiescent Output	$V_{OUT(QBI)}$	I_P = 0 A, T_A = 25°C	–	V_{CC}×0.5	–	V
TIMING PERFORMANCE CHARACTERISTICS						
VIOUT Signal Rise Time	t_r	T_A = 25°C, swing I_P from 0 A to I_{P0A}, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	3	–	μs
VIOUT Signal Propagation Time	t_{PROP}	T_A = 25°C, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	1	–	μs
VIOUT Signal Response Time	$t_{RESPONSE}$	T_A = 25°C, swing I_P from 0 A to I_{P0A}, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	4	–	μs
VIOUT Large Signal Bandwidth [5]	f_{3dB}	–3 dB, T_A = 25°C, no capacitor on FILTER pin, 100 pF from VIOUT to GND	–	120	–	kHz
Power-On Time	t_{PO}	Output reaches 90% of steady-state level, no capacitor on FILTER pin, T_A = 25°C	–	35	–	μs
OVERCURRENT CHARACTERISTICS						
Setting Voltage for Overcurrent Switch Point [6]	V_{OC}		V_{CC}×0.25	–	V_{CC}×0.4	V
Signal Noise at Overcurrent Comparator Input	I_{NCOMP}		–	±1	–	A
Overcurrent Fault Switch Point Error [7][8]	E_{OC}	Switch point in V_{OC} safe operating area; assumes I_{NCOMP} = 0 A	–	±5	–	%
Overcurrent $\overline{\text{FAULT}}$ Pin Output Voltage	$V_{\overline{FAULT}}$	1 mA sink current at $\overline{\text{FAULT}}$ pin	–	–	0.4	V
Fault Enable (FAULT_EN Pin) Input Low Voltage Threshold	V_{IL}		–	–	0.1×V_{CC}	V
Fault Enable (FAULT_EN Pin) Input High Voltage Threshold	V_{IH}		0.8×V_{CC}	–	–	V
Fault Enable (FAULT_EN Pin) Input Resistance	R_{FEI}		–	1	–	MΩ

Continued on the next page…

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COMMON OPERATING CHARACTERISTICS (continued): Valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
OVERCURRENT CHARACTERISTICS (continued)						
Fault Enable (FAULT_EN Pin) Delay [9]	t_{FED}	1. Set FAULT_EN to low, V_{OC} = 0.25 × V_{CC}, C_{OC} = 0 F 2. Run a DC I_P that exceeds the corresponding overcurrent threshold 3. Reset FAULT_EN from low to high 4. Measure delay from rising edge of FAULT_EN to falling edge of $\overline{\text{FAULT}}$	–	15	–	μs
Overcurrent Fault Response Time	t_{OC}	FAULT_EN set to high for a minimum of 20 μs before the overcurrent event; switch point set at V_{OC} = 0.25 × V_{CC}; delay from I_P exceeding overcurrent fault threshold to $V_{\overline{FAULT}}$ < 0.4 V, without external C_{OC} capacitor	–	1.9	–	μs
Overcurrent Fault Reset Delay	t_{OCR}	Time from $V_{FAULTEN}$ < V_{IL} to V_{FAULT} > 0.8 × V_{CC}, R_{PU} = 330 kΩ	–	500	–	ns
Overcurrent Fault Reset Hold Time	t_{OCH}	Time from $V_{FAULTEN}$ pin < V_{IL} to reset of fault latch; see Functional Block Diagram	–	250	–	ns
Overcurrent Input Pin Resistance	R_{OC}	T_A = 25°C, VOC pin to GND	2	–	–	MΩ
VOLTAGE REFERENCE CHARACTERISTICS						
Voltage Reference Output	V_{ZCR}	T_A = 25 °C	–	0.5 × V_{CC}	–	V
Voltage Reference Output Load Current	I_{ZCR}	Source current	3	–	–	mA
		Sink current	50	–	–	μA
Voltage Reference Output Drift	ΔV_{ZCR}		–	±10	–	mV

[1] Devices are trimmed for maximum accuracy at V_{CC} = 5 V. The ratiometry feature of the device allows operation over the full V_{CC} range; however, accuracy may be slightly degraded for V_{CC} values other than 5 V.
[2] $R_{F(INT)}$ forms an RC circuit via the FILTER pin.
[3] This parameter can drift by as much as 0.25% over the lifetime of this product.
[4] This parameter can drift by as much as 0.3% over the lifetime of this product.
[5] Calculated using the formula $f_{3dB} = 0.35 / t_r$.
[6] For instructions to set the overcurrent fault switch point, see the Setting Overcurrent Fault Switch Point section.
[7] Switch point can be lower at the expense of switch-point accuracy.
[8] This error specification does not include the effect of noise. To factor in the additional influence of noise on the fault switch point, see the I_{NCOMP} specification.
[9] Fault enable delay is designed to avoid false tripping of an overcurrent (OC) fault at power-up. A 15 μs (typical) delay is needed every time FAULT_EN rises from low to high. Before this delay occurs, the device is not ready to respond to an overcurrent event.

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***X*10BB PERFORMANCE CHARACTERISTICS, T_A Range L, valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	$I_{P(OA)}$		–10	–	10	A
Linear Sensing Range	$I_{P(LIN)}$		–24	–	24	A
Performance Characteristics at V_{CC} = 5 V						
Noise [1]	$V_{NOISE(rms)}$	T_A = 25°C, Sens = 85 mV/A, C_f = 0, C_{LOAD} = 4.7 nF, R_{LOAD} open	–	2.3	–	mV
Sensitivity [2][3]	Sens	I_P = 10 A, T_A = 25°C	–	85	–	mV/A
		I_P = 10 A, T_A = 25°C to 150°C	82	85	88	mV/A
		I_P = 10 A, T_A = –40°C to 25°C	80	85	90	mV/A
Electrical Offset Voltage [2]	V_{OE}	I_P = 0 A, T_A = 25°C	–	±5	–	mV
		I_P = 0 A, T_A = 25°C to 150°C	–30	–	30	mV
		I_P = 0 A, T_A = –40°C to 25°C	–45	–	45	mV
Total Output Error [2][4]	E_{TOT}	Tested at I_P =10 A, I_P applied for 5 ms, T_A = 25°C to 150°C	–	±2	–	%
		Tested at I_P =10 A, I_P applied for 5 ms, T_A = –40°C to 25°C	–	±4	–	%

[1] V_{pk-pk} noise (6-sigma noise) is equal to 6 × $V_{NOISE(rms)}$. To achieve lower noise levels, use C_f for applications requiring narrower bandwidth. For graphs of noise versus C_f and bandwidth versus C_f, see the Characteristic Performance section.
[2] For parameter distribution over ambient temperature range, see the Characteristic Performance Data section.
[3] This parameter can drift by as much as 1.75% over lifetime of the product.
[4] This parameter can drift by as much as 2.5% over lifetime of the product.

***X*20BB PERFORMANCE CHARACTERISTICS, T_A Range L, valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified**

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	$I_{P(OA)}$		–20	–	20	A
Linear Sensing Range	$I_{P(LIN)}$		–37.5	–	37.5	A
Performance Characteristics at V_{CC} = 5 V						
Noise [1]	$V_{NOISE(rms)}$	T_A = 25°C, Sens = 56 mV/A, C_f = 0, C_{LOAD} = 4.7 nF, R_{LOAD} open	–	1.50	–	mV
Sensitivity [2][3]	Sens	I_P = 12.5 A, T_A = 25°C	–	56	–	mV/A
		I_P = 12.5 A, T_A = 25°C to 150°C	54.5	–	58	mV/A
		I_P = 12.5 A, T_A = –40°C to 25°C	54.5	–	58.5	mV/A
Electrical Offset Voltage [2]	V_{OE}	I_P = 0 A, T_A = 25°C	–	±5	–	mV
		I_P = 0 A, T_A = 25°C to 150°C	–25	–	25	mV
		I_P = 0 A, T_A = –40°C to 25°C	–40	–	40	mV
Total Output Error [2][4]	E_{TOT}	Tested at I_P =12.5 A, I_P applied for 5 ms, T_A = 25°C to 150°C	–	±2	–	%
		Tested at I_P =12.5 A, I_P applied for 5 ms, T_A = –40°C to 25°C	–	±3	–	%

[1] V_{pk-pk} noise (6-sigma noise) is equal to 6 × $V_{NOISE(rms)}$. To achieve lower noise levels, use C_f for applications requiring narrower bandwidth. For graphs of noise versus C_f and bandwidth versus C_f, see the Characteristic Performance section.
[2] For parameter distribution over ambient temperature range, see the Characteristic Performance Data section.
[3] This parameter can drift by as much as 1.75% over lifetime of the product.
[4] This parameter can drift by as much as 2.5% over lifetime of the product.

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X35BB PERFORMANCE CHARACTERISTICS, T_A Range L, valid at T_A = –40°C to 150°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Optimized Accuracy Range	$I_{P(OA)}$		–37.5	–	37.5	A
Linear Sensing Range	$I_{P(LIN)}$		–75	–	75	A
Performance Characteristics at V_{CC} = 5 V						
Noise [1]	$V_{NOISE(rms)}$	T_A = 25°C, Sens = 28 mV/A, C_f = 0, C_{LOAD} = 4.7 nF, R_{LOAD} open	–	1	–	mV
Sensitivity [2][3]	Sens	I_P = 25 A, T_A = 25°C	–	28	–	mV/A
		I_P = 25 A, T_A = 25°C to 150°C	27	–	29.5	mV/A
		I_P = 25 A, T_A = –40°C to 25°C	27	–	29.5	mV/A
Electrical Offset Voltage [2]	V_{OE}	I_P = 0 A, T_A = 25°C	–	±5	–	mV
		I_P = 0 A, T_A = 25°C to 150°C	–25	–	25	mV
		I_P = 0 A, T_A = –40°C to 25°C	–40	–	40	mV
Total Output Error [2][4]	E_{TOT}	Tested at I_P = 25 A, I_P applied for 5 ms, T_A = 25°C to 150°C	–	±3	–	%
		Tested at I_P = 25 A, I_P applied for 5 ms, T_A = –40°C to 25°C	–	±3	–	%

[1] V_{pk-pk} noise (6 sigma noise) is equal to 6 × $V_{NOISE(rms)}$. To achieve lower noise levels, use C_f for applications requiring narrower bandwidth. For graphs of noise versus C_f and bandwidth versus C_f, see the Characteristic Performance section.
[2] For parameter distribution over ambient temperature range, see the Characteristic Performance Data section.
[3] This parameter can drift by as much as 1.75% over lifetime of the product.
[4] This parameter can drift by as much as 2.5% over lifetime of the product.

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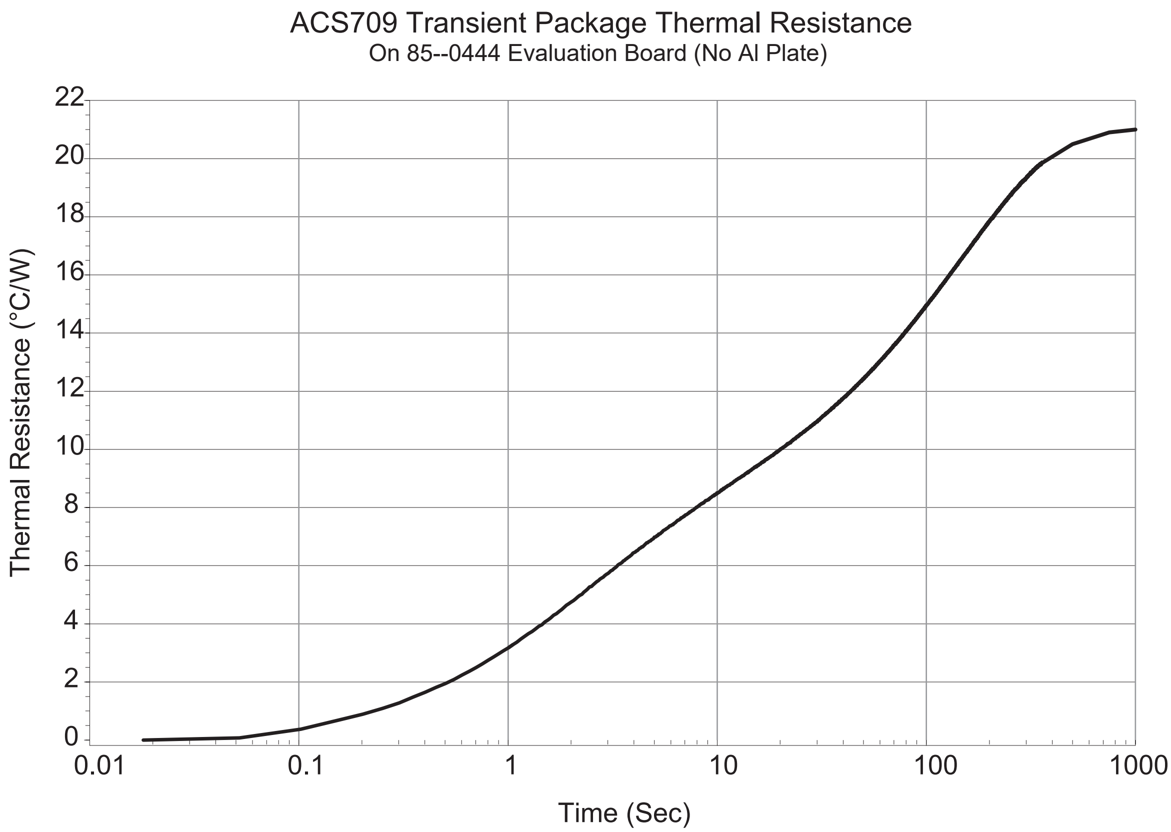
THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Value	Units
Steady-State Package Thermal Resistance	$R_{\theta JA}$	Tested with 30 A DC current and based on ACS709 evaluation board in 1 cu. ft. of still air. For detailed information about the ACS709 evaluation board, refer to the product page on the Allegro website	21	°C/W
Transient Package Thermal Resistance	$R_{T\theta JA}$	Tested with 30 A DC current and based on ACS709 evaluation board in 1 cu. ft. of still air. For detailed information about the ACS709 evaluation board, refer to the product page on the Allegro website.	See graph	°C/W



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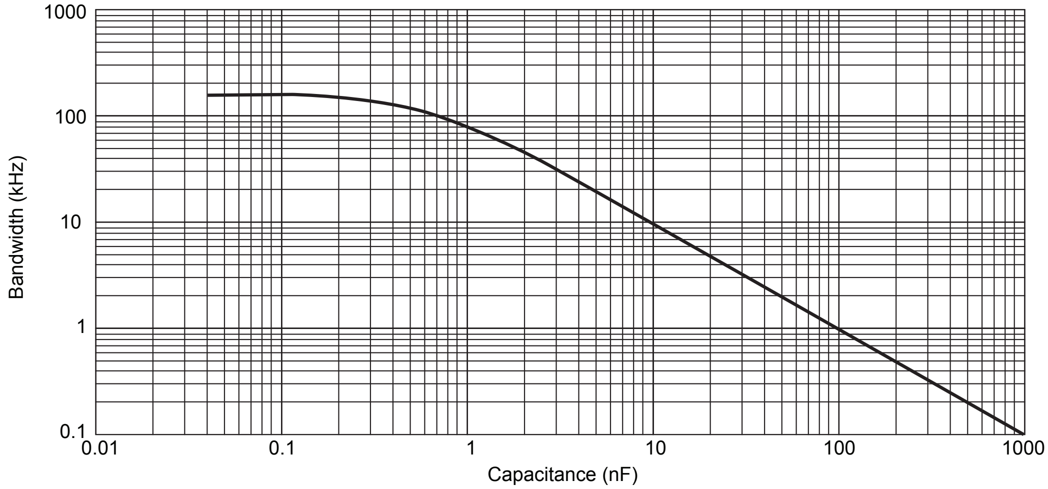
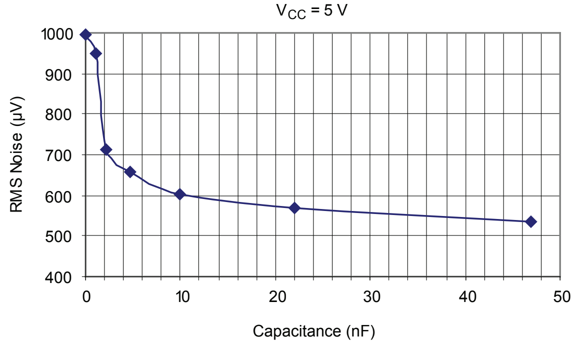
CHARACTERISTIC PERFORMANCE

ACS709 Bandwidth versus External Capacitor Value, C_F
Capacitor connected between FILTER pin and GND

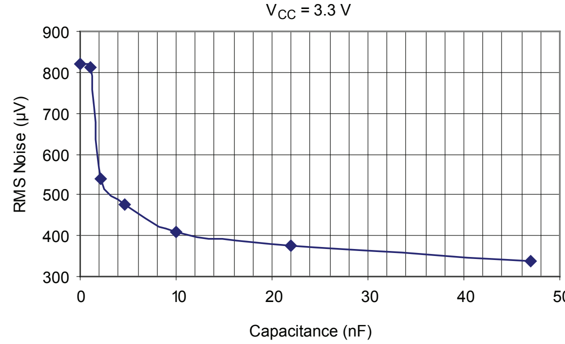


ACS709 Noise versus External Capacitor Value, C_F
Capacitor connected between FILTER pin and GND

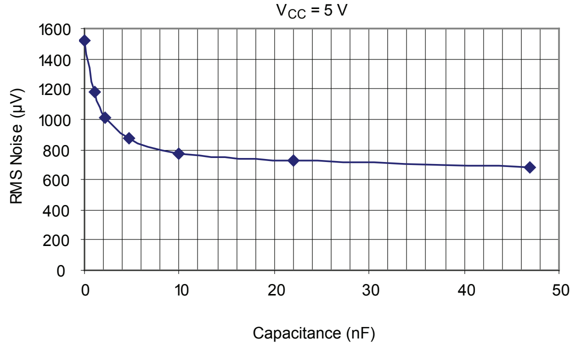
ACS709x-35B
V_{CC} = 5 V



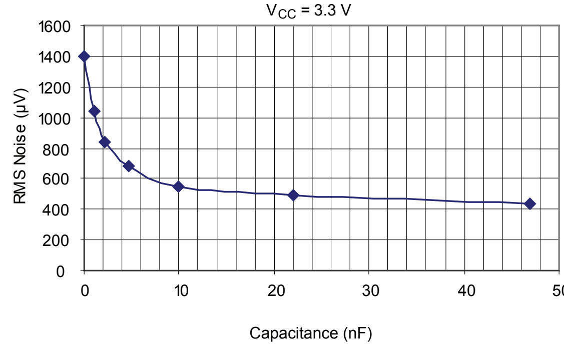
ACS709x-35B
V_{CC} = 3.3 V



ACS709x-20B
V_{CC} = 5 V



ACS709x-20B
V_{CC} = 3.3 V



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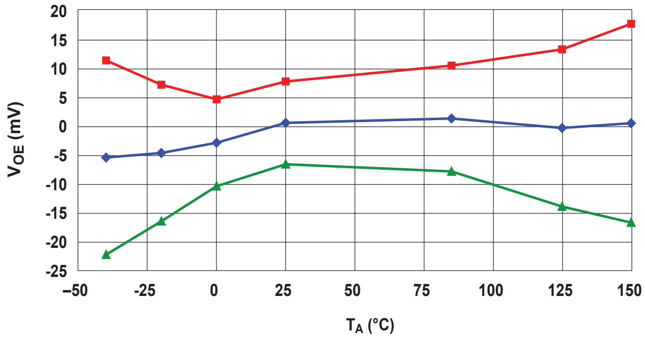
CHARACTERISTIC PERFORMANCE DATA

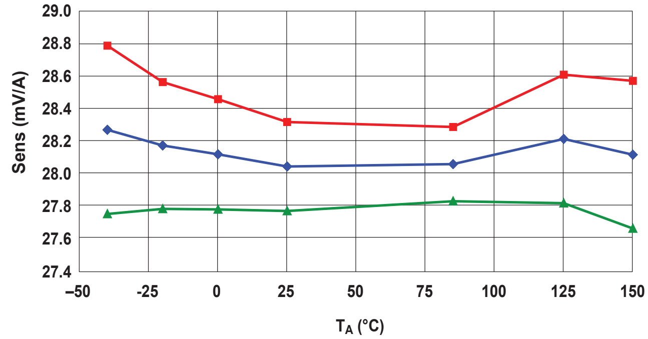
Data taken using the ACS709-35BB, V_{CC} = 5 V

Accuracy Data

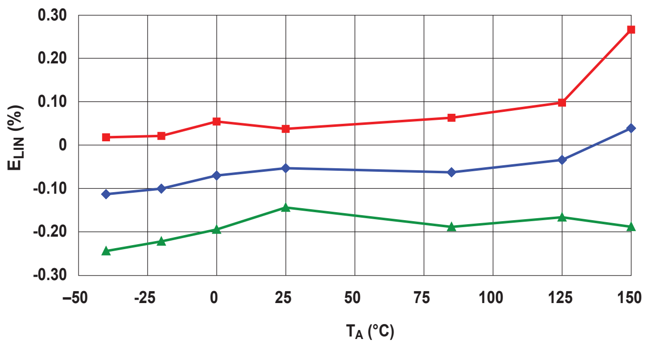
Electrical Offset Voltage versus Ambient Temperature



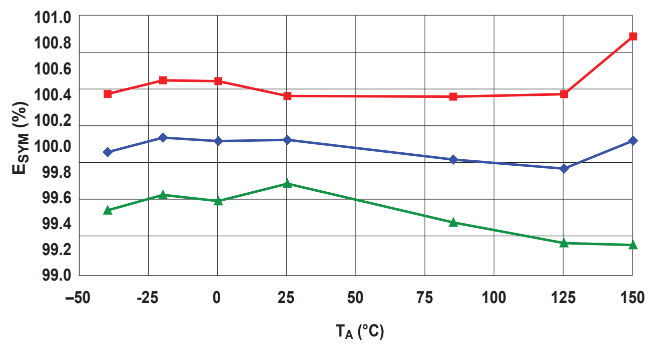
Sensitivity versus Ambient Temperature



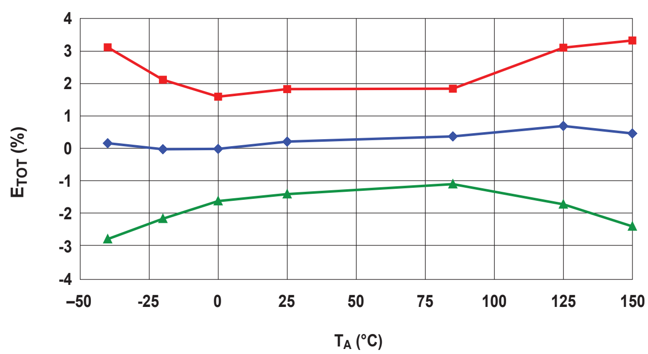
Nonlinearity versus Ambient Temperature

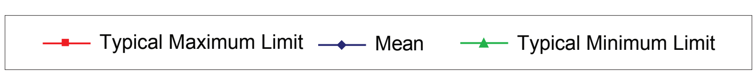


Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature





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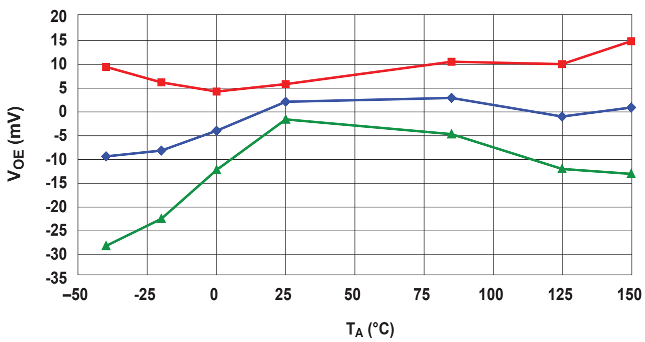
CHARACTERISTIC PERFORMANCE DATA

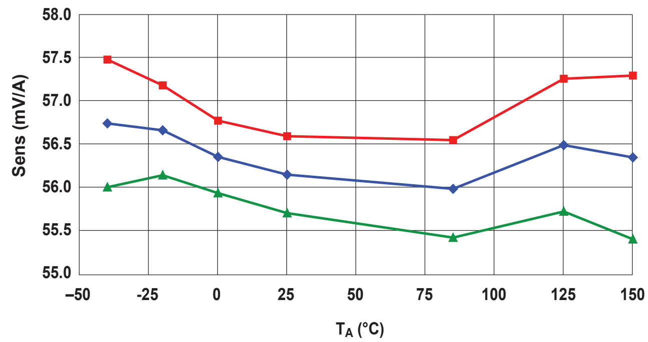
Data taken using the ACS709-20BB, V_{CC} = 5 V

Accuracy Data

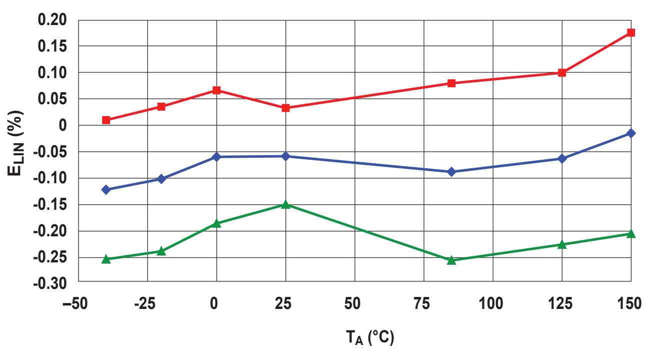
Electrical Offset Voltage versus Ambient Temperature



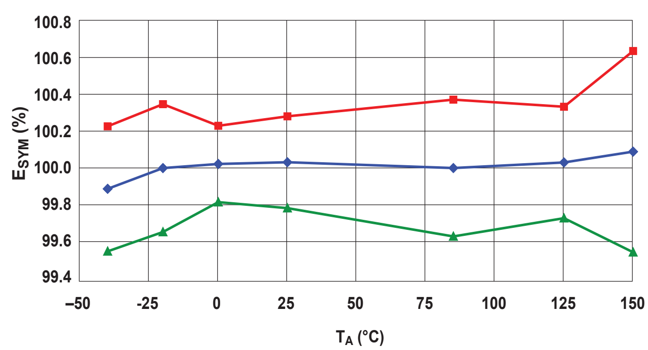
Sensitivity versus Ambient Temperature



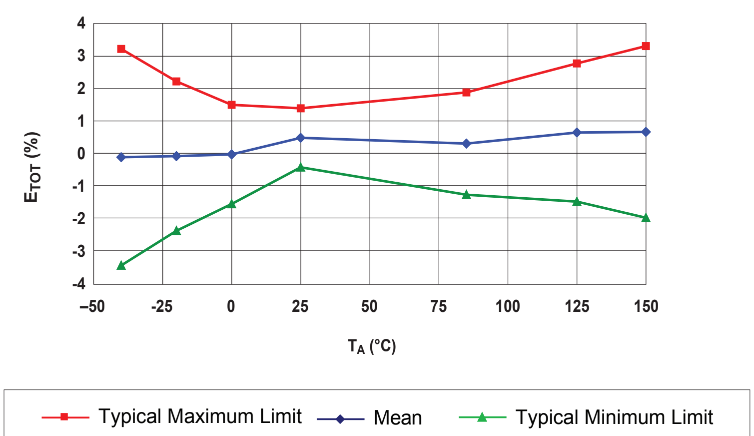
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



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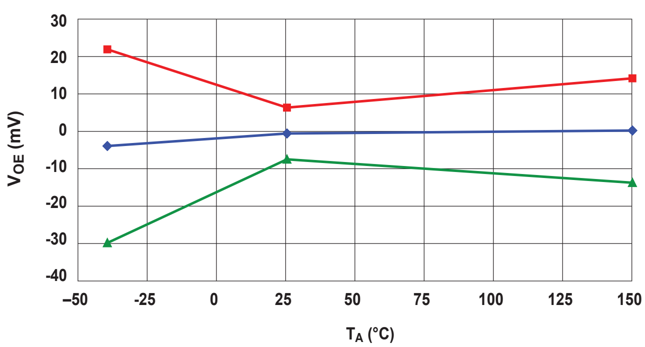
CHARACTERISTIC PERFORMANCE DATA

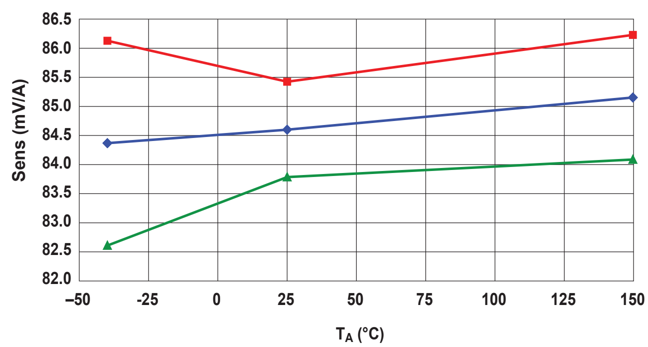
Data taken using the ACS709-10BB, V_{CC} = 5 V

Accuracy Data

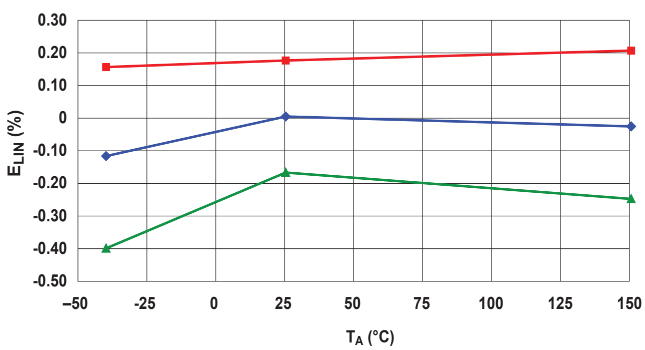
Electrical Offset Voltage versus Ambient Temperature



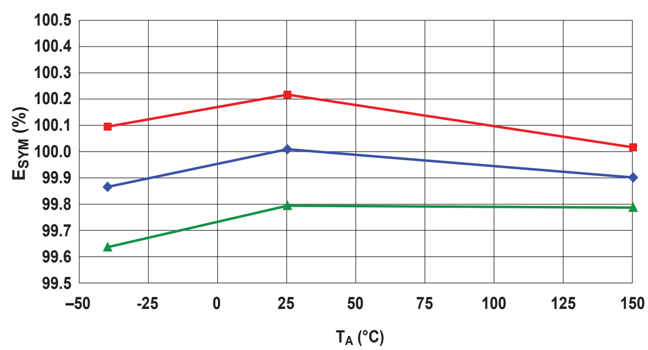
Sensitivity versus Ambient Temperature



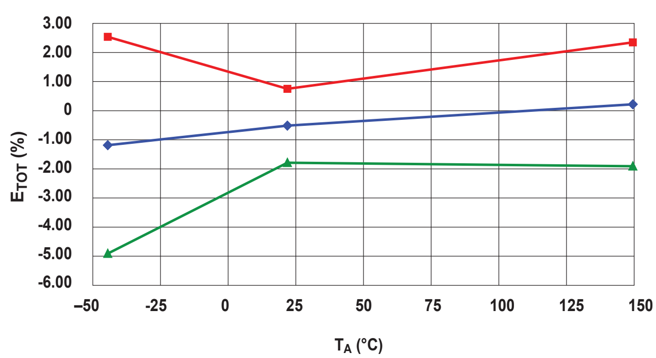
Nonlinearity versus Ambient Temperature



Symmetry versus Ambient Temperature



Total Output Error versus Ambient Temperature



Typical Maximum Limit — Mean — Typical Minimum Limit

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SETTING OVERCURRENT FAULT SWITCH POINT

Setting 20BB and 35BB Versions

The V_{OC} needed for setting the overcurrent fault switch point can be calculated as follows:

$$V_{OC} = \text{Sens} \times |I_{OC}| \ ,$$

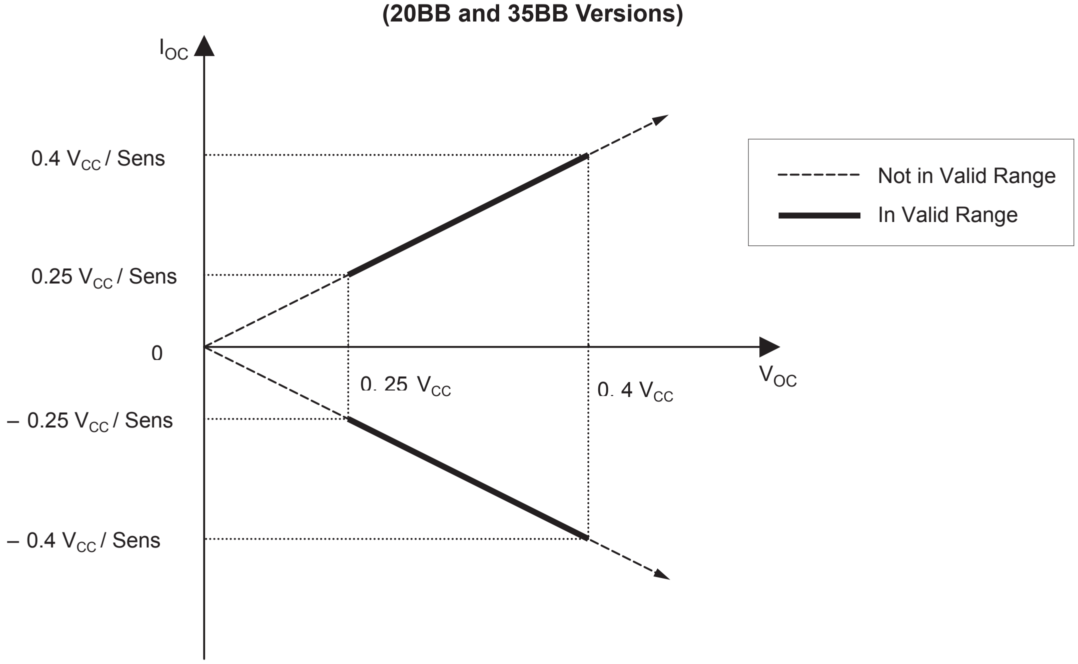
where V_{OC} is in mV, Sens is in mV/A, and I_{OC} (overcurrent fault switch point) is in A.

|Ioc | is the overcurrent fault switch point for a bi-directional (AC) current, which means a bidirectional device has two symmetrical overcurrent fault switch points, $+I_{OC}$ and $–I_{OC}$.

For I_{OC} and V_{OC} ranges, see the graph that follows.

I_{OC} versus V_{OC}

(20BB and 35BB Versions)



Example: For ACS709LLFTR-35BB-T, if required overcurrent fault switch point is 50 A, and V_{CC} = 5 V, then the required V_{OC} can be calculated as follows:

$$V_{OC} = \text{Sens} \times I_{OC} = 28 \times 50 = 1400 \text{ (mV)}$$

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Setting 10BB Versions

The V_{OC} needed for setting the overcurrent fault switch point can be calculated as follows:

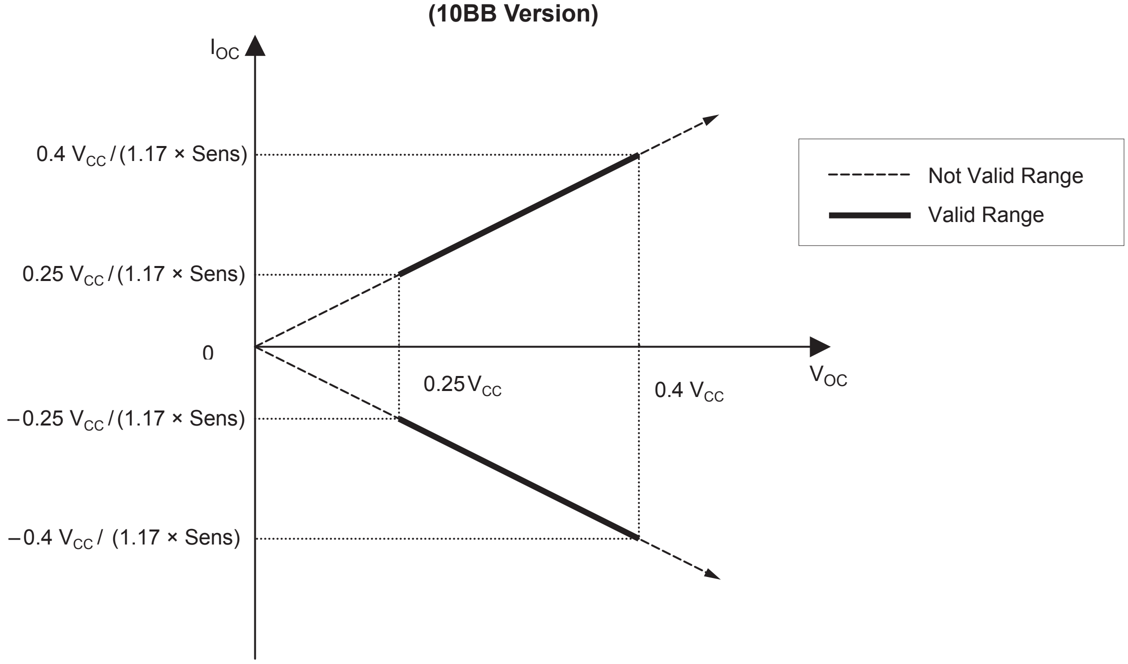
$$V_{OC} = 1.17 \times Sens \times |I_{OC}| \ ,$$

where V_{OC} is in mV, Sens is in mV/A, and I_{OC} (overcurrent fault switch point) is in A.

$|I_{oc}|$ is the overcurrent fault switch point for a bidirectional (AC) current, which means a bidirectional sensor has two symmetrical overcurrent fault switch points, $+I_{OC}$ and $-I_{OC}$.

For I_{OC} and V_{OC} ranges, see the graphs that follow.

I_{OC} versus V_{OC}
(10BB Version)



Example: For ACS709LLFTR-10BB-T, if required overcurrent fault switch point is 10 A and V_{CC} = 5 V, then the required V_{OC} can be calculated as follows:

$$V_{OC} = 1.17 \times Sens \times I_{OC} = 1.17 \times 85 \times 10 = 994.5 \text{ (mV)}$$

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FUNCTIONAL DESCRIPTION

Overcurrent Fault Operation

The primary concern with high-speed fault detection is that noise may cause false tripping. Various applications have or need to be able to ignore certain faults that are due to switching noise or other parasitic phenomena, which are application-dependant. The problem with simply trying to filter out this noise up front is that, in high-speed applications, with asymmetric noise, the act of filtering introduces an error into the measurement. To get around this issue and allow the user to prevent the fault signal from being latched by noise, a circuit was designed to slew the $\overline{\text{FAULT}}$ pin voltage based on the value of the capacitor from that pin to ground. Once the voltage on the pin reduces to less than 2 V, as established by an internal reference, the fault output is latched and pulled to ground quickly with an internal N-channel MOSFET.

Fault Walk-Through

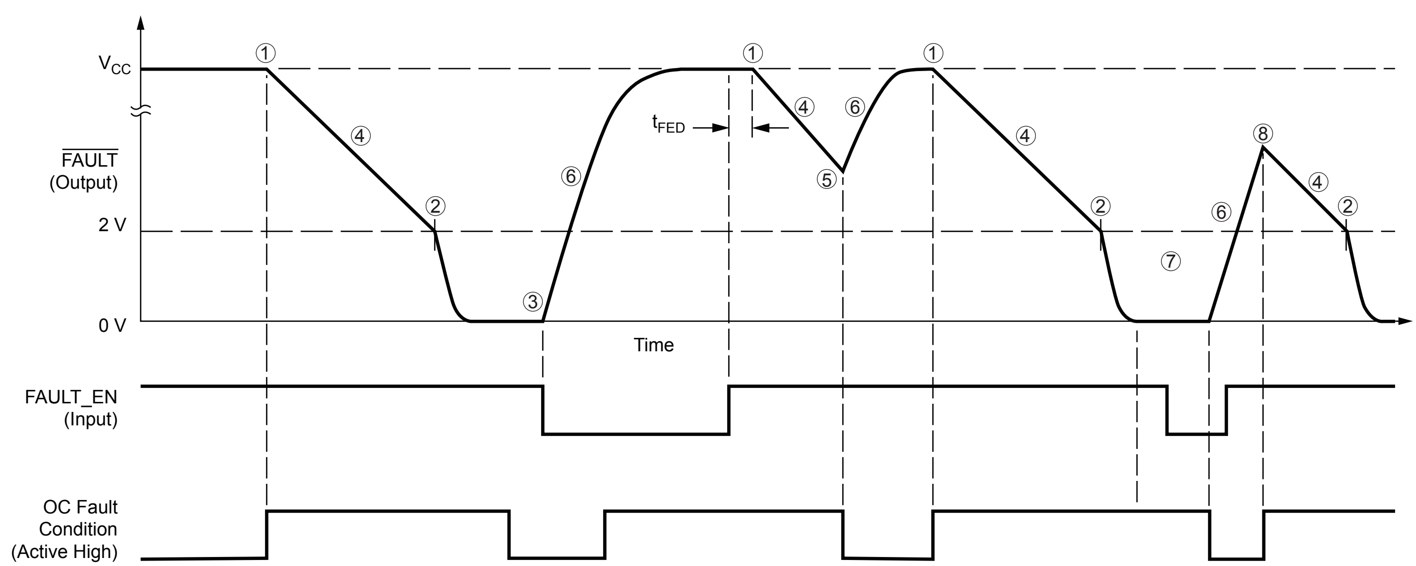
The following walk-through references various sections and attributes in the figure that follows. This figure shows different fault set/reset scenarios and how they relate to the voltages on the $\overline{\text{FAULT}}$ pin, FAULT_EN pin, and internal overcurrent (OC) fault node, which is invisible to the customer.

1. Because the device is enabled (FAULT_EN is high for a minimum period of time, the fault-enable delay, t_{FED}, 15 µs, typical) and there is an OC fault condition, the device $\overline{\text{FAULT}}$ pin starts to discharge.
2. When the $\overline{\text{FAULT}}$ pin voltage reaches approximately 2 V, the fault is latched, and an internal NMOS device pulls the $\overline{\text{FAULT}}$ pin voltage to approximately 0 V. The rate at which the $\overline{\text{FAULT}}$ pin slews downward (see [4] in the figure) is dependent on the external capacitor, C_{OC}, on the $\overline{\text{FAULT}}$ pin.
3. When the FAULT_EN pin is brought low, the $\overline{\text{FAULT}}$ pin starts to reset if an OC fault condition does not exist. The internal NMOS pull-down turns off and an internal PMOS pull-up turns on (if the OC fault condition persists, see [7]).
4. The slope, and thus the delay, on the fault is controlled by the capacitor, C_{OC}, placed on the $\overline{\text{FAULT}}$ pin to ground. During this portion of the fault (when the $\overline{\text{FAULT}}$ pin is between V_{CC} and 2 V), there is a 3 mA constant current sink, which discharges C_{OC}. The length of the fault delay, t, is equal to:

   Equation 1:

   $$t = \frac{C_{OC} \times (V_{CC} - 2\text{ V})}{3\text{ mA}}$$

   where V_{CC} is the device power supply voltage.
5. The $\overline{\text{FAULT}}$ pin does not reach the 2 V latch point before the OC fault condition cleared. Because of this, the fixed 3 mA current sink turns off, and the internal PMOS pull-up turns on to recharge C_{OC} through the $\overline{\text{FAULT}}$ pin.



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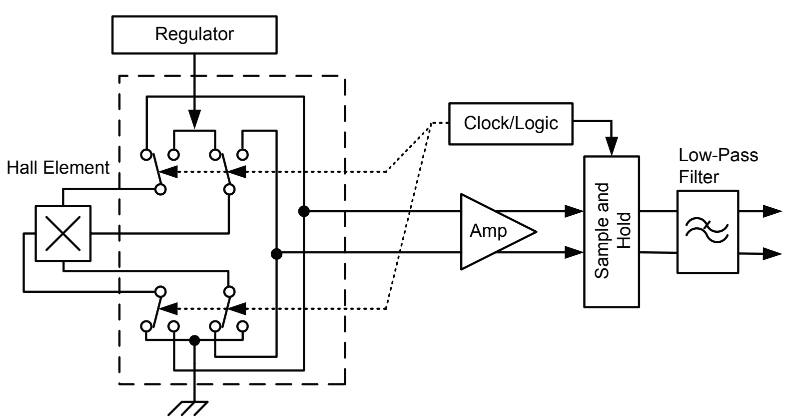
6. This curve shows V_{CC} charging external capacitor C_{OC} through the internal PMOS pull-up. The slope is determined by C_{OC}.
7. When the FAULT_EN pin is brought low, if the fault condition still exists, the latched $\overline{\text{FAULT}}$ pin remains low until the fault condition is removed; then, it starts to reset.
8. At this point there is a fault condition, and the part is enabled before the $\overline{\text{FAULT}}$ pin can charge to V_{CC}. This shortens the user-set delay; thus, the fault latches earlier. The new delay time can be calculated by Equation 1, after substituting the voltage observed on the $\overline{\text{FAULT}}$ pin for V_{CC}.

Chopper Stabilization Technique

Chopper stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. The Allegro-patented chopper stabilization technique used in the device nearly eliminates Hall IC output drift induced by temperature or package stress effects.

This offset-reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable electrical offset voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.



Concept of Chopper Stabilization Technique

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DEFINITIONS OF ACCURACY CHARACTERISTICS

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the full-scale current of the device.

Noise (V_{NOISE}). The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall-effect linear IC (≈1 G). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Linearity (E_{LIN}). The degree to which the voltage output from the device varies in direct proportion to the primary current through its full-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the full-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{V_{IOUT\_full\text{-}scale\ amperes}-V_{IOUT(Q)}}{2\left(V_{IOUT\_1/2\ full\text{-}scale\ amperes}-V_{IOUT(Q)}\right)}\right]\right\}$$

where $V_{IOUT\_full\text{-}scale\ amperes}$ is the output voltage (V) when the sensed current approximates full-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the device varies in proportion to either a positive or negative full-scale primary current. The following formula is used to derive symmetry:

$$100\left(\frac{V_{IOUT\_+\ full\text{-}scale\ amperes}-V_{IOUT(Q)}}{V_{IOUT(Q)}-V_{IOUT\_-full\text{-}scale\ amperes}}\right)$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $0.5 \times V_{CC}$. For example, in the case of a bidirectional output device, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent voltage due to nonmagnetic causes. To convert this voltage to amperes, divide by the device sensitivity, Sens.

Accuracy (E_{TOT}). The accuracy represents the maximum deviation of the actual output from its ideal value. This is also known as the total output error. The accuracy is illustrated graphically in the output voltage versus current chart that follows. Note that error is directly measured during final test at Allegro.

Accuracy is divided into four areas:

- **0 A at 25°C.** Accuracy of sensing zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy of sensing zero current flow including temperature effects.
- **Full-scale current at 25°C.** Accuracy of sensing the full-scale current at 25°C, without the effects of temperature.
- **Full-scale current over Δ temperature.** Accuracy of sensing full-scale current flow including temperature effects.

Ratiometry. The ratiometric feature means that its 0 A output, $V_{IOUT(Q)}$, (nominally equal to $V_{CC}/2$) and sensitivity, Sens, are proportional to its supply voltage, V_{CC}. The following formula is used to derive the ratiometric change in 0 A output voltage, $\Delta V_{IOUT(Q)RAT}$ (%):

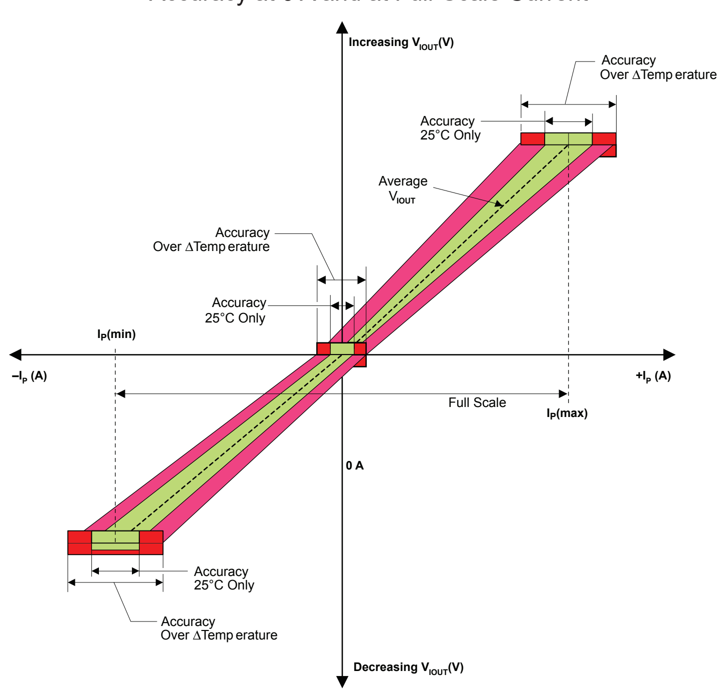
$$100\left(\frac{V_{IOUT(Q)VCC}\,/\,V_{IOUT(Q)5V}}{V_{CC}\,/\,5\text{ V}}\right)$$

The ratiometric change in sensitivity, $\Delta Sens_{RAT}$ (%), is defined as:

$$100\left(\frac{Sens_{VCC}\,/\,Sens_{5V}}{V_{CC}\,/\,5\text{ V}}\right)$$

Output Voltage versus Sensed Current

Accuracy at 0 A and at Full-Scale Current



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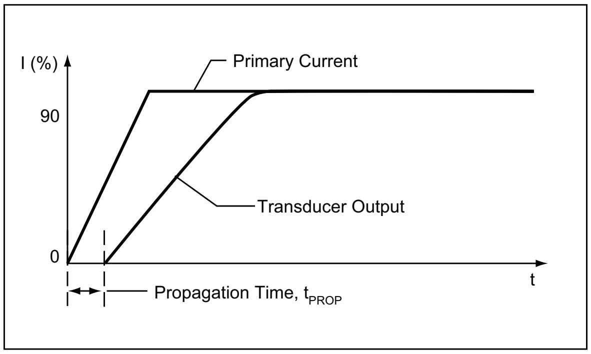
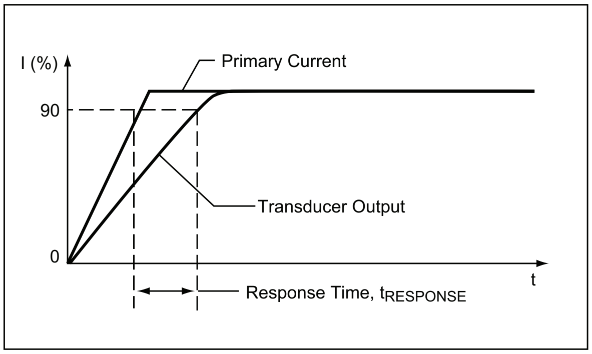
DEFINITIONS OF DYNAMIC RESPONSE CHARACTERISTICS

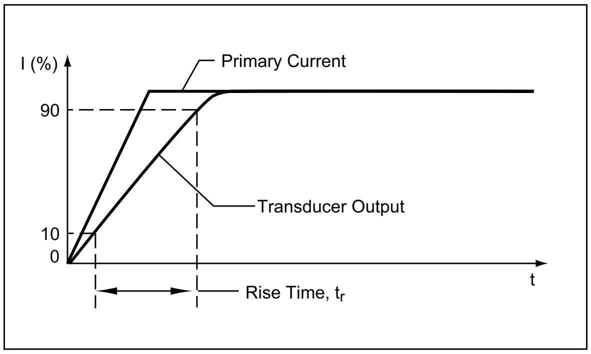
Propagation delay (t_{PROP}). The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



Response time ($t_{RESPONSE}$). The time interval between a) when the primary current signal reaches 90% of its final value, and b) when the device reaches 90% of its output corresponding to the applied current.



Rise time (t_r). The time interval between a) when the device reaches 10% of its full-scale value, and b) when the device reaches 90% of its full-scale value. The rise time to a step response is used to derive the bandwidth of the current sensor IC, in which $f(–3\text{ dB}) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.



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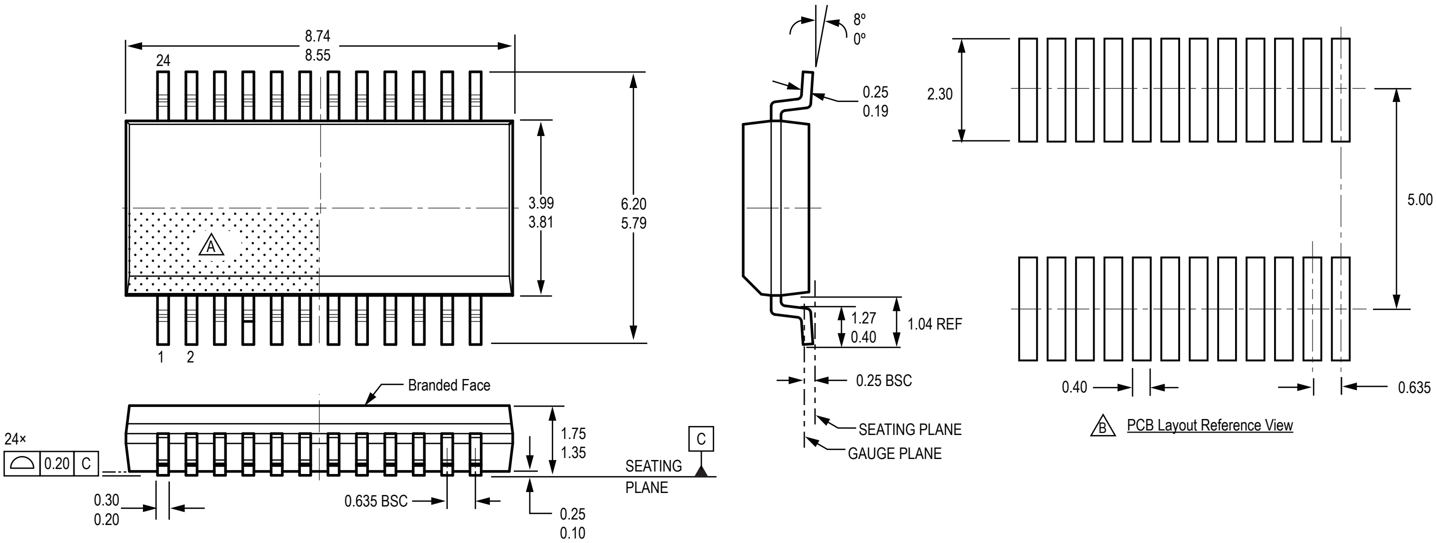
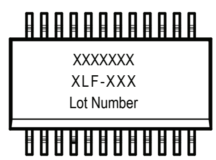
Package LF, 24-pin QSOP

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000387, Rev. 2 and JEDEC MO-137 AE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





C Standard Branding Reference View

Line 1 = 13 characters
Lines 2, 3 = 11 characters

Line 1: Part Number
Line 2: Temp, Pkg - Amps
Line 3: Assembly Lot Number

A Terminal #1 mark area

B Reference pad layout (reference IPC7351 SOP63P600X175-24M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

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REVISION HISTORY

Number	Date	Description
3	June 6, 2014	Added 10BB and 6BB parts
4	February 8, 2016	Updated Common Operating Characteristics and Supply Current in electrical characteristics table
5	June 5, 2017	Updated product status
6	February 5, 2019	Updated Dielectric Strength Test Voltage and minor editorial updates
7	January 30, 2020	Updated product status and minor editorial updates
8	February 7, 2022	Updated package drawing (page 20)
9	September 16, 2022	Added -S lead free part variants (page 2); added Certification Pending footnote to Isolation Characteristics Table (page 2); removed ACS709LLF-6BB-T variant (all pages); minor editorial edits
10	September 29, 2023	Updated part variants ACS709LLFTR-10BB-T and ACS709LLFTR-35BB-T status to Not for New Design
11	October 15, 2024	Removed -S part variants (page 2) and made minor editorial changes throughout, including minimization of capitalization, minimization of future tense, addition of links to cross-referenced sections, and removal of patent numbers.
12	March 11, 2025	Not for new design

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