# 12 V High-Side Hot-Swap Hall Effect Based Current Monitor IC

Features and Benefits

- Hall-effect current monitor—no external sense resistor required
- PGOOD and $\overline{\text{PGOOD}}$ indication
- Analog output voltage (factory trimmed for gain and offset) proportional to applied current
- External high-side FET gate drive
- 240V*A power fault protection with user-selectable delay
- Overcurrent fault protection with user-selectable delay
- Fault protection isolates failed supply from output in <2 µs
- 1.5 mΩ internal conductor resistance
- Active low latched Fault indicator output signal
- User controlled soft start / hot-swap function
- Logic enable input pin
- 10.8 to 13.2 V, single-supply operation
- 2 kV ESD protection for all pins

Package: 24 pin QSOP (suffix LF)
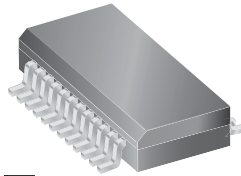
Approximate Scale

Description

The ACS761 combines Allegro™ Hall-effect current sense technology with a hot-swap controller resulting in a more efficient integrated controller for 12 V applications. By eliminating the need for a shunt resistor, the I^2R losses in the power path are reduced.

When the ACS761 is externally enabled, and the voltage rail is above the internal UVLO threshold, the internal charge pump drives the gate of the external FET. When the load voltage reaches its target value P_{GOOD} is asserted high. When a fault is detected, the gate is disabled while simultaneously alerting the application that a fault has occurred.

The integrated protection in the ACS761 incorporates three levels of fault protection, which includes a Power Fault with user-selectable delay, an Overcurrent Fault threshold with user-selectable delay, and Short Circuit protection, which disables the gate in less than 2 µs. These faults are indicated to the host system via the Fault pin and are cleared upon reasserting enable high.

Typical Application
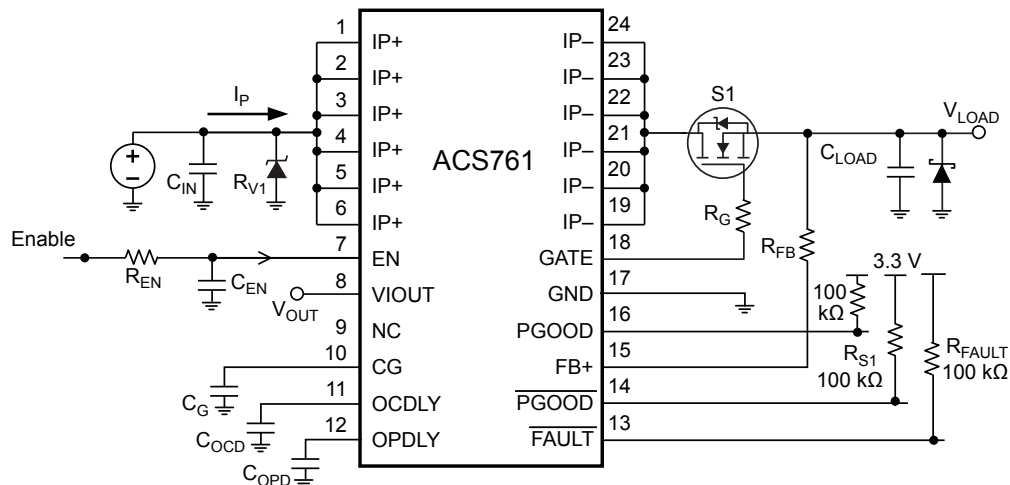
Selection Guide

Part Number	Package	Packing*
ACS761ELFTR-20B-T	QSOP24 surface mount	2500 pieces/reel

*Contact Allegro for additional packing options

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Voltage, IP*x* pins*	V_{CC}		24	V
GATE Drive Output Voltage*	V_{GATE}		32	V
FB+ Forward Voltage*	V_{FB+}		24	V
EN Forward Voltage*	V_{EN}		32	V
All Other Pins Forward Voltage	V_{IN}		8	V
Reverse DC Voltage, All Pins*	V_R		–0.5	V
Reverse Transient DC Voltage, All Pins*	V_r	VIOUT to GND	–5	V
Current Sense Output Current Source	$I_{VIOUT(Source)}$		1	mA
Current Sense Output Current Sink	$I_{VIOUT(Sink)}$	VCC to VIOUT	1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Maximum Junction Temperature	$T_J(max)$		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

* With respect to GND.

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Pin-out Diagram

```
IP+    1              24   IP–
IP+    2              23   IP–
IP+    3              22   IP–
IP+    4              21   IP–
IP+    5              20   IP–
IP+    6              19   IP–
EN     7              18   GATE
VIOUT  8              17   GND
NC     9              16   PGOOD
CG    10              15   FB+
OCDLY 11              14   PGOOD
OPDLY 12              13   FAULT
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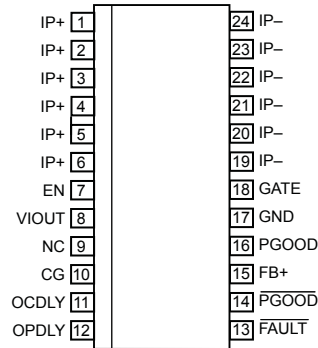
Terminal List Table

Number	Name	Function
1-6	IP+	Primary sampled current conduction path input; power input pins: connected to V_{CC}.
7	EN	Enable pin. The falling edge on the EN pin clears an overpower, overcurrent, or short circuit fault.
8	VIOUT	Analog output. Output voltage on this pin is proportional to the current flowing from the IP+ pins to the IP– pins.
9	NC	No connect. Connection to ground is recommended.
10	CG	Terminal for C_G capacitor. May be used to adjust the turn-on time and soft start control of an external MOSFET, S1. Voltage on this pin limits inrush current through MOSFET S1. Set via external capacitance, C_G, connected between this pin and GND. This capacitor is charged by an internal 20 µA current source.
11	OCDLY	Terminal for external capacitor, C_{OCD}, Used to adjust delay for overcurrent shutdown, set via the external capacitor, C_{OCD}, connected between this pin and GND.
12	OPDLY	Terminal for external capacitor, C_{OPD}, Used to adjust delay for overpower shutdown, set via the external capacitor, C_{OPD}, connected between this pin and GND.
13	$\overline{FAULT}$	Active low; output signal for device short circuit and overpower faults. Connect a pull-up resistor between this pin and the 3.3 V rail.
14	$\overline{PGOOD}$	Active low; output signal indicating load voltage has risen to the proper level.
15	FB+	Input of positive feedback on output voltage. Used to determine overpower fault threshold by difference between FB+ and GND pins.
16	PGOOD	Active high; output signal indicating load voltage has risen to the proper level.
17	GND	Terminal for ground connection.
18	GATE	Terminal for external MOSFET, S1. Provides output voltage to drive S1. Current through S1 is controlled at start-up by external capacitance connected between the CG pin and GND.
19-24	IP–	Primary sampled current conduction path output; power output pins.

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Functional Block Diagram

+12 V Load

S1

EN

CG

GATE

100 kΩ

Charge Pump

$\overline{\text{PGOOD}}$

FB+

Bias and V_{REG}

UVLO

Power Calculator

+

V_{REF}

−

PGOOD

OPDLY

Hall Current Drive

Dynamic Offset Cancellation

Signal Recovery

−

+

OCDLY

VIOUT

IP−

IP+

Zero Current Output Voltage Adjustment

Short Circuit Detection

+12 V$_{IN}$

OPDLY

OCDLY

PGOOD / Fault Logic

$\overline{\text{FAULT}}$

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OPERATING CHARACTERISTICS valid at V_{CC} = 12 V, T_A = 0°C to 85°C, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
General Electrical Characteristics						
Source Current	I_{SOURCE}	T_A = 25°C, VIOUT connected to GND	–	250	–	µA
Linear Sensing Range	I_P	Current flows from IP+ to IP- pins	0	–	55	A
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	1.5	–	mΩ
Supply Voltage	V_{CC}	Voltage applied to IP+ pins	10.8	12	13.2	V
Supply Current	I_{CC}		–	8	10.5	mA
Undervoltage Lockout (UVLO)	V_{UVLOH}	V_{CC} rising and CG pin current source turns on, EN pin = high	–	–	10.5	V
	V_{UVLOL}	V_{CC} falling and CG pin current source turns off, EN pin = high	7.0	–	–	V
UVLO Delay to Chip Enable/ Disable	t_{UVLOE}	Enabling, measured from rising V_{CC} > V_{UVLOH} to V_{GATE} > 1 V, EN pin = high	–	700	1100	µs
	t_{UVLOD}	Disabling, measured from falling V_{CC} < V_{UVLOL} to V_{GATE} < 1 V, EN pin = high	–	1	2.5	µs
FB+ Input Resistance	R_{FB}	T_A = 25°C	–	240	–	kΩ
Current Sense Performance Characteristics						
VIOUT Analog Output Propagation Time	t_{PROP}	T_A = 25°C, I_P = 0 →20 A, capacitance from VIOUT to GND = 100 pF	–	2	–	µs
VIOUT Analog Output 10-90% Rise Time	t_r	T_A = 25°C, I_P = 0 →20 A, capacitance from VIOUT to GND = 100 pF	–	5	–	µs
VIOUT Load Capacitance	C_{LOAD}		–	–	1	nF
VIOUT Load Resistance	R_{LOAD}		20	–	–	kΩ
VIOUT Analog Signal Bandwidth[1]	f_{3dB}	–3 dB, Ip = 10 A peak-to-peak, T_A = 25°C, no external device filter, capacitance from VIOUT to GND = 100 pF	–	50	–	kHz
VIOUT Analog Signal Sensitivity	Sens	T_A = 25°C	–	65	–	mV/A
		Over full ambient operating temperature range	63	–	69	mV/A
Sensitivity Slope Over Temperature	$\Delta Sens_{TA}$	T_A = 0°C to 25°C	–	0.042	–	mV/A/°C
		T_A = 25°C to 85°C	–	0.027	–	mV/A/°C
VIOUT Analog Noise Level[2]	$V_{NOISE(PP)}$	Mean peak-to-peak, T_A = 25°C, 50 kHz external device filter	–	20	–	mV
VIOUT Analog Nonlinearity	E_{LIN}	Over full ambient operating temperature range and linear sensing range	–	±0.5	±1	%
Zero Current Output Voltage	$V_{IOUT(Q)}$	T_A = 0°C to 85°C	0.18	0.2	0.22	V
Zero Current Output Slope Over Temperature	$\Delta I_{OUT(Q)TA}$	T_A = 0°C to 25°C	–	–0.148	–	mV/°C
		T_A = 25°C to 85°C	–	–0.057	–	mV/°C
Output Voltage Saturation[3]	V_{OL}	T_A = 25°C	–	0.15	–	V
	V_{OH}	T_A = 25°C	–	3.71	–	V
VIOUT Total Error % of I_P	E_{TOT}	T_A = 25°C, I_P = 20 A	–	<±1.0	–	%
		T_A = 0°C to 85°C, I_P = 20 A	–4	–	4	%

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OPERATING CHARACTERISTICS (continued) valid at V_{CC} = 12 V, T_A = 0°C to 85°C, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operational Supply Indicator Performance Characteristics						
PGOOD Output Voltage	$V_{PGOODOL}$	I_{PGOOD} = 3 mA sink current	–	–	0.4	V
PGOOD Output Leakage Current	$I_{PGOODOH}$	V_{PGOOD} = 3.3 V	–	–	1	µA
PGOOD Activation Threshold	$V_{PGOODHIGH}$	T_A = 25°C; FB+ = 0 V → 12 V	–	10.2	10.8	V
PGOOD Deactivation Threshold	$V_{PGOODLOW}$	T_A = 25°C; FB+ = 12 V → 0 V	9.6	9.8	–	V
$\overline{\text{PGOOD}}$ Output Voltage	$V_{\overline{PGOOD}OL}$	$I_{\overline{PGOOD}}$ = 3 mA sink current	–	–	0.4	V
$\overline{\text{PGOOD}}$ Output Leakage Current	$I_{\overline{PGOOD}OH}$	$V_{\overline{PGOOD}}$ = 3.3 V	–	–	1	µA
$\overline{\text{PGOOD}}$ Deactivation Threshold	$V_{\overline{PGOOD}HIGH}$	T_A = 25°C; FB+ = 0 V → 12 V	–	10.2	10.8	V
$\overline{\text{PGOOD}}$ Activation Threshold	$V_{\overline{PGOOD}LOW}$	T_A = 25°C; FB+ = 12 V → 0 V	9.6	9.8	–	V
Current Fault Performance Characteristics						
Overpower Fault Threshold	$P_{F(th)}$	T_A = 0°C to 85°C	221	230	238	W
Overpower Fault Signal Delay[4]	t_{PFL}	T_A = 25°C, measured from $\overline{\text{FAULT}}$ signal to V_{GATE} < 1 V, OPDLY pin open, load step from 17 to 23 A in 100 ns	–	11	18	µs
Internal –3 dB Filter Frequency for FB+ Pin	f_{FBFILT}	T_A = 25°C	–	50	–	kHz
Overcurrent Fault Signal Delay[4]	t_{CFL}	Measured from $\overline{\text{FAULT}}$ signal to V_{GATE} < 1 V, OCDLY pin open, OPDLY = 0 V, load step from 17 to 55 A in 1 µs	–	8	12	µs
Device IP Short Circuit Fault Threshold[5]	I_{PF}		60	130	160	A
Device IP Overcurrent Fault Threshold	I_{OC}	T_A = 0°C to 85°C	35	40	45	A
Short Circuit/Overcurrent Fault Gate Delay	t_{SC}	Measured from $\overline{\text{FAULT}}$ signal to V_{GATE} < 1 V, includes t_{GF}	–	2	3	µs
Fault Related Signal Characteristics						
Internal Pull Down Resistance Between EN and GND	R_{EN}	T_A = 25°C	–	100	–	kΩ
EN Voltage Threshold[6]	V_{ENH}	IC enabled when V_{EN} > V_{ENH}	2	–	–	V
	V_{ENL}	IC disabled when V_{EN} < V_{ENL}	–	–	0.55	V
Enable Signal Duration	t_{EN}	C_X in µF, where Cx is the largest capacitance among: C_G, C_{OCD}, and C_{OPD}	8 × C_X	–	–	ms
FAULT Output Voltage	$V_{FAULTOL}$	I_{FAULT} = 3 mA sink current	–	–	0.4	V
FAULT Output Leakage Current	$I_{FAULTIH}$	V_{FAULT} = 3.3 V	–	–	1	µA

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OPERATING CHARACTERISTICS (continued) valid at V_{CC} = 12 V, T_A = 0°C to 85°C, unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Gate Drive Performance Characteristics						
Nominal Gate Voltage	V_{GATE}	T_A = 25°C	–	V_{CC} + 10	–	V
Gate Voltage Tolerance	ΔV_{GATE}	T_A = 25°C	–	–	±2	V
Average GATE Drive Current	I_{GD}	V_{CC} = 12 V, T_A = 25°C	30	50	70	µA
Charge Pump Switching Frequency	f_{CP}	T_A = 25°C	–	1	–	MHz
GATE Rise Time	t_{GR}	T_A = 25°C, external MOSFET S1 gate capacitance = 5.8 nF, measured from V_{GATE} = 0 to 15 V, CG pin open, no output load capacitance	–	1	–	ms
GATE Sink Resistance[7]	R_{Gsink}	< 5 µs after gate voltage falls low	–	20	30	Ω
GATE Sink Steady State Resistance[7]	$R_{Gsink(ss)}$	> 80 µs after gate voltage falls low	–	100	–	kΩ
GATE Shutdown Delay	t_{GSD}	Measured from fault event to start of GATE pull down	–	200	–	ns
GATE Maximum Fall Time	t_{GF}	Measured from V_{GATE} = 90% of maximum to V_{GATE} < 1 V, while EN pin switched from high to low, assuming external MOSFET S1 gate capacitance = 5.8 nF	–	800	–	ns
CG Output Current	I_{SLEW}	T_A = 25°C	18	20	22	µA

[1] The small signal, ac bandwidth of this device is approximately 90 kHz.

[2] This is the 6 σ noise voltage.

[3] This test requires currents sufficient to swing the output driver between the fully off state and the saturated state. Assumes that the VIOUT pin is connected to an analog-to-digital converter that saturates at 2.5 V. The VIOUT signal is linear above 2.5 V, however, this test is NOT intended to indicate a range of linear operation.

[4] This is the minimum delay time achievable without C_{OPD} or C_{OCD}. Longer delay time can be achieved by using C_{OPD} or C_{OCD}. See Functional Description section for details. Voltage trip point for both the OPDLY and the OCDLY pins is 3.85 V.

[5] This parameter is internally programmed and cannot be controlled by the end user.

[6] The FAULT output signal is latched. After a latched fault event, the device will be reset only when either: (a) V_{EN} drops below V_{ENL}, or (b) the power to the device (applied to the IP+ pins) is toggled off and then back on.

[7] The gate resistance switches to high impedance approximately 15 to 45 µs after the gate voltage falls low after a fault.

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Functional Description

Soft Start and Fault Characteristics

Gate turn on rise time, t_{GR}. Set by external capacitance, C_G, on the CG pin, such that $C_G = 7.5 \times t_{GR}$, where C_G is in µF and t_{GR} is rise time in seconds. For example, a 3.9 µF capacitor connected from the CG pin to GND (without an output load) will yield a rise time of approximately 500 ms: $C_G \cong 7.5 \times 0.5$ s $= 3.75$ µF, $\cong 3.9$ µF (a common capacitor value). When the CG pin is kept open, the ACS761 has a minimum t_{GR} of 1 ms typical.

It is important to select values for CG and the FET load resistance ($R_{LOADFET}$) that ensure safe power consumption during FET activation. The combination of a large FET current consumption caused by $R_{LOADFET}$, and a long gate voltage slew caused by CG, could cause the overall FET power consumption to be outside of its safe operating area during FET activation.

I_{PF} fault signal delay, t_{IPF}. This is the delay from high current level fault sense to the start of turn-off of the external MOSFET S1 turn-off. Set by external capacitance, C_{OCD}, on the OCDLY pin, such that $C_{OCD} = 5.17 \times t_{rOCD}$; where C_{OCD} is in µF and t_{rOCD} is rise time in seconds. When the OCDLY pin is kept open, the IC has a minimum fault delay, $t_{IPFLmax}$, of 8 µs maximum.

Load power fault signal delay, t_{PFL}. This is the delay from maximum power level fault, $P_{F(th)}$, sense to the start of external MOSFET S1 turn-off. Set by external capacitance, C_{OPD}, on the OPDLY pin, such that $C_{OPD} = 5.17 \times t_{rOPD}$; where C_{OPD} is in µF and t_{rOPD} is rise time in seconds. The IC has a minimum fault delay when the OPDLY pin kept open of 10 µs typical.

Accuracy Characteristics

Sensitivity, Sens. The change in device output in response to a 1 A change through the primary conductor. Sens is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is trimmed at Allegro final test to optimize the sensitivity (mV/A) for the full-scale current range of the device.

Noise, $V_{NOISE(PP)}$. The product of the linear IC amplifier gain (mV/G) and the noise floor for the Allegro Hall effect linear IC. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Nonlinearity, E_{LIN}. The linearity of the V_{IOUT} signal is the degree to which the voltage output from the device varies in direct proportion to the primary sampled current, up to 20 A. Nonlinearity reveals the maximum deviation in the slope of the device transfer function compared to the slope of the ideal transfer curve for this transducer. The following equation is used to derive the linearity:

$$100 \left\{ 1- \left[\frac{(V_{IOUT\_full\text{-}scale\ amperes} - V_{IOUT(Q)})}{2\,(V_{IOUT\_half\text{-}scale\ amperes} - V_{IOUT(Q)})} \right] \right\} ,$$

where full-scale current is 20 A, and half-scale current is 10 A.

Zero Current Output Voltage, $V_{IOUT(Q)}$. The output of the device when the primary current, I_P, is 0 A. Variation in $V_{IOUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim and thermal drift.

V_{IOUT} Total Error, E_{TOT}. The maximum percentage deviation of the actual output from its ideal value, based on an ideal sensitivity of 65 mV/A over the operating ambient temperature range.

PGood Indication. The PGood indication is active high when valid power is applied to the device. PGood activates approximately 500 ms after the FB+ voltage reaches its $V_{PGOODON}$ threshold. PGood will not release until 500 ms after the FB+ voltage drops below its $V_{PGOODOFF}$ threshold.

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Overpower Fault Operation

The timing diagram in figure 1 shows characteristic operation of the ACS761 when the power consumed from the 12 V system bus exceeds Overpower Fault Threshold, $P_{F(th)}$. The system power supply bus reaches the nominal steady state level of 12 V before the EN pin (Enable pin, active high) of the ACS761 transitions to the high state at time t_{EN1}. Note that, when the EN pin is in the low state, the GATE pin is actively pulled low. However, as shown in the timing diagram, the voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state. The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin. At a certain GATE voltage, current begins to flow through the external protection MOSFET, S1, and this current increases as the GATE voltage increases. The voltage at the VIOUT pin, which is the current device output voltage of the ACS761, proportionally tracks the current that flows through the MOSFET.

In the timing diagram, the system is in normal, steady state operation up until the time t_{INIT_F}. At t_{INIT_F}, the current load on the 12 V power supply increases from 19.2 to 22 A and the ACS761 internally registers an overpower fault condition. At this time, the voltage on the OPDLY pin increases with a constant slope. (This slope is controlled by the value of the capacitor connected to the OPDLY pin). This voltage continues to increase with a constant slope until either:

• The OPDLY pin voltage reaches a threshold of 3.85 V (if this occurs, the $\overline{FAULT}$ signal is latched in the low state), or

• The power consumption of the system falls below $P_{F(th)}$ (at which time the OPDLY pin voltage is pulled to ground)

An overpower fault event is detected at t_{OP_F}. At this time, the $\overline{FAULT}$ signal transitions to the low state and the GATE pin is pulled to ground. The $\overline{FAULT}$ signal is latched and the chip will pull down the GATE voltage until the EN pin of the
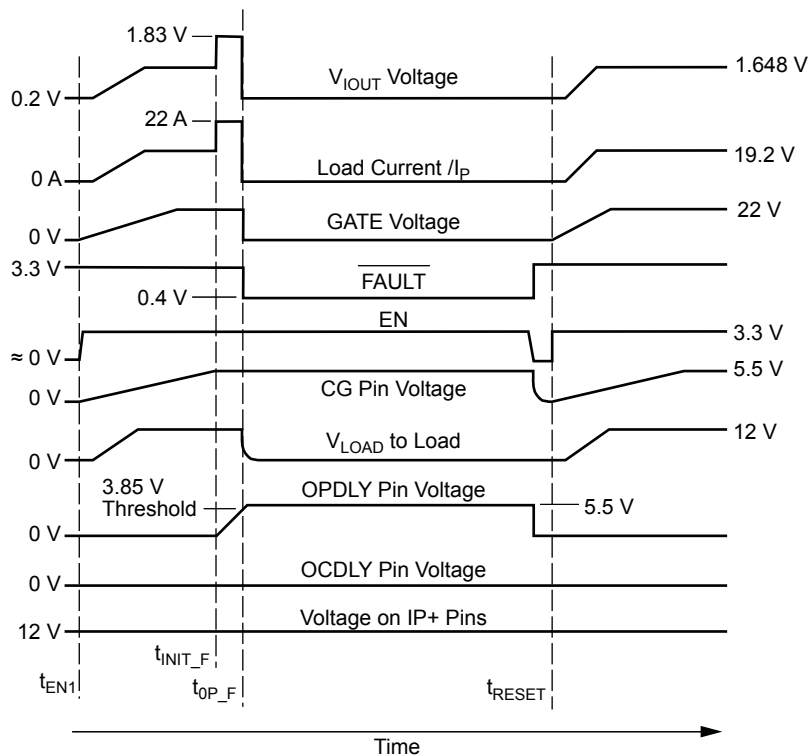

Figure 1. Timing Diagram for Overpower Fault

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ACS761 transitions to the low state and then back to the high state. As shown in the timing diagram, certain ACS761 signals (the $\overline{FAULT}$ signal and the OPDLY pin voltage) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation (soft start and fault monitoring) when the EN signal transitions back to the high state.

Soft Short Circuit Fault Operation

The timing diagram in figure 2 shows the characteristic operation of the ACS761 when the current load on the 12 V system bus jumps from the 19-to-20 A level to the 40 A level. The 40 A load is typically indicative of a soft short circuit on the I_{LOAD} side of the external MOSFET. In figure 2, the system power supply bus reaches the nominal steady state level of 12 V before the EN pin (Enable pin, active high) of the ACS761 transitions to the high state at time t_{EN1}. Note that when the EN pin is in the low state, the GATE pin is actively pulled low. However, as shown in the timing diagram, the voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state.

The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin.

At a certain GATE voltage, current begins to flow through the external protection MOSFET, S1, and this current increases as the GATE voltage increases. The voltage at the VIOUT pin, which is the current device output voltage of the ACS761, proportionally tracks the current that flows through the MOSFET. In the figure 2, the system is in normal, steady state operation up until the time t_{INIT_F}. At t_{INIT_F} the current load on the 12 V power supply increases from 19.2 A to 40 A , reached at t_{40A_F} at which the ACS761 internally registers both an overpower fault and an overcurrent fault. At t_{INIT_F}, the voltage on the OPDLY and OCDLY pins increases with a constant slope. The slope of the voltage on the two delay pins is controlled by the value of the capacitor connected to each pin. In this case the capacitor on the OCDLY pin is smaller than the capacitor on the OPDLY pin and the voltage on the OCDLY pin ramps much faster than the voltage on the OPDLY pin (both pins are connected to separate 20 µA current
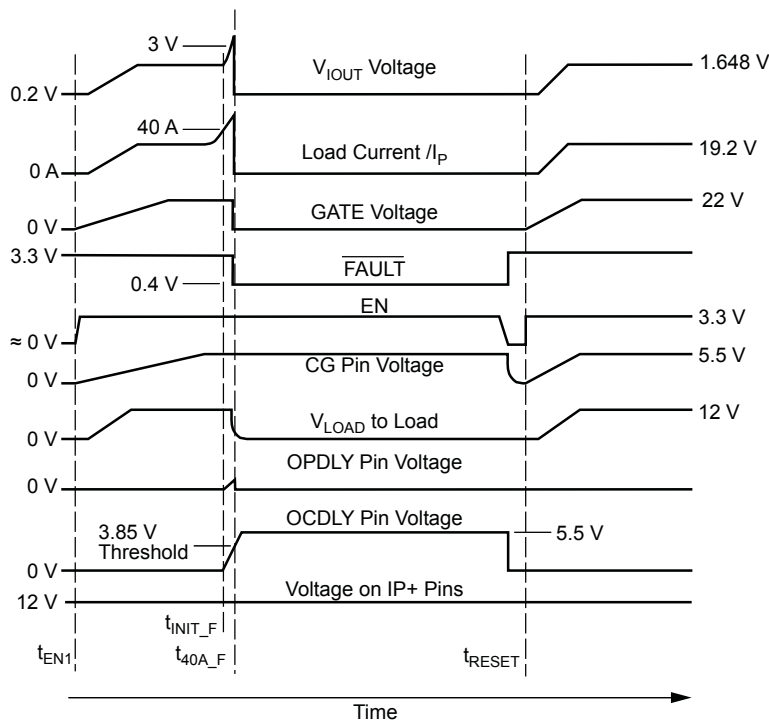

Figure 2. Timing Diagram for 30 to 40 A Load Fault

sources). The voltages on each delay pin continues to increase with a constant slope until:

• either the OPDLY or the OCDLY pin voltage reaches a threshold of 3.85 V (if this occurs, the $\overline{FAULT}$ signal is latched in the low state), or

• the current load of the system falls below 20 A for the OPDLY pin and 40 A for the OCDLY pin.

In figure 2 a short circuit fault event is detected at t_{40A_F}. At this time, the $\overline{FAULT}$ signal transitions to the low state and the GATE pin is pulled to ground. The $\overline{FAULT}$ state is latched and the chip will pull down the GATE voltage until the EN pin of the ACS761 transitions to the low state and then back to the high state. As shown in the timing diagram, certain ACS761 signals (the $\overline{FAULT}$ signal and the OCDLY pin voltage) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation (soft start and fault monitoring) when the EN signal transitions back to the high state.

Hard Short Circuit Fault Operation

The timing diagram in figure 3 specifically shows characteristic operation of the ACS761 when the device is powered on (via the EN pin) and a 50 mΩ short circuit is present from load side of the external MOSFET, S1, to ground. In figure 3 the system power supply bus reaches the nominal steady state level of 12 V before the EN pin of the ACS761 transitions to the high state at time t_{EN1}. The voltage on the GATE pin increases with a positive slope after the EN pin transitions to the high state. The ramp rate of the GATE pin is controlled by the value of the capacitor connected to the CG pin. In the example shown below a small capacitor is connected to the CG pin and the pin ramps to 5.5 V in < 10 µs.

In panel A of figure 3, the device is enabled into a 50 mΩ short circuit. Therefore, as the GATE voltage increases the current through the external MOSFET increases at a rapid rate. In this example, it is assumed that there is no capacitor on the OCDLY pin. When the current through the MOSFET exceeds
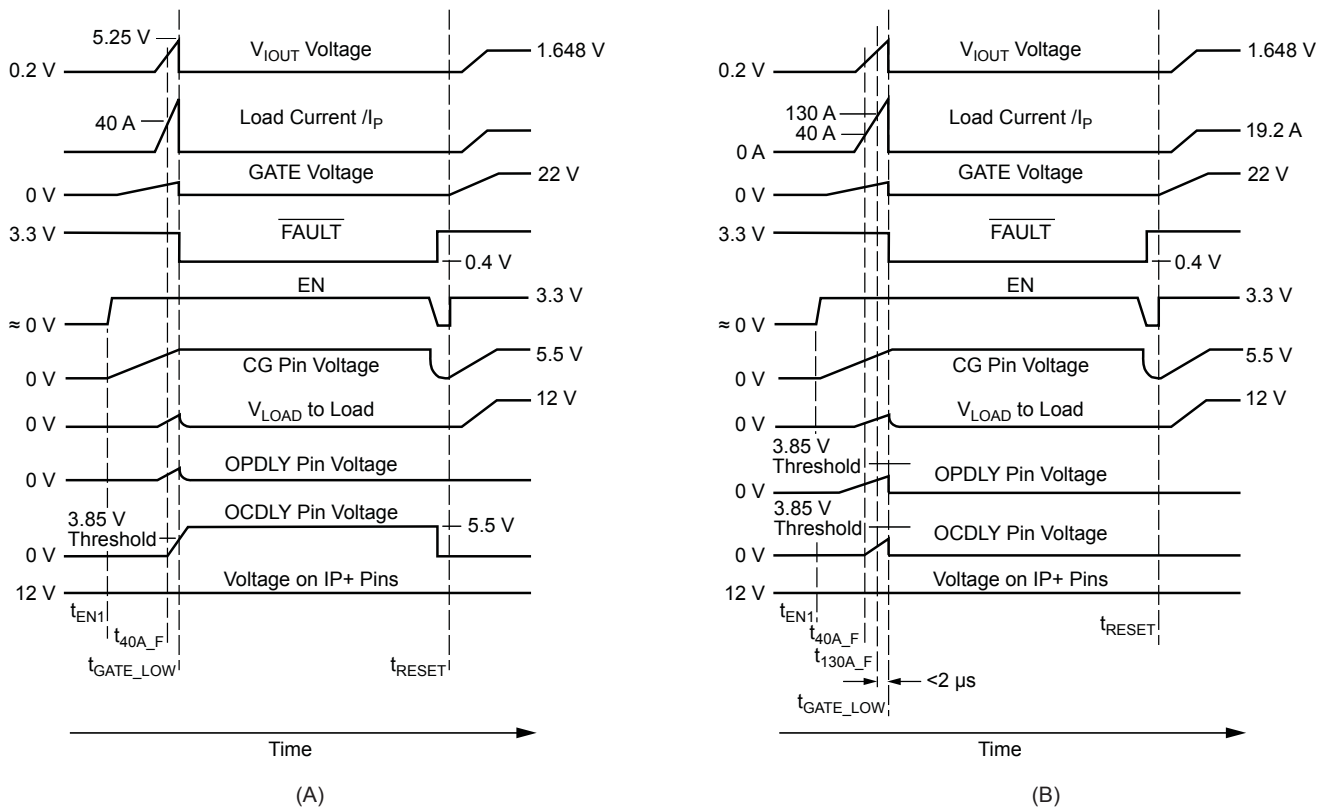

Figure 3. (A) Timing Diagram for a 50 mΩ Short Circuit from V_{LOAD} to GND; (B) Timing Diagram for a 50 mΩ Short Circuit from V_{LOAD} to GND, capacitor C_{OCD} with high rating connected.

the overcurrent threshold, the voltage on the OCDLY pin rises quickly beginning at t_{40A_F}. As the voltage on the OCDLY pin rises, so does the voltage on the CG pin and the current through the external MOSFET. If there is no capacitor on the OCDLY pin, and if the ACS761 Short Circuit Fault Threshold, I_{SC}, is greater than 100 A, then the OCDLY pin will reach the 3.85 V threshold before the current through the external MOSFET exceeds I_{SC}. This is the case depicted in the panel A. The fault event is detected at t_{GATE_LOW}. At this time. the $\overline{FAULT}$ signal transitions to the low state and the GATE pin is pulled to ground.

In the event that a large capacitor is connected to the OCDLY pin, the ACS761 will not pull down the gate of the external MOSFET until the current flowing through the MOSFET exceeds I_{SC} (shown in panel B, under the assumption that I_{SC} equals 130 A). The device pulls down the MOSFET GATE approximately 2 µs after the load current exceeds this threshold. In this case, a significant current (> 40 A but < 130 A) may flow through the

MOSFET for tens of microseconds before the Short Circuit Fault Threshold trips.

When tripped, the $\overline{FAULT}$ signal is latched and the chip will pull down the GATE voltage until the EN pin of the ACS761 transitions to the low state and then back to the high state. Certain ACS761 signals (soft start and fault monitoring related) are reset when the EN pin transitions to the low state. These signals are reset in order to guarantee normal device operation when the EN signal transitions to the high state.

Determining the Root Cause of an ACS761 Fault Event

The Fault Condition Truth Table provides system debugging information in the event of a fault event during use of the ACS761. Note that for all of the fault conditions listed, it is possible to monitor the voltages of various ACS761 output pins and determine the cause of the ACS761 $\overline{FAULT}$ event.
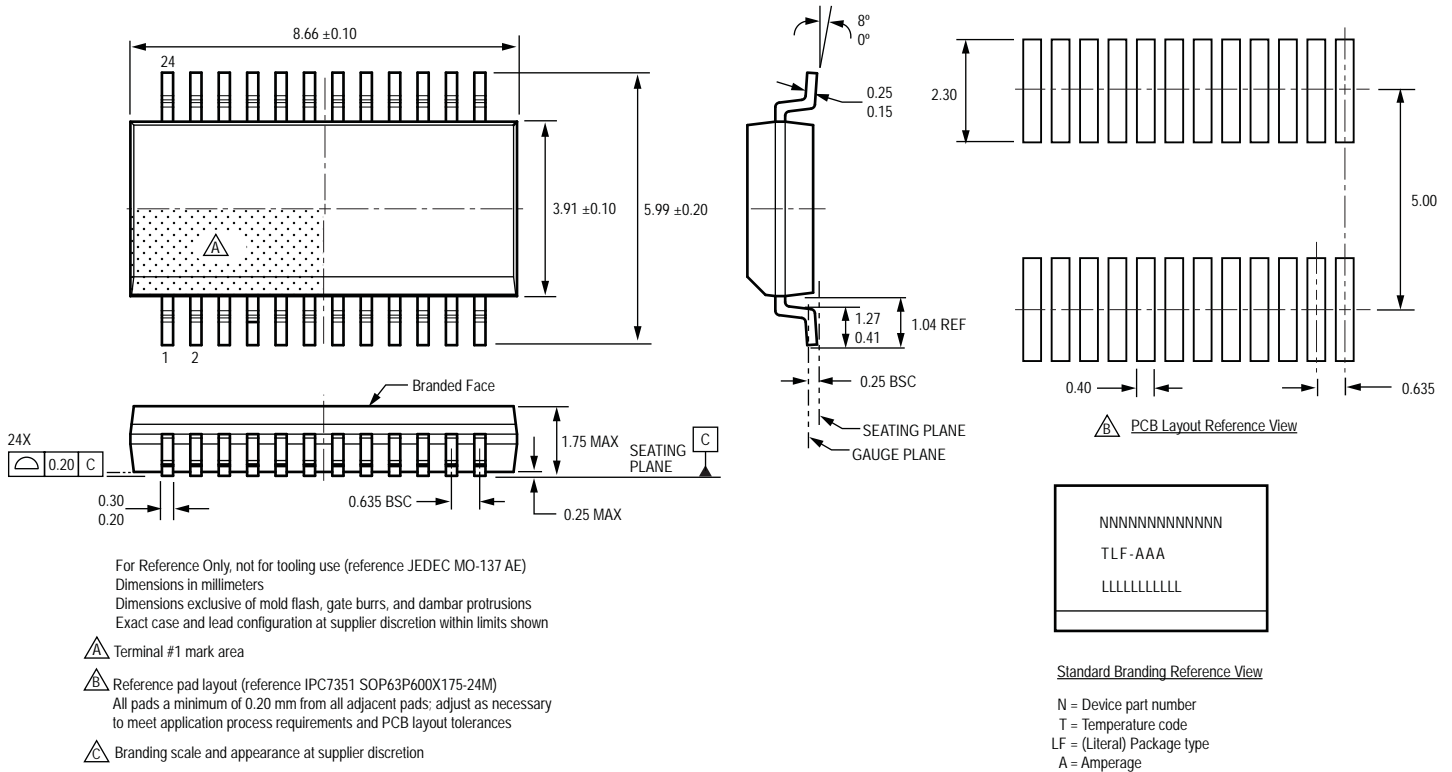
Fault Condition Truth Table

Pin Logic State				Probable Root Cause
EN Pin	**$\overline{FAULT}$ Pin**	**OPDLY Pin**	**OCDLY Pin**	
High	Low	High	Low	Device Overpower Fault Threshold, $P_{F(th)}$, exceeded
High	Low	Low	High	Device IP Overcurrent Fault Threshold, I_{OC}, exceeded
High	Low	Low	Low	Device IP Short Circuit Fault Threshold, I_{PF}, exceeded

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Application Information

Current Mode Operation
The ACS761 can be set to ignore a Power Mode fault condition to operate in pure Current Mode. This can be done by grounding the OPDLY pin to disable the overpower fault condition.

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Package LF, 24-pin QSOP

8.66 ±0.10

24

3.91 ±0.10

5.99 ±0.20

1   2

8°
0°

0.25
0.15

2.30

1.27
0.41

1.04 REF

0.25 BSC

5.00

0.40

0.635

SEATING PLANE
GAUGE PLANE

B   PCB Layout Reference View

Branded Face

24X

0.20   C

1.75 MAX

SEATING
PLANE

C

0.30
0.20

0.635 BSC

0.25 MAX

C

For Reference Only, not for tooling use (reference JEDEC MO-137 AE)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC7351 SOP63P600X175-24M)
    All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
    to meet application process requirements and PCB layout tolerances

C Branding scale and appearance at supplier discretion

NNNNNNNNNNNNNN

TLF-AAA

LLLLLLLLLLLL

Standard Branding Reference View

N = Device part number
 T = Temperature code
LF = (Literal) Package type
 A = Amperage

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