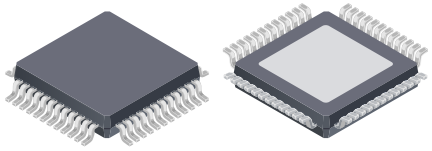
80 V Automotive Three-Phase MOSFET Driver

FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Fixed-frequency buck converter
- Operation at any PWM duty cycle up to and including 100%
- Programmable gate drive strength
- 10 to 80 V supply voltage operating range
- Programmable 3.3 or 5 V CMOS compatible logic I/O
- Three programmable current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Programmable control input logic sense
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems*

PACKAGE:

48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

*The AMT49100 was developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

DESCRIPTION

The AMT49100 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a 3-phase bridge arrangement and is specifically designed for 48 V automotive power applications with high-power inductive loads, such as BLDC motors.

A fixed-frequency buck converter provides a regulated gate drive and bootstrap charge voltage over the full supply voltage range from 10 to 80 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs. The bootstrap charge is maintained by an additional charge pump providing 0-100% PWM with no duty cycle restriction.

Full control over all six power MOSFETs in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

In addition to providing full access to the bridge control, the serial interface is also used to alter programmable settings such as dead time, VDS threshold, and fault blank time. Detailed diagnostic information can be read through the serial interface.

The AMT49100 is supplied in a 48-pin QFP package (suffix JP) with exposed thermal pad. The package is lead (Pb) free with 100% matte-tin leadframe plating.

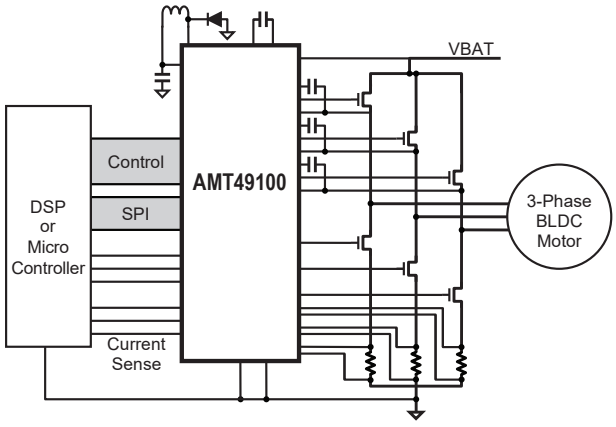


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Buck Regulator	V_{IO} (V)	Packing	Package
AMT49100KJPTR-A-3	Enabled	3.3	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-terminal LQFP with exposed thermal pad
AMT49100KJPTR-A-5	Enabled	5		
AMT49100KJPTR-B-3	Disabled	3.3		
AMT49100KJPTR-B-5	Disabled	5		

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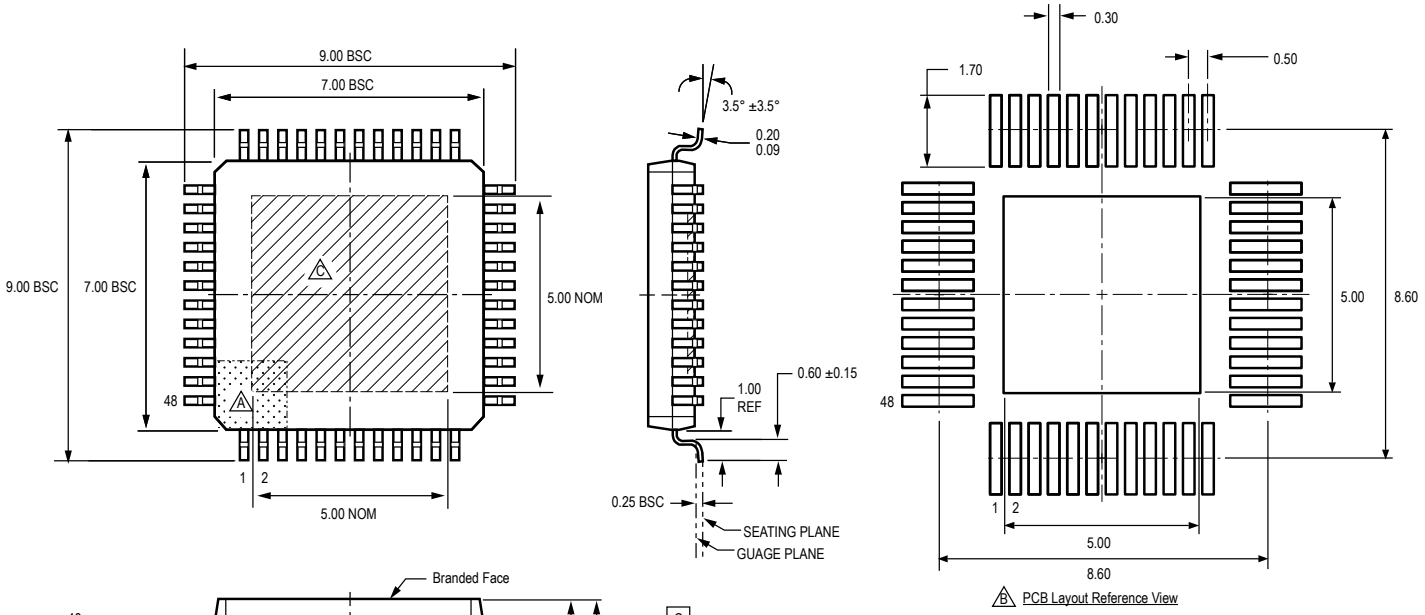
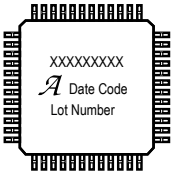
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown





A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

Figure 2: JP Package, 48-Pin LQFP with Exposed Thermal Pad

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Revision History

Number	Date	Description
–	March 24, 2020	Initial release
1	May 8, 2020	Updated GHx and GLx Active Pull-Down test conditions and maximum values (page 8), Off-State Test Sink and Source Current test conditions (page 12), External Regulated Supply Mode section (page 19), Gate Drive Control section (page 23), Register 7 (page 46), and Register 6 (page 53). Removed I_{REGS} characteristic (page 6).
2	July 9, 2020	Updated Bootstrap Boost Voltage values (page 6), Pull-Up On-Resistance max values (page 7); removed Input Common Mode Range (page 10); updated VDS Threshold High-Side and Low-Side values (page 11); added footnote 9 to Temperature Warning Threshold, Temperature Warning Hysteresis, Overtemperature Threshold, and Overtemperature Hysteresis (page 12); updated Logic Outputs section (page 24), Monitor: VCC Undervoltage section (page 28), and Bridge: Phase Disconnected section (page 38).
3	October 28, 2021	Updated VBRG Operating Range, VBRG Input Current, VREG Quiescent Current Regulator Inactive, Bootstrap Boost Voltage (page 6), Pull-Up On-Resistance, Pull-Up Peak Source Current, Pull-Down Peak Source Current (page 7), Input Offset Voltage, Input Common-Mode Range (DC) (page 10), Bootstrap Undervoltage (page 11); removed Input Pulse Filter Time (page 9) and VBRG Input Current (page 11); updated On-State Open Load Timeout, LSS Current (page 12), Input and Output Terminal Functions (page 18), Buck Regulator Mode, External Regulated Supply Mode, VREG Supply Charge Pump Regulator (page 19), High-Side Gate Drive, Low-Side Gate Drive (page 21), Bridge: Bootstrap Capacitor Undervoltage Fault (page 34), On-Line Verification (page 37), VIO, VCL, and BRE footnotes (page 53); added Application Information (page 66-68) and Layout Guidelines (page 70-71); updated package drawing (page 72).
4	January 17, 2023	Updated ASIL statement status (page 1); Updated Bootstrap Boost Voltage test conditions and typical value (page 6); typo corrected in Register 6 footnote (page 53)
5	January 22, 2025	Updated reference to ISO 26262 (page 1), Drive Regulator Terminal rating (page 3), functional block diagram (page 5), VREG Supply Ripple Rejection characteristic (page 10), Status Register Mapping table (page 48), Register 3 threshold values (page 51), Register 6 VCL value (page 53), Input/Output Structures Supplies figure (page 69), added errata, created short-form variant of long-form datasheet

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