80 V Automotive Three-Phase MOSFET Driver

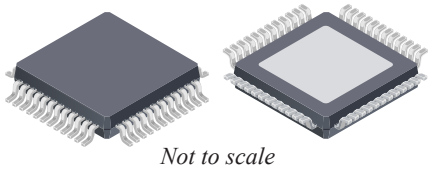
FEATURES AND BENEFITS

- 3-phase bridge MOSFET driver
- Bootstrap gate drive for N-channel MOSFET bridge
- Cross-conduction protection with adjustable dead time
- Fixed-frequency buck converter
- Operation at any PWM duty cycle up to and including 100%
- Programmable gate drive strength
- 10 to 80 V supply voltage operating range
- Programmable logic supply regulator controller
- Programmable 3.3 or 5 V CMOS compatible logic I/O
- Two programmable current sense amplifiers
- SPI-compatible serial interface
- Bridge control by direct logic inputs or serial interface
- Programmable control input logic sense
- Extensive programmable diagnostics
- Diagnostic verification
- Safety-assist features
- Automotive AEC-Q100 qualified
- A²-SIL™ product—device features for safety-critical systems*

ISO 26262 ASIL Compliant

PACKAGE:

48-pin LQFP with exposed thermal pad (suffix JP)



Not to scale

*The AMT49101 was developed in accordance with ISO 26262 as a hardware safety element out of context with ASIL D capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety application note and datasheet.

DESCRIPTION

The AMT49101 is an N-channel power MOSFET driver capable of controlling MOSFETs connected in a 3-phase bridge arrangement and is specifically designed for 48 V automotive power applications with high-power inductive loads, such as BLDC motors.

A fixed-frequency buck converter provides a regulated gate drive and bootstrap charge voltage over the full supply voltage range from 10 to 80 V. A bootstrap capacitor is used to provide the above-battery supply voltage required for N-channel MOSFETs. The bootstrap charge is maintained by an additional charge pump providing 0-100% PWM with no duty cycle restriction. The AMT49101 also provides a low voltage regulated output suitable for controller or sensor circuits power supply.

Full control over all six power MOSFETs in the 3-phase bridge is provided, allowing motors to be driven with block commutation or sinusoidal excitation. The power MOSFETs are protected from shoot-through by integrated crossover control and optional programmable dead time.

Integrated diagnostics provide indication of multiple internal faults, system faults, and power bridge faults, and can be configured to protect the power MOSFETs under most short-circuit conditions. For safety-critical systems, the integrated diagnostic operation can be verified under control of the serial interface.

Configuration settings can be set, and detailed diagnostic information can be read through the serial interface.

The AMT49101 is supplied in a 48-pin QFP package (suffix JP) with exposed thermal pad. The package is lead (Pb) free with 100% matte-tin leadframe plating.

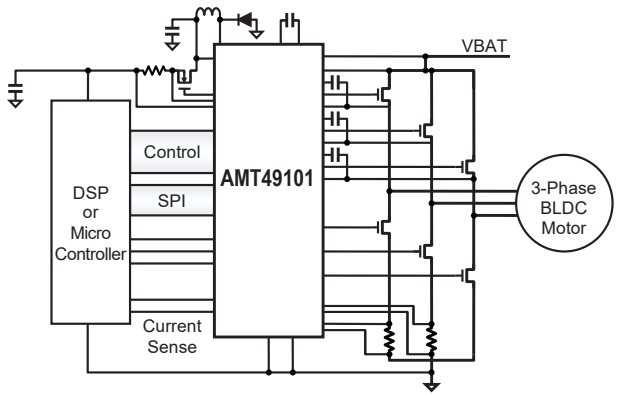


Figure 1: Typical Application

SELECTION GUIDE

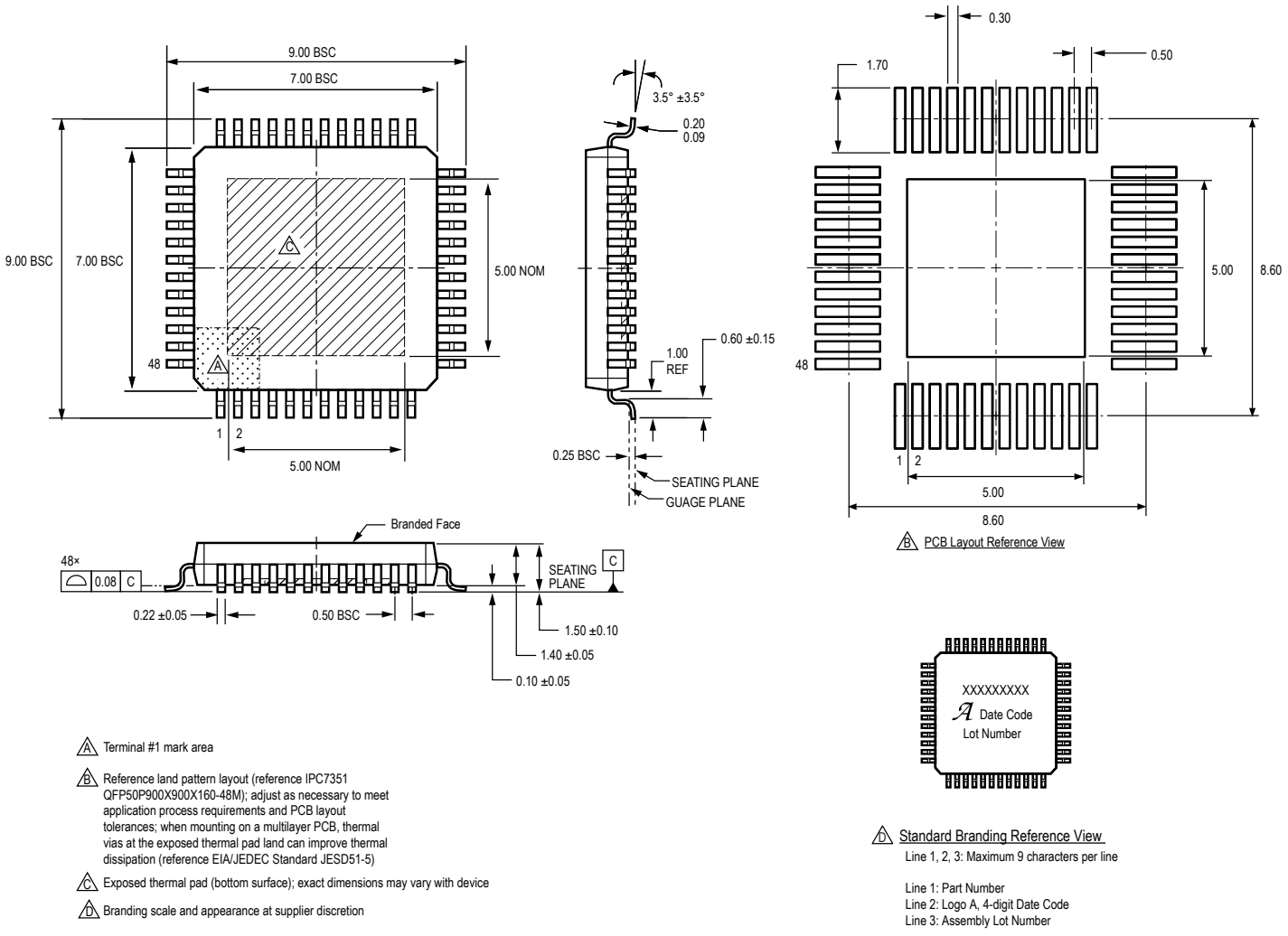
Part Number	Buck Regulator	V_{IO} (V)	Packing	Package
AMT49101KJPTR-A-3	Enabled	3.3	1500 pieces per 13-inch reel	7 mm × 7 mm, 1.6 mm nominal height 48-terminal LQFP with exposed thermal pad
AMT49101KJPTR-A-5	Enabled	5		
AMT49101KJPTR-B-3	Disabled	3.3		
AMT49101KJPTR-B-5	Disabled	5		

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000386, Rev. 5 or JEDEC MS-026 BBCHD)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 QFP50P900X900X160-48M); adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

C Exposed thermal pad (bottom surface); exact dimensions may vary with device

D Branding scale and appearance at supplier discretion

D Standard Branding Reference View
Line 1, 2, 3: Maximum 9 characters per line

Line 1: Part Number
Line 2: Logo A, 4-digit Date Code
Line 3: Assembly Lot Number

Figure 2: JP Package, 48-Pin LQFP with Exposed Thermal Pad

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
–	March 26, 2025	Initial release

For the latest version of this document, visit our website:
www.allegromicro.com

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com