50 V Code-Free FOC BLDC Motor Controller

FEATURES AND BENEFITS

- Code-free sensorless field-oriented control (FOC)
- Proprietary non-reverse fast startup
- Soft-On Soft-Off (SOSO) for quiet operation
- Analog / PWM / Clock mode speed control
- Closed-loop speed control
- Configurable current limit
- Windmill startup operation
- Lock detection
- Short-circuit protection (OCP)
- Brake and direction inputs

APPLICATIONS

- Ceiling fans
- Pedestal fans
- Bathroom exhaust fans
- Home appliance fans and pumps

EFFICIENCY WITH EASE QUIETMOTION

DESCRIPTION

The AMT49406 is a 3-phase, sensorless, brushless DC (BLDC) motor driver (gate driver) which can operate from 5.5 to 50 V.

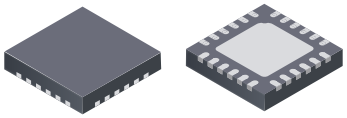
A field-oriented control (FOC) algorithm is fully integrated to achieve the best efficiency and acoustic noise performance. The device optimizes the motor startup performance in a stationary condition, a windmill condition, and even in a reverse windmill condition.

Motor speed is controlled through analog, PWM, or CLOCK input. Closed-loop speed control is optional, and RPM-to-clock frequency ratio is programmable.

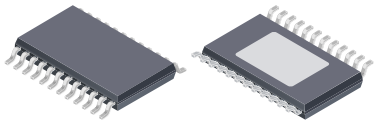
A simple I²C interface is provided for setting motor-rated voltage, rated current, rated speed, resistance, and startup profiles.

The AMT49406 is available in a 24-contact 4 mm × 4 mm QFN with exposed thermal pad (suffix ES) and a 24-lead TSSOP with exposed thermal pad (suffix LP). These packages are lead (Pb) free, with 100% matte-tin leadframe plating.

PACKAGES



24-contact QFN
with exposed thermal pad
4 mm × 4 mm × 0.75 mm
(ES package)



24-lead TSSOP
with exposed thermal pad
(LP package)

Not to scale

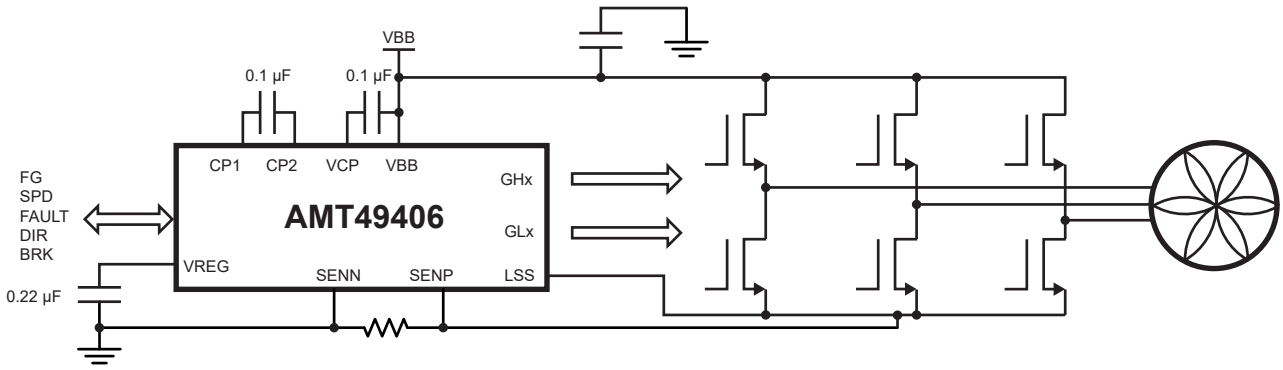


Figure 1: Typical Application

SELECTION GUIDE

Part Number	Ambient Temperature Range (T_A) (°C)	Packaging	Packing
AMT49406GESSR	–40 to 105	24-contact QFN with exposed thermal pad	6000 pieces per 13-inch reel
AMT49406GLPTR	–40 to 105	24-lead TSSOP with exposed thermal pad	4000 pieces per 13-inch reel

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{BB}		50	V
Logic Input Voltage Range	V_{IN}	SPD, BRAKE, DIR	–0.3 to 6	V
Logic Output	V_O	FG (I < 5 mA)	6	V
LSS	V_{LSS}	DC	±500	mV
		t_W < 500 ns	±4	V
VREG	V_{REG}		0 to 4	V
SENN, SENP	V_{SENN}, V_{SENP}	DC	±500	mV
		t_W < 500 ns	±4	V
Output Voltage	V_{OUT}	SA, SB, SC	–2 to V_{BB}+2	V
GHx	V_{GHx}		V_{Sx}–0.3 to V_{CP}+0.3	V
GLx	V_{GLx}		V_{LSS}–0.3 to 8.5	V
VCP	V_{CP}		V_{BB}–0.3 to V_{BB}+8	V
CP1	V_{CP1}		–0.3 to V_{BB}+0.3	V
CP2	V_{CP2}		V_{BB}–0.3 to V_{CP}+0.3	V
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C
Operating Temperature Range	T_A	Range G	–40 to 105	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	24-contact QFN (package ES), on 2-sided PCB 1-in.^{2} copper	45	°C/W
		24-lead TSSOP (package LP), on 2-sided PCB 1-in.^{2} copper	36	°C/W

*Additional thermal information is available on the Allegro website.

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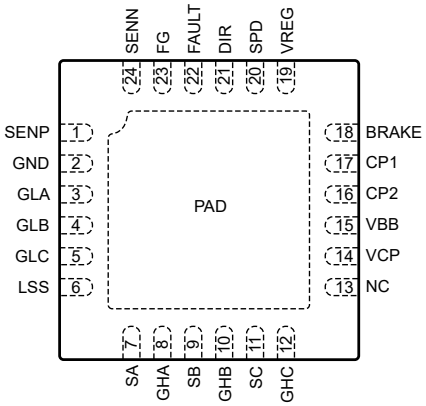
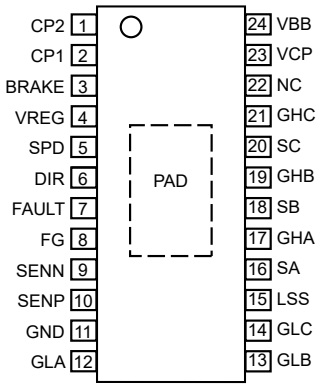
PINOUT DIAGRAMS AND TERMINAL LIST TABLE



ES Package Pinouts



LP Package Pinouts

Terminal List Table

Terminal Number		Name	Function
ES Package	LP Package		
16	1	CP2	Charge pump
17	2	CP1	Charge pump
18	3	BRAKE	Logic input
19	4	VREG	2.8 V regulator voltage
20	5	SPD	PWM or clock mode speed control
21	6	DIR	Direction control
22	7	FAULT	Fault indicator output
23	8	FG	Motor speed output
24	9	SENN	Current sense negative terminal
1	10	SENP	Current sense positive terminal
2	11	GND	Ground
3	12	GLA	Low-side gate drive output
4	13	GLB	Low-side gate drive output
5	14	GLC	Low-side gate drive output
6	15	LSS	Low-side source
7	16	SA	Motor output
8	17	GHA	High-side gate drive output
9	18	SB	Motor output
10	19	GHB	High-side gate drive output
11	20	SC	Motor output
12	21	GHC	High-side gate drive output
13	22	NC	No connect
14	23	VCP	Charge pump
15	24	VBB	Power supply
PAD	PAD	PAD	Exposed pad for enhanced thermal dissipation

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ELECTRICAL CHARACTERISTICS [1]: Valid over operating ambient temperature range and operating voltage range, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
GENERAL						
Supply Voltage Range	V_{BB}	Driving	5.5	–	48	V
		Operating	5.5	–	50	V
VBB Supply Current	I_{BB}	I_{VREG} = 0 mA	–	8	12	mA
		Standby mode	–	10	20	µA
Reference Voltage	V_{REG}	I_{OUT} = 10 mA	2.7	2.86	2.95	V
GATE DRIVE						
High Side Gate Drive Output	V_{GH}	V_{BB} = 8 V	6.5	6.8	–	V
		V_{BB} = 24 V	6.5	6.8	–	V
Low Side Gate Drive Output	V_{GL}	V_{BB} = 8 V	6.5	7.3	–	V
		V_{BB} = 24 V	6.5	7.3	–	V
Gate Drive Source Current	I_{SO}		–	55	–	mA
Gate Drive Sink Current	I_{SI}		–	105	–	mA
MOTOR DRIVE						
PWM Duty On Threshold	PWM_{ON}	Relative to target	–0.5	–	0.5	%
PWM Duty Off Threshold	PWM_{OFF}	Relative to target	–0.5	–	0.5	%
PWM Input Frequency Range	$f_{PWM(MIN)}$	PWM input frequency setting = 0	2.5	–	100	kHz
		PWM input frequency setting = 1	80	–	3200	Hz
Clock Input Frequency Range	f_{CLOCK}	CLOCK mode	1	–	2000	Hz
SPD Standby Threshold (Analog Enter)	$V_{SPD(TH\_ENT)}$		50	100	150	mV
SPD Standby Threshold (Analog Exit)	$V_{SPD(TH\_EXIT)}$		0.4	0.75	1	V
SPD On Threshold	$V_{SPD(ON)}$	ON/OFF setting = 10%	210	250	290	mV
SPD Max	$V_{SPD(MAX)}$		–	2.5	–	V
SPD ADC Resolution	$V_{SPDADC(RES)}$		–	9.78	–	mV
SPD ADC Accuracy	$V_{SPDADC(ACC)}$	V_{SPD} = 0.2 to 2.5 V	–40	–	40	mV
Speed Closed Loop Accuracy	$f_{SPD(ACC)}$	PWM mode or Analog mode	–5	–	5	%
		Clock mode	–0.1	–	0.1	rpm
Dead Time	t_{DT}	Code = 9	–	400	–	ns
Motor PWM Frequency	f_{PWM}	T_A = 25°C	23.3	24.4	25.4	kHz
PROTECTION						
VBB UVLO	$V_{BB(UVLO)}$	V_{BB} rising	–	4.75	4.95	V
VBB UVLO Hysteresis	$V_{BB(HYS)}$		200	300	450	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	165	–	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C

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ELECTRICAL CHARACTERISTICS [1] (continued): Valid over operating ambient temperature range and operating voltage range, unless noted otherwise

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
LOGIC, IO, I²C						
Input Current	I_{IN}	SPD, FG; V_{IN} = 0 to 5.5 V	–5	1	5	µA
		BRK, DIR; V_{IN} = 5 V	–	50	–	µA
Logic Input, Low Level	V_{IL}		0	–	0.8	V
Logic Input, High Level	V_{IH}		2	–	5.5	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
FG Output Leakage	I_{FG}	V = 5.5 V	–	–	1	µA

[1] Specified limits are tested at 25°C and 125°C and statistically assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The AMT49406 is a three-phase BLDC controller with integrated gate driver. It operates from 5.5 to 50 V and targets pedestal fan, ceiling fan, and ventilation fan applications.

The integrated field-oriented control (FOC) algorithm achieves the best efficiency and dynamic response and minimizes acoustic noise. Allegro's proprietary non-reverse startup algorithm improves startup performance. The motor will start up towards the target direction after power-up without reverse shaking or vibration. The Soft-On Soft-Off (SOSO) feature gradually increases the current to the motor at "on" command (windmill condition), and gradually reduces the current from the motor at the "off" command, further reducing the acoustic noise and operating the motor smoothly.

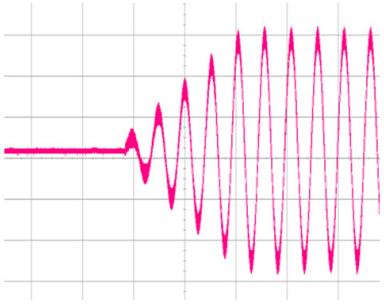

Figure 2: Current Waveform of Soft-On

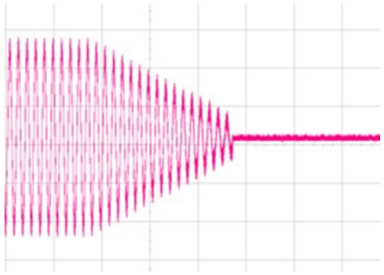

Figure 3: Current Waveform of Soft-Off

Speed Control

Speed demand is provided via the SPD pin. Three speed control modes are selectable through the EEPROM. The AMT49406 also features a closed-loop speed function, which can be enabled or disabled via the EEPROM.

PWM Mode: The motor speed is controlled by the PWM duty cycle on the SPD pin, and higher duty cycle represents higher speed demand. If closed-loop speed is disabled, the output amplitude will be proportional to the PWM duty cycle. If closed-loop speed is enabled, the motor speed is proportional to the PWM duty cycle, and 100% duty represents the rated speed of the motor, which can be programmed in the EEPROM.

$$close\_loop\_speed = rated\_speed \times duty\_input$$

The SPD PWM frequency range is 80 Hz to 100 kHz. If it is higher than 2.8 kHz, set PWMfreq = 0; if it is lower than 2.8 kHz, set PWMfreq = 1.

Analog Mode: The motor speed is controlled by the analog voltage on the SPD pin, with higher voltage representing higher speed demand. If closed-loop speed is disabled, the output amplitude will be proportional to the analog voltage input. If closed-loop speed is enabled, the motor speed is as follows:

$$closed\_loop\_speed = rated\_speed \times analog\_input / SPD_{MAX}$$

CLOCK Mode: In the clock speed control mode, the closed-loop speed is always enabled. Higher frequency on the SPD pin will drive a higher motor speed as follows:

$$close\_loop\_speed\ (rpm) = clock\_input \times speed\_ctrl\_ratio,$$

where the speed_ctrl_ratio can be programmed in the EEPROM.

For example, if the ratio is 4 and the clock input frequency is 60 Hz, then the motor will operate at 240 rpm. Note the number of motor pole pairs must be set properly in the programming application for the rated speed (rpm) setting to be accurate.

If the clock frequency commands a speed that is higher than twice the rated speed, the AMT49406 treats it as a clock input error and stops the motor.

For all three speed control modes with closed-loop speed enabled, if the demand speed is higher than the maximum speed, the system can run at a certain supply voltage and load condition, and the AMT49406 will just provide the maximum output voltage (if current limit is not triggered) or the maximum output current (if current limit is triggered).

The SPD pin is also used as SCL in the I^2C mode.

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Motor Stop and Standby Mode

If the speed demand is less than the programmed threshold, the motor will stop.

On/Off Setting	On Threshold	Off Threshold
6%	7.8%	5.9%
10%	11.7%	9.8%
15%	14.9%	12.9%
20%	21.5%	19.6%

For example, consider 10% is set as the threshold. If PWM duty is less than 9.8% (in PWM mode), or the analog voltage is less than 250 mV (in Analog mode), or the CLOCK input frequency is less than 9.8% of the "rated_speed" (in CLOCK mode), the IC will stop the motor and enter the "idle" mode.

In order to enter standby, two conditions must be met: 1) the motor must be stationary, and 2) PWM or CLOCK signal must remains logic low (in PWM and CLOCK mode) or the analog voltage remains less than $V_{SPD(TH\_ENT)}$ (in Analog mode) for longer than one second.

A rising edge on PWM or CLOCK will wake the IC in PWM and CLOCK mode, and in Analog mode, the SPD voltage must be higher than $V_{SPD(TH\_EXIT)}$ to wake up the IC.

Standby Mode will turn off all circuitry including the charge pump and VREG.

After powering on, the device will always be in the active mode before entering standby mode.

The standby mode can be disabled in the EEPROM.

Direction Input: Logic input to control motor direction. For logic high, the motor phases are ordered A→B→C. For logic low, the motor phases are ordered A→C→B. The AMT49406 supports changing the direction input while the motor is running. The direction can also be controlled through register.

BRAKE: Active-high signal turns on all low sides for braking function. The Brake function overrides speed control input. Care should be taken to avoid stress on the MOSFET when braking while the motor is running. With braking, the current will be limited only by V_{BEMF}/R_{MOTOR}. The AMT49406 includes an optional feature which holds off braking until the motor speed drops to a low enough (configurable) level so that the braking current will not damage the MOSFET.

FAULT: Open-drain output provides motor operation fault status. Default is high when there is no fault.

An LED and a serial resistor is recommended between the FAULT and VREG pins. The LED indicates fault information.

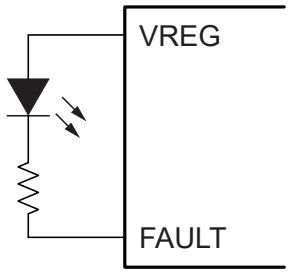

Figure 4: AMT49406 with LED and Serial Resistor

Fault Type	FAULT Pin	LED Pattern
Lock detected	low	constant on
OCP	0.67 seconds high 0.67 seconds low	slow flashing
OTP	0.67 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high 0.08 seconds low 0.17 seconds high	long-short-short flashing
system error	0.08 seconds low 0.08 seconds high 0.08 seconds low 1.09 seconds high	double short flashing
OVP	0.17 seconds high 0.17 seconds low	fast flashing
zero speed demand	0.25 seconds high 0.08 seconds low 0.34 seconds high 0.67 seconds low	long-short flashing

FG: Open-drain output provides motor speed information to the system. The open-drain output can be pulled up to VREG or an external 3.3 or 5 V supply.

The FG pin is also used as SDA in I^2C mode. The first I^2C command can pass only when the FG is high (open drain off). After the first I^2C command, the FG pin is no longer used for speed information, and the FG pin is dedicated as a data pin for the I^2C interface.

FG is default high after power-on and exit from standby mode, and stays high for at least 9.8 ms. To ensure successful I^2C communication, it is recommended to have the first I^2C demand right after power-up or exit from standby mode within 9.8 ms.

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VREG: Voltage reference (2.8 V) to power internal digital logic and analog circuitry. VREG can be used to power external circuitry with up to 10 mA bias current, if desired. A ceramic capacitor with 0.22 µF or greater is required on the pin to stabilize the supply.

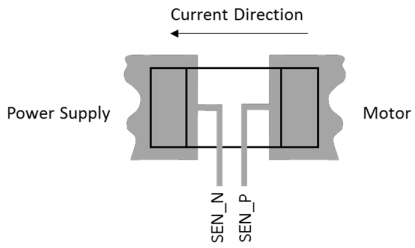
When VREG is loaded externally, the power consumption of the internal LDO is calculated by the equation:

$$P_{LDO} = (I_{LOAD} + I_{INTERNAL}) \times (V_{BB} - V_{REG}).$$

Ensure that the system has good power dissipation and the temperature is within the operating temperature range. The AMT49406 thermal shutdown function does not protect the LDO.

Bus Current Sensing: A single shunt-resistor connection between SENN and SENP is used to measure the bus current for the FOC algorithm and current limit. The resistor value is approximately tens of a milliohm, depends on the rated current of the system. The voltage difference between SENN and SENP should be less than 65 mV to prevent signal saturation. For example, if the rated current is 4 A, it is recommended to use a 15 mΩ sensing resistor, so that 4 A × 15 mΩ is between 55 and 65 mV.

Use Kelvin sensing connection for the shunt resistor.



Lock Detect: A logic circuit monitors the motor position to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for the configurable t_{LOCK} time before an auto-restart is attempted. For additional information, refer to the configuration guide.

Current Control: The motor's rated current at rated speed and normal load must be programmed to the EEPROM for proper operation. The AMT49406 will limit the motor current (phase current peak value) to 1.3 times the programmed rated current during acceleration or increasing load, which protects the IC and the motor. The current profile during startup can also be programmed.

Overcurrent Protection (short protection): The V_{DS} voltages across each power MOSFET are monitored by the AMT49406. If a V_{DS} is higher than the threshold when that MOSFET enabled, an OCP fault is triggered and the IC will stop driving immediately.

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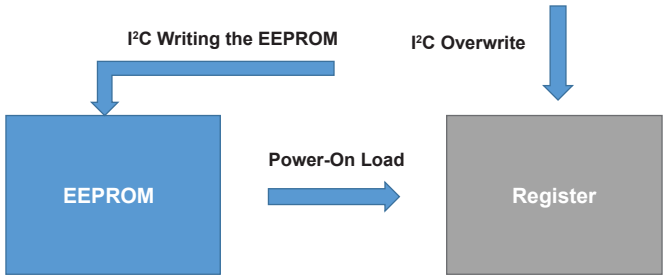
I²C OPERATION AND EEPROM MAP

The I²C interface allows the user to program the register and parameters into EEPROM. The AMT49406 7-bit peripheral address is 0x55.

After power-on, the default values in EEPROM will be loaded into the registers, which determines motor system operation. I²C can overwrite those values and change the motor system operation on the fly.

I²C can also be used to program the EEPROM, which is normally done in the production line.

The figures below shows the I²C interface timing.



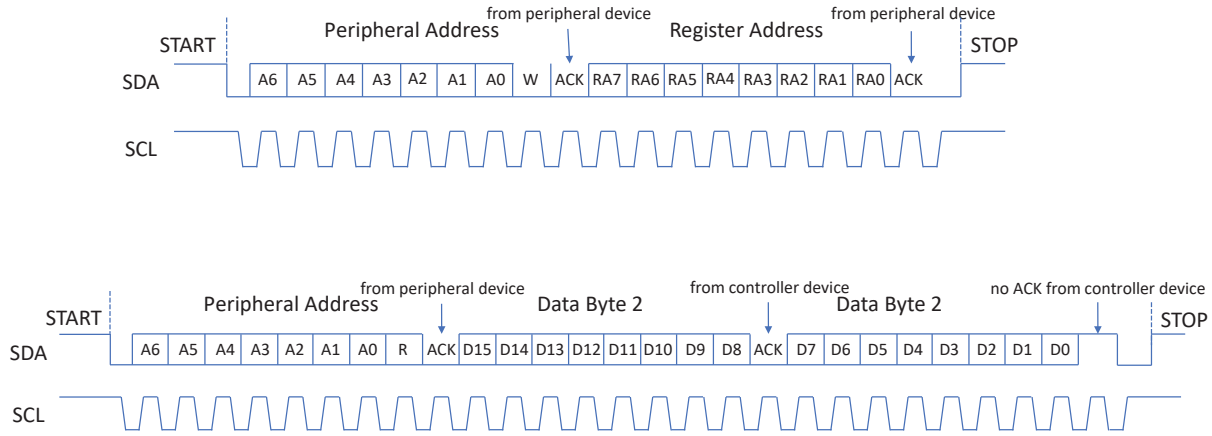


Figure 5: Read Command

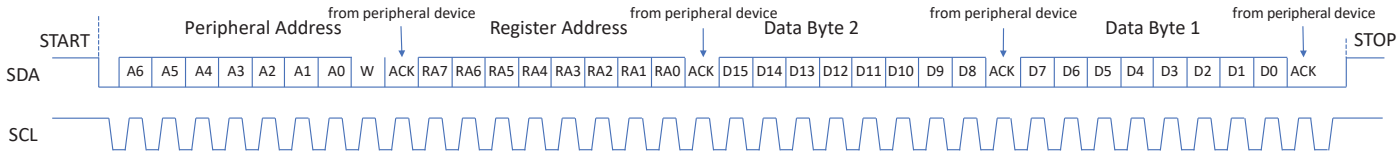


Figure 6: Write Command

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Register and EEPROM Map

Each register bit is associated with one EEPROM bit. The register address is the associated EEPROM bit address plus 64. For example, the rated speed is in EEPROM address 8, bit[10:0]; the associated register address is 72, bit[10:0].

In the following table, the bits shaded in gray should be kept at their default values. Changing these values may cause malfunction or damage to the part. If programming the EEPROM with a custom programmer, it is recommended to use the AMT49406 application to determine the appropriate settings, save the settings file, and use the file contents to program to the EEPROM. The application's settings file contains one line for each EEPROM address, containing addresses 8 through 22 (15 lines/addresses).

Registers not shown in the table are not for users to access. Changing the value in undocumented registers may cause malfunction or damage to the part.

Table 1: Register and EEPROM Map

Address		AMT49406 Register Map			
0		Allegro internal information. No associated register for these EEPROM data			
1					
2					
3					
4					
5					
6		User-flexible code. No associated register for these EEPROM data. Provided to user. For example, tracking number of product, product revision info, etc.			
7					
8 / 72	3:0	RATED_SPEED [3:0]			
	7:4	RATED_SPEED [7:4]			
	11:8	SPEED_CLOSE_LOOP	RATED SPEED [10:8]		
	15:12	PWMIN_RANGE	DIRECTION	ACCELERATE_RANGE	CLOCK_PWM
9 / 73	3:0	ACCELERATION [3:0]			
	7:4	ACCELERATION [7:4]			
	11:8	MOTOR_RESISTANCE [3:0]			
	15:12	MOTOR_RESISTANCE [7:4]			
10 / 74	3:0	RATED CURRENT [3:0]			
	7:4	RATED CURRENT [7:4]			
	11:8	SPD MODE	RATED CURRENT [10:8]		
	15:12	STARTUP_CURRENT [2:0]			
11 / 75	3:0	OPEN_DRIVE			
	7:4	POWER_CTL_EN			OPEN_PH_PROTECT
	11:8	STARTUP_MODE [1:0]			
	15:12				
12 / 76	3:0	PID_P [3:0]			
	7:4	PID_P [7:4]			
	11:8	MOTOR_INDUCTANCE [3:0]			
	15:12	OPEN_WINDOW		OVER_SPEED_LOCK	MOTOR_INDUCTANCE [4]

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Table 1: Register and EEPROM Map (continued)

Address		AMT49406 Register Map			
13 / 77	3:0	PID_I [3:0]			
	7:4	PID_I [7:4]			
	11:8				
	15:12		DELAY_START		
14 / 78	3:0				
	7:4				
	11:8				
	15:12				
15 / 79	3:0	ANGLE_ERROR_LOCK (startup)			
	7:4	SOFT_ON	SOFT_OFF		
	11:8	DEADTIME_SETTING [3:0]			
	15:12	SAFE_BRAKE_THRD [1:0]			
16 / 80	3:0	OCP_RESET_MODE	OCP_ENABLE		
	7:4	FIRST_CYCLE_SPEED [1:0]			
	11:8	DECELERATE_BUFFER [1:0]		ACCELERATE_BUFFER [1:0]	
	15:12			BEMF_LOCK_FILTER [1:0]	
17 / 81	8:0	SPEED_DEMAND [8:0]			
	9	I2C_SPEED_MODE			
	15:10				
18 / 82	3:0				
	7:4				
	11:8	IPD_CURRENT_THR [3:0]			
	15:12			IPD_CURRENT_THR [5:4]	
19 / 83	7:0				
	15:8				
20 / 84	7:0	RATED_VOLTAGE			
	15:8	SENSE_RESISTOR			
21 / 85	3:0				
	7:4	SLIGHT_MV_DEMAND [2:0]			
	11:8			SPEED_INPUT_OFF_THRESHOLD [1:0]	
	15:12	STANDBY_DIS			
22 / 86	3:0	SPEED CLOSE LOOP PARAMETER			
	7:4	RESTART_ATTEMPT		SPEED CLOSE LOOP PARAMETER	
	11:8	LOCK_RESTART_SET	VIBRATION_LOCK		BRAKE_MODE
	15:12				

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Table 2: Register and EEPROM Map Notes

Parameter	Address	Notes
RATED_VOLTAGE	20 [7:0]	Rated Voltage (V) = Rated_voltage_register_value / 5
RATED_SPEED	8 [10:0]	Rated Speed (Hz) = Rated_speed_register_value × 0.530
MOTOR_RESISTANCE	9 [15:8]	Motor Resistance (Ω) = Motor_resistance_register_value / [(Rated_voltage_register_value × 4.096) / (Sense_resistor_register_value / 125) / (Rated_voltage_register_value / 10)]
RATED_CURRENT	10 [10:0]	Rated Current (mA) = Rated_current_register_value / (Sense_resistor_register_value / 125)
STARTUP_CURRENT	10 [15:13]	0: NA. else Startup Current = Rated Current × 1/8 × (startup_current_register_value + 1)
ACCELERATION	9 [7:0]	Acceleration (Hz/s) = Acceleration_register_value × k if range = 0 then k = 0.05, else k = 3.2
ACCELERATE_RANGE	8 [13]	
SPEED_CLOSE_LOOP	8 [11]	1: closed loop. 0: open loop.
DIRECTION	8 [14]	1: A→B→C. 0: A→C→B.
SPD MODE	10 [11]	1: analog 0: digital (PWM or Clock).
CLOCK_PWM	8 [12]	1: clock mode. 0: PWM mode.
PWMIN_RANGE	8 [15]	1: ≤ 2.8 kHz 0: > 2.8 kHz.
CLOCK_SPEED_RATIO	22 [5:0]	Ratio (rpm/Hz) = clock_speed_ratio_value × 0.25. clock_speed_ratio maximum value is 42.
SPEED_INPUT_OFF_THRESHOLD	21 [9:8]	00: 10%. 01: 6% 10: 15%. 11: 20%
STARTUP_MODE	11 [11:10]	00: 6 pulse mode. 01: 2 pulse mode. 10: slight-move mode. 11: align & go.
IPD_CURRENT_THRD	18 [13:8]	IPD current threshold (A) = IPD_current_thrd_value × 0.086
SLIGHT_MV_DEMAND	21 [7:5]	Amplitude demand in slight move mode (%) = value × 3.2 + 2.4
PID_P	12 [7:0]	Position observer loop P gain.
PID_I	13 [7:0]	Position observer loop I gain.
MOTOR_INDUCTANCE	12 [12:8]	Refer to the configuration guide.
SENSE_RESISTOR	20 [15:8]	Sense resistor value (mΩ) = sense_resistor_value / 3.7
OPEN_DRIVE	11 [3]	Refer to the configuration guild.
POWER_CTRL_EN	11 [7]	1: enable the current limit.
OPEN_WINDOW	12 [15]	1: open window for inductance tuning. 0: normal
DELAY_START	13[14]	1: delayed start. 0: start right after windmill checking.
SOFT_OFF	15 [6]	Refer to the functional description.
SOFT_ON	15 [7]	Refer to the functional description.
FIRST_CYCLE_SPEED	16 [7:6]	00: 0.55 Hz. 01: 1.1 Hz. 10: 2.2 Hz. 11: 4.4 Hz
ACCELERATE_BUFFER	16 [9:8]	Refer to the configuration guide.
DECELERATE_BUFFER	16 [11:10]	Refer to the configuration guide.
DEADTIME_SETTING	15[11:8]	(n + 1) × 40 ns.
STANDBY_MODE	21 [15]	0: enable. 1: disable.
BRAKE_MODE	22 [8]	0: brake when safe. 1: 100% uncontrolled
SAFE_BRAKE_THRD	15 [15:14]	00: 1× rated current. 01: 2×. 10: 4×. 11: 8×.
OCP_RESET_MODE	16 [3]	0: upon motor restart. 1: after 5 seconds.

Continued on next page...

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Table 2: Register and EEPROM Map Notes (continued)

Parameter	Address	Notes
OCP_ENABLE	16 [2:0]	100: 480 ns filter. 111: OCP disabled.
ANGLE_ERROR_LOCK	15 [3:2]	Lock detect during startup. 00: disabled. 01: 5 degrees. 10: 9 degrees. 11: 13 degrees
BEMF_LOCK_FILTER	16 [13:12]	Refer to the configuration guide.
OPEN_PH_PROTECT	11 [4]	Refer to the configuration guide.
VIBRATION_LOCK	22 [10]	Refer to the configuration guide.
OVER_SPEED_LOCK	12 [13]	Refer to the configuration guide.
RESTART_ATTEMPT	22 [7:6]	00: Always. 01: 3 times. 10: 5 times. 11: 10 times.
LOCK_RESTART_SET	22 [11]	0: 5 seconds. 1: 10 seconds.
I2C_SPD_MODE	17 [9]	0: controlled by SPD pin. 1: controlled by register value in 17 [8:0].
I2C_SPD_DEMAND	17 [8:0]	0~511 represents 0~100%
READBACK		
MOTOR SPEED	120	Motor Speed (Hz) = register_value × 0.530 Hz
BUS CURRENT	121	Bus current (mA) = register_value / (Sense_resistor_register_value / 125)
Q-AXIS CURRENT	122	Q-axis current (mA) = register_value / (Sense_resistor_register_value / 125)
V_{BB}	123	V_{BB} (V) = register_value / 5
TEMPERATURE	124	Temperature (°C) = register_value – 53
CONTROL DEMAND	125	0~511 represents 0~100%
CONTROL COMMAND	126	0~511 represents 0~100%
OPERATION STATE	127 [15:12]	

Note: Refer to application note and user interface for additional detail.

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Programming EEPROM

The AMT49406 contains 24 words of EEPROM, each of 16 bit length. The EEPROM is controlled with the following I²C registers.

EEPROM Control – Register 161: Used to control programming of EEPROM

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	0	RD	WR	ER	EN

Bit	Name	Description
0	EN	Set EEPROM voltage required for Writing or Erasing.
1	ER	Sets Mode to Erase.
2	WR	Sets Mode to Write.
3	RD	Sets Mode to Read. Note this bit is not needed to read the EEPROM when using the method described on the following page.
15:4	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Address – Register 162: Used to set the EEPROM address to be altered

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	0	0	0	0	0	0	0	0	0	0	0	eeADDRESS				

Bit	Name	Description
0:4	eeADDRESS	Used to specify the EEPROM address to be erased or written. There are 24 addresses.
15:5	n/a	Do not use; always set to zero (0) during programming process.

EEPROM Data_In – Register 163: Used to set the EEPROM new data to be programmed

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	eeDATAin															

Bit	Name	Description
15:0	eeDATAin	Used to specify the new EEPROM data to be changed. This must be set to 0 when erasing the current EERPOM contents.

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EEPROM Commands

To change the contents of a memory location, the word must be first erased. The EEPROM programming process (writing or erasing) takes about 15 ms per word.

Each word must be written individually. The example below is shown in the following format:
I²C Write/Read, I2C_REGISTER_ADDRESS [data] // comment

Example #1: Write 261 (0x000105) to EEPROM address 7

1. Erase the existing data.
   - A. I²C Write, 162 [7] // set which EEPROM address to erase.
   - B. I²C Write, 163 [0] // set DATA_IN = 0x000000.
   - C. I²C Write, 161 [3] // set control to erase and set voltage high.
   - D. Wait 15 ms // requires 15 ms high-voltage pulse to erase.
2. Write the new data.
   - A. I²C Write, 162 [7] // set which EEPROM address to write.
   - B. I²C Write, 163 [261] // set DATA_IN = 261 (0x000105).
   - C. I²C Write, 161 [5] // set control to write and set voltage high.
   - D. Wait 15 ms // requires 15 ms high-voltage pulse to write.

Example #2: Read EEPROM address 7 to confirm the data was properly programmed.

1. Read the word.
   - A. I²C Read, 7 // read I2C register 7; this will be contents of EEPROM address 7.

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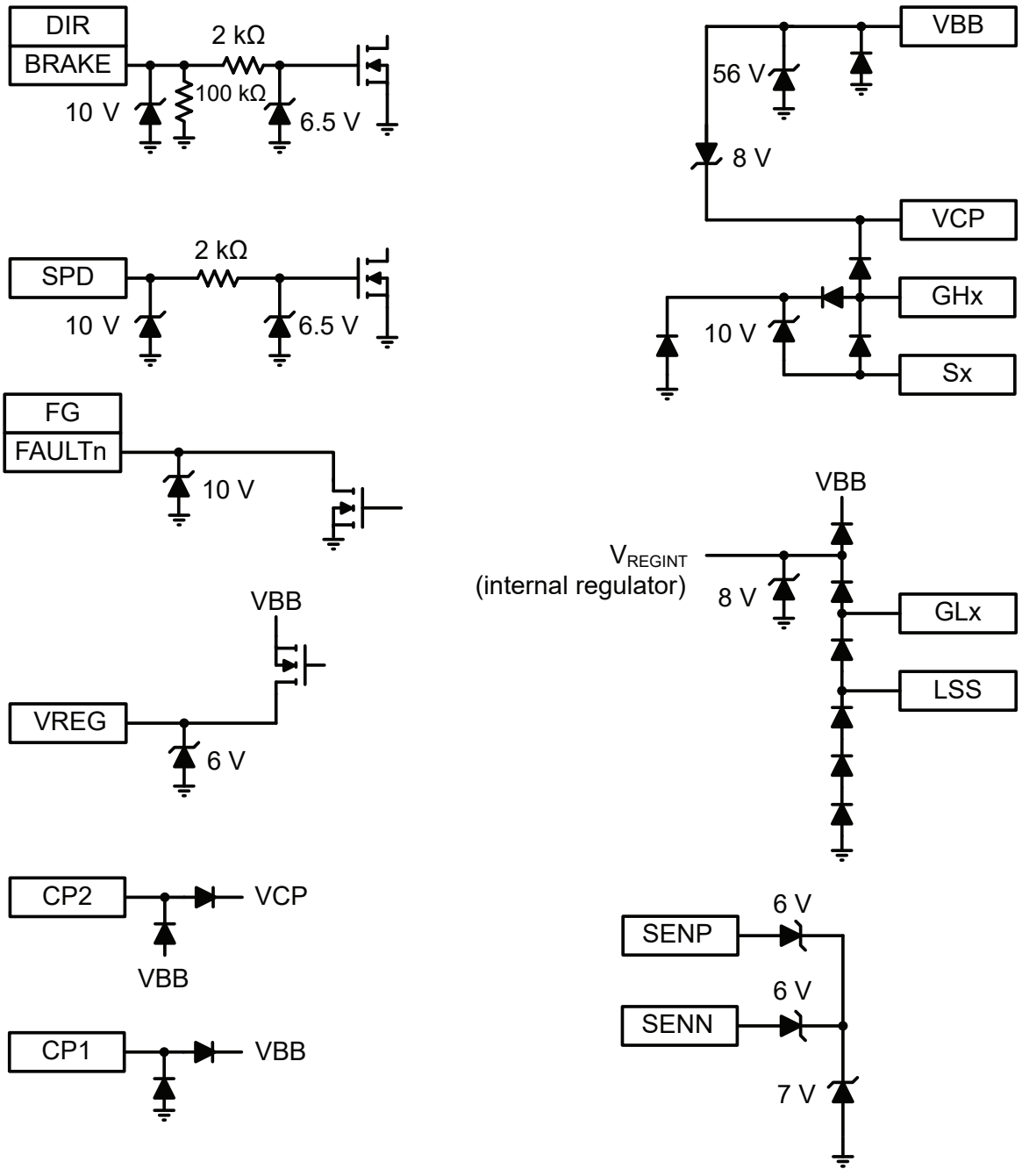
PIN DIAGRAMS



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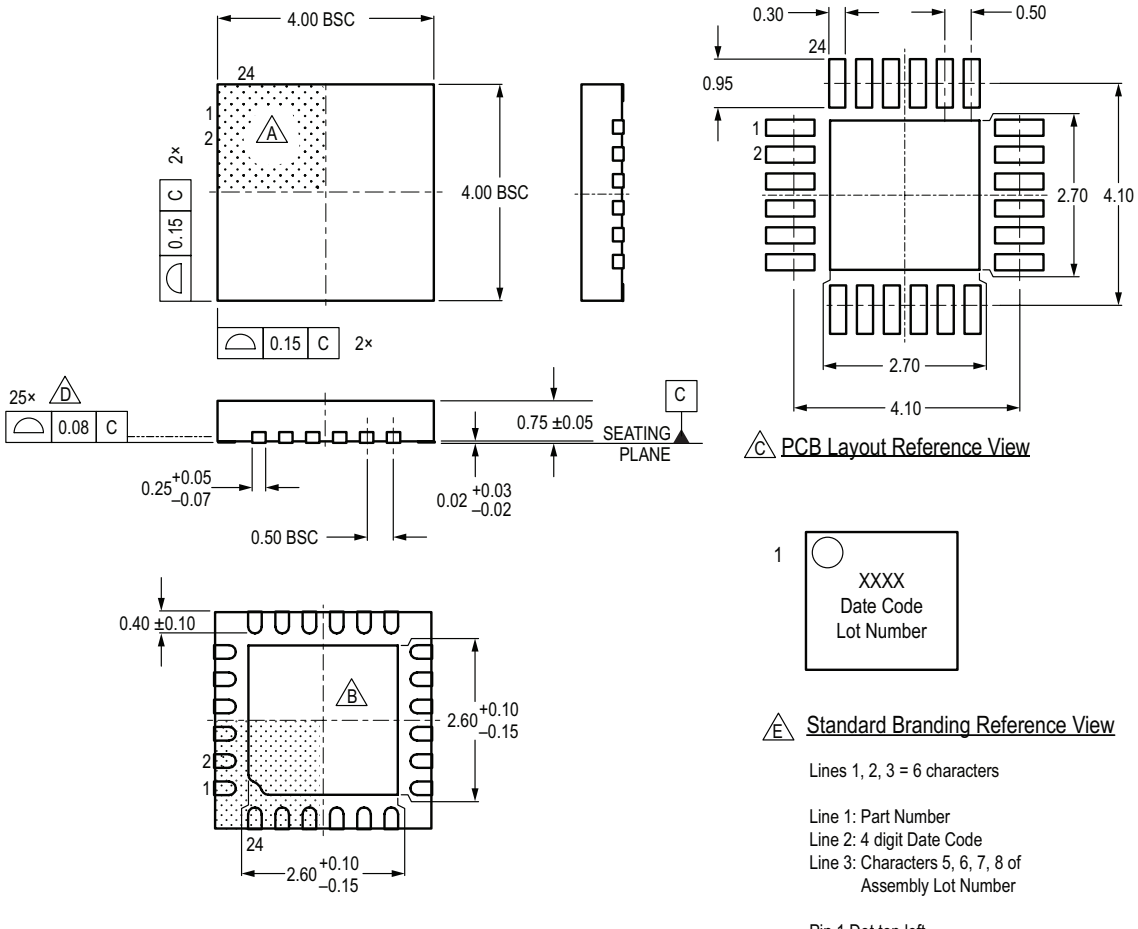
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000222 Rev. 4 or JEDEC MO-220WGGD.)
Dimensions in millimeters – NOT TO SCALE.
Exact case and lead configuration at supplier discretion within limits shown.



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion).

C Reference land pattern layout (reference IPC7351 QFN50P400X400X80-25W6M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Branding scale and appearance at supplier discretion.

Figure 7: Package ES, 24-Contact QFN with Exposed Pad

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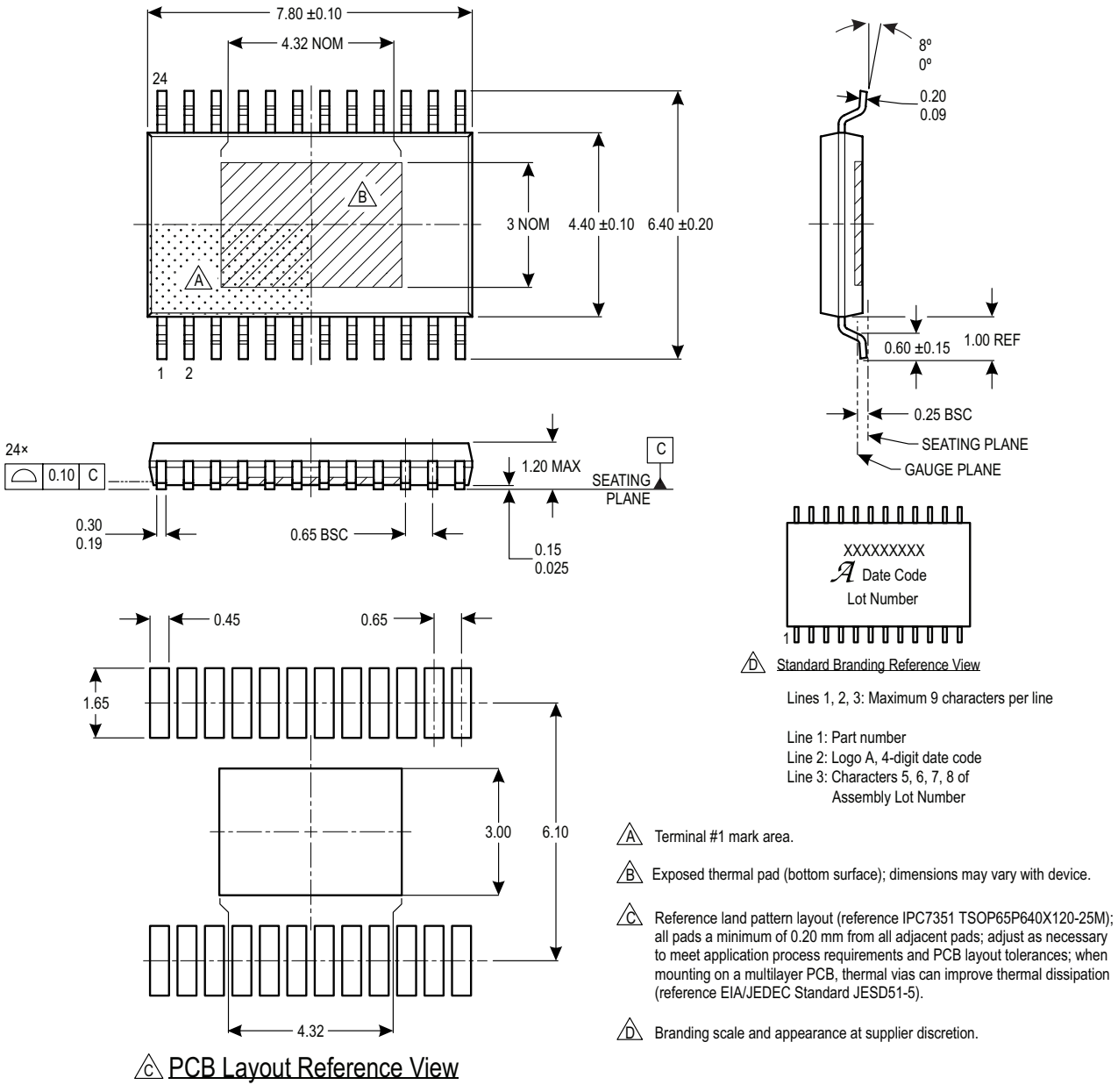
For Reference Only – Not for Tooling Use
(Reference Allegro DWG-0000379, Rev. 3 and JEDEC MO-153ADT)
NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Ⓒ PCB Layout Reference View

Ⓓ Standard Branding Reference View

Lines 1, 2, 3: Maximum 9 characters per line

Line 1: Part number
Line 2: Logo A, 4-digit date code
Line 3: Characters 5, 6, 7, 8 of Assembly Lot Number

Ⓐ Terminal #1 mark area.

Ⓑ Exposed thermal pad (bottom surface); dimensions may vary with device.

Ⓒ Reference land pattern layout (reference IPC7351 TSOP65P640X120-25M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5).

Ⓓ Branding scale and appearance at supplier discretion.

Figure 8: Package LP, 24-Lead TSSOP with Exposed Pad

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Revision History

Number	Date	Description
–	December 13, 2018	Initial release
1	January 24, 2019	Updated Motor PWM Frequency (page 4)
2	June 2, 2020	Corrected delay_start address (page 12) and minor editorial updates
3	July 28, 2021	Updated Programming EEPROM register descriptions (page 14); updated EEPROM Commands section (page 15); updated ES package drawing (page 17)
4	August 8, 2022	Updated LP package drawing (page 18)
5	August 19, 2024	Updated programming registers to uppercase according to the current standard, and minor editorial updates.

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