

## Automotive-Grade, Low-EMI, 1.5 A PWM Dimmable Synchronous Buck LED Module

### FEATURES AND BENEFITS

- Automotive AEC-Q100 qualified
- Supply voltage 4.5 to 36 V, maximum 40 V
- Complete 1.5 A output compact LED driver
- Integrated inductor, VIN and boot capacitors
- Ultra-low EMI architecture,  $f_{SW} > 2$  MHz
- Spread spectrum for improved EMC
- Integrated high-side and low-side MOSFETs: 80 m $\Omega$  / 60 m $\Omega_{TYP}$ , 90% efficiency at 1 A
- 5 V, 14 mA LDO regulator for peripheral circuits
- Dimming via external PWM or EN pin
- Programmable internal PWM dimming
- Analog dimming for brightness calibration and thermal foldback
- Low power shutdown (1  $\mu$ A typical)
- High side current sense,  $\pm 3\%$  accuracy
- Fault flag output
- LED open fault mask setting for low VIN operation
- Undervoltage lockout (UVLO) and thermal shutdown protection
- Robust protection against:
  - Adjacent pin-to-pin short
  - Pin-to-ground short
  - Component open/short faults

### PACKAGE:



*Not to scale*

32-pin QFN  
4 mm × 6 mm × 2.1 mm  
with wettable flank  
(suffix NB)

### DESCRIPTION

The APM80904 is a complete synchronous buck switching regulator module that provides constant current output to drive high-power LEDs. It integrates both high-side and low-side N-channel switches, inductor, high frequency VIN and boot capacitors. A true average current is output using a cycle-by-cycle, controlled on-time method.

Output current is user-selectable by an external current sense resistor. Output voltage automatically adjusts to the LED string voltage to ensure optimal system efficiency.

LED dimming is accomplished by a direct logic input pulse-width modulation (PWM) signal at the PWM pin while EN is enabled. Alternatively, applying a PWM signal at the EN pin while the PWM pin is high provides “chopped battery” PWM dimming for legacy control modules. Additionally, the APM80904 includes programmable internal dimming.

The analog dimming input (ADIM pin) can be used to calibrate the LED current or implement thermal foldback in conjunction with an external NTC thermistor.

The APM80904 is provided in a compact, thermally enhanced 4 mm × 6 mm × 2.1 mm QFN-32 package with wettable flanks.

### APPLICATIONS:

- Daytime running lights
- Front and rear fog lights
- Turn/stop lights
- Map light
- Dimmable interior lights
- Puddle lights

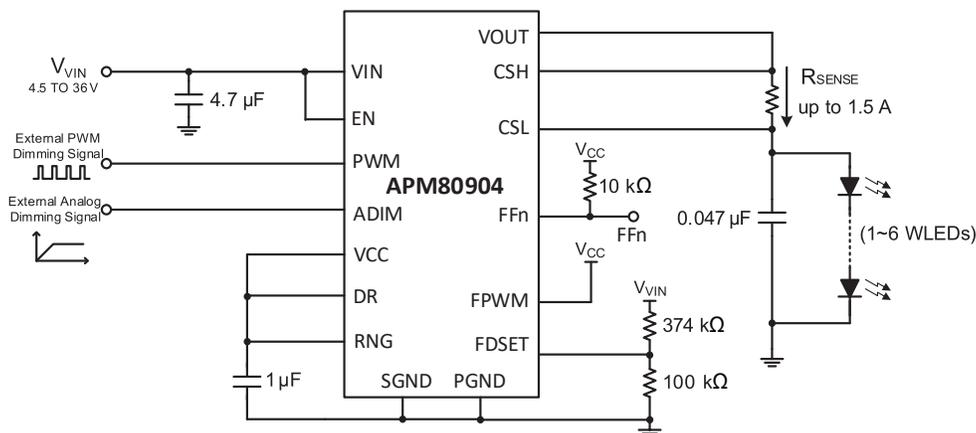


Figure 1: APM80904 Typical Application Circuit

## SELECTION GUIDE

Part Number	Package	Packing
APM80904KNBATR	32-pin 4 mm × 6 mm × 2 mm QFN with wettable flanks	3000 pieces per 13-inch reel



## SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	$V_{VIN}$		-0.3 to 40	V
EN Voltage	$V_{EN}$		-0.3 to $V_{VIN} + 0.3$	V
Current Sense Voltages	$V_{CSH}, V_{CSL}$		-0.3 to $V_{VIN} + 0.3$	V
DR Pin	$V_{DR}$	DR pin voltage must not be higher than $V_{VCC}$ even when device is off ( $V_{VCC} = 0$ V)	-0.3 to $V_{VCC} + 0.3$	V
VCC, ADIM, RNG, FDSET, FFn, PWM, and FPWM Terminal Voltages	$V_{VCC}, V_{ADIM}, V_{RNG}, V_{FDSET}, V_{FFn}, V_{PWM}, V_{FPWM}$		-0.3 to 7	V
Bootstrap Voltage	$V_{BOOT}$		-0.3 to $V_{VIN} + 8$	V
Switching Voltage	$V_{SW}$	Continuous	-0.3 to $V_{VIN} + 0.3$	V
		Pulsed, $t < 50$ ns	-1 to $V_{VIN} + 3$	V
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

### THERMAL CHARACTERISTICS\*: May require derating at maximum conditions; see application section for optimization

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance (Junction to Ambient)	$R_{\theta JA}$	On 4-layer PCB based on JEDEC standard.	30	°C/W
Package Thermal Resistance (Junction to Pad)	$R_{\theta JP}$		2	°C/W

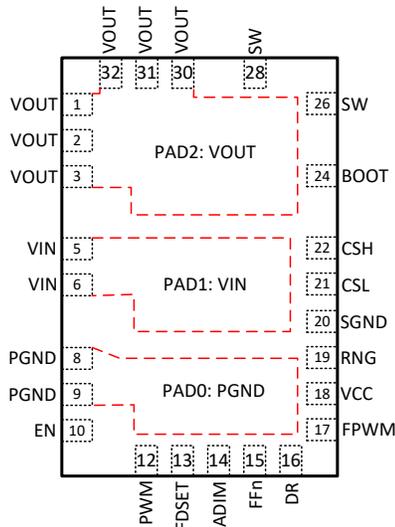
\*Additional thermal information available on the Allegro™ website.

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## PINOUT DIAGRAM AND TERMINAL LIST

QFN-32 Pinout Diagram



Terminal List

Number	Name	Function
1, 2, 3, 30, 31, 32	VOUT	Output of converter. Sources LED current.
5, 6	VIN	Input voltage supply for power stage.
8, 9	PGND	Power ground terminal.
10	EN	Enable pin for all IC functions. EN pin can also be used for PWM dimming when PWM pin is High.
12	PWM	Logic input for PWM dimming: When PWM = Low, LED is OFF; if PWM = High and EN = High, LED is ON. For internal PWM dimming mode, no signal is needed at this pin.
13	FDSET	Sets LED Open fault mask threshold. Connect to a voltage divider formed between VIN and SGND. When VIN is low, resulting in FDSET below the internal reference, LED Open Fault detection will be masked.
14	ADIM	Analog dimming control voltage input.
15	FFn	Open-drain output that is pulled low when a fault occurs. Connect through an external pull-up resistor to the desired logic level.
16	DR	A voltage applied to this pin programs the duty cycle for the internal PWM dimming generator. Tying DR to VCC disables the internal PWM dimming generator.
17	FPWM	For internal PWM mode, connect a resistor to SGND to set the internal PWM dimming frequency. For external PWM, FPWM pin can be either left open or tied to VCC.
18	VCC	Internal IC bias regulator output. Connect 1 $\mu$ F MLCC to PGND. Can be used to supply up to 14 mA to an external load.
19	RNG	Output current range select pin. Connect to VCC or GND to select high or low output current range.
20	SGND	Signal ground terminal.
21	CSL	Current Sense (negative end) feedback input for LED current.
22	CSH	Current Sense (positive end) feedback input for LED current.
24	BOOT	High-side gate driver bootstrap terminal (for test only). Leave this pin disconnected.
26, 28	SW	Switched terminal (for test only). Leave this pin disconnected.
PAD0	PAD	Exposed pad for enhanced thermal dissipation; connect to PGND plane.
PAD1	PAD	Exposed pad for enhanced thermal dissipation; connect to VIN.
PAD2	PAD	Exposed pad for enhanced thermal dissipation; connect to VOUT.

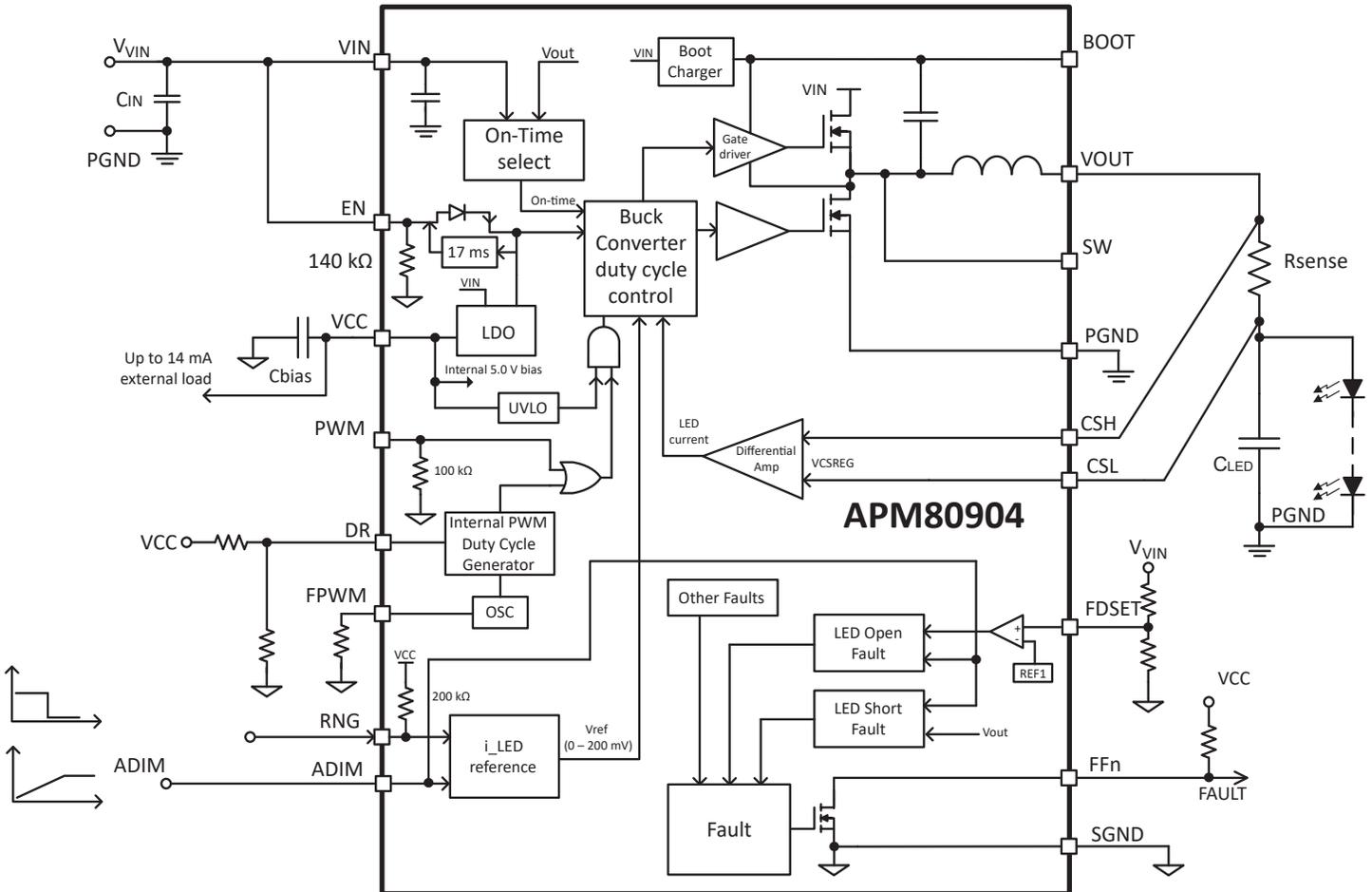


Figure 2: Functional Block Diagram

**ELECTRICAL CHARACTERISTICS:** Valid at  $V_{VIN} = 12\text{ V}$ ,  $V_{VOUT} = 6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values at  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Input Supply Voltage	$V_{VIN}$		4.5	–	36	V	
$V_{VIN}$ Undervoltage Lockout Threshold	$V_{UVLO(ON)}$	$V_{VIN}$ increasing	–	–	4.31	V	
$V_{VIN}$ Undervoltage Lockout Hysteresis	$V_{UVLO(HYS)}$	$V_{VIN}$ decreasing	100	–	300	mV	
VIN Pin Supply Current	$I_{VIN}$	$V_{CSH} - V_{CSL} = 0.5\text{ V}$ , $V_{EN} = V_{IH(EN)}$ , $V_{PWM} = V_{IH(PWM)}$	–	5	–	mA	
VIN Pin Shutdown Current [1]	$I_{IN(SD)}$	$V_{EN} = V_{IL(EN)}$ , $T_J \leq 85^\circ\text{C}$ , $V_{SW} = 0\text{ V}$	–	1	10	$\mu\text{A}$	
Output Current Sense Common Mode Voltage (measured at CSL pin) [1]	$V_{VOUT}$	$V_{VIN} = 36\text{ V}$	2.65	–	25	V	
Buck Switch Current Limit Threshold	$I_{SW(LIM)}$		2.5	3.1	3.6	A	
Buck High-Side Switch On-Resistance	$R_{DSON(HS)}$	$V_{BOOT} = V_{VIN} + 4.3\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_{SW} = 0.5\text{ A}$	–	0.08	–	$\Omega$	
Buck Low-Side Switch On-Resistance	$R_{DSON(LS)}$	$V_{BOOT} = 4.3\text{ V}$ , $T_J = 25^\circ\text{C}$ , $I_{SW} = 0.5\text{ A}$	–	0.06	–	$\Omega$	
Switching Minimum Off-Time	$t_{OFF(MIN)}$	$V_{CSH} - V_{CSL} = 0\text{ V}$	50	65	80	ns	
Switching Minimum On-Time	$t_{ON(MIN)}$		65	80	95	ns	
Selected On-Time	$t_{ON}$	$V_{VIN} = 12\text{ V}$ , $V_{VOUT} = 6\text{ V}$	–	250	–	ns	
$t_{ON}$ Spread Spectrum Range	$f_{SW(SWEEP)}$		–	$\pm 5$	–	%	
Spread Spectrum Modulation Frequency	$f_{SW(MOD)}$		–	11.5	–	kHz	
<b>REGULATION COMPARATOR AND ERROR AMPLIFIER</b>							
Load Current Sense Regulation Threshold at 100% [2]	$V_{CSREG}$	$V_{CSH} - V_{CSL}$ decreasing, SW turns on, ADIM tied to VCC	RNG = High	194	200	206	mV
			RNG = Low	96	100	104	mV
CSH Input Sense Current [3]	$I_{CSH}$	$V_{CSH} - V_{CSL} = 0\text{ V}$	–	170	–	$\mu\text{A}$	
CSL Input Sense Current	$I_{CSL}$	$V_{CSH} - V_{CSL} = 0\text{ V}$	–	170	–	$\mu\text{A}$	
<b>INTERNAL LINEAR REGULATOR</b>							
VCC Regulated Output	$V_{VCC}$	$0\text{ mA} < I_{VCC} < 14\text{ mA}$ , $V_{VIN} > 6\text{ V}$	4.85	5.0	5.15	V	
VCC Dropout Voltage	$V_{LDO}$	Measure $V_{VIN} - V_{VCC}$ : $V_{VIN} = 4.8\text{ V}$ , $I_{VCC} = 14\text{ mA}$	–	0.3	0.6	V	
VCC Current Limit	$i_{VCC(LIM)}$	$V_{VCC} \geq 4.35\text{ V}$	20	–	–	mA	
VCC Undervoltage Lockout	$V_{VCC(UVLO)}$	Rising	3.6	3.9	4.15	V	
	$V_{VCC(UVLOHYS)}$	Hysteresis	180	230	280	mV	
<b>EN INPUT</b>							
Maximum IC Turn Off Delay	$t_{OFF(DELAY)}$	Measured while PWM dimming signal applied at EN keeping low and exceeding $t_{OFF(DELAY)}$ results in shutdown	10	17	–	ms	
Logic High Voltage	$V_{IH(EN)}$	$V_{EN}$ increasing	1.8	–	–	V	
Logic Low Voltage	$V_{IL(EN)}$	$V_{EN}$ decreasing	–	–	0.4	V	
Enable Pin Pull-Down Resistance	$R_{EN(PD)}$		–	140	–	k $\Omega$	

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**ELECTRICAL CHARACTERISTICS (continued):** Valid at  $V_{VIN} = 12\text{ V}$ ,  $V_{VOUT} = 6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values at  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>PWM INPUT</b>							
PWM Logic High	$V_{IH(PWM)}$	$V_{PWM}$ increasing	1.8	–	–	V	
PWM Logic Low	$V_{IL(PWM)}$	$V_{PWM}$ decreasing	–	–	1.2	V	
PWM Pin Pull-Down Resistance	$R_{PWM(PD)}$		–	100	–	k $\Omega$	
<b>PWM DIMMING: INTERNAL</b>							
Internal PWM Dimming Frequency	$f_{PWM}$	External $R_{FPWM} = 69.8\text{ k}\Omega$ from FPWM pin to GND	180	200	225	Hz	
Internal PWM Duty Cycle	$D_{PWM(5)}$	$V_{DR}$ driven by resistor divider from VCC, $V_{DR} / V_{VCC} = 0.034$ , $f_{PWM} = 200\text{ Hz}$	4.5	5	5.5	%	
	$D_{PWM(90)}$	$V_{DR}$ driven by resistor divider from VCC, $V_{DR} / V_{VCC} = 0.642$ , $f_{PWM} = 200\text{ Hz}$	87	90	93	%	
	$\Delta D_{PWM}$	$\Delta V_{DR} = 36\text{ mV}$ , $f_{PWM} = 200\text{ Hz}$ [4]	–	1	–	%	
<b>RNG INPUT</b>							
RNG Logic High	$V_{IH(RNG)}$	$V_{RNG}$ increasing	1.8	–	–	V	
RNG Logic Low	$V_{IL(RNG)}$	$V_{RNG}$ decreasing	–	–	0.8	V	
RNG Pull-Up Resistance to VCC	$R_{RNG(PU)}$		–	200	–	k $\Omega$	
<b>ANALOG DIMMING INPUT</b>							
Input Voltage For >94% LED Current	$V_{ADIM(H)}$	$V_{CSH} - V_{CSL} = V_{CSREG}$	RNG = High	1.5	–	–	V
Input Voltage For >90% LED Current	$V_{ADIM(L)}$	$V_{CSH} - V_{CSL} = V_{CSREG}$	RNG = Low	1.0	–	–	V
Regulation Threshold at 50% Analog Dimming	$V_{CSREG(50)}$	$V_{ADIM} = 0.9\text{ V}$	RNG = High	–	100	–	mV
		$V_{ADIM} = 0.65\text{ V}$	RNG = Low	–	50	–	mV
Regulation Threshold at 20% Analog Dimming	$V_{CSREG(20)}$	$V_{ADIM} = 0.6\text{ V}$	RNG = High	38	40	42	mV
<b>FAULT</b>							
ADIM Threshold for LED Open/Short Fault Detection	$V_{ADIM(FAULT)}$	$V_{ADIM}$ rising		475	500	525	mV
Output Voltage Low Threshold for LED Short Fault Detection	$V_{OUT(SHORT)}$	$V_{VOUT}$ falling, $V_{ADIM} = 5\text{ V}$		1.3	1.5	1.7	V
LED Open Fault Enable Reference	$V_{REF1}$			2.352	2.4	2.448	V
LED Open Fault Current Threshold	$V_{CS(OPEN)}$	$V_{CSREG} = 200\text{ mV}$ start falling (PWM duty = max), $V_{ADIM} = V_{VCC}$ , $V_{FDSET} = V_{VCC}$		35	65	95	mV
LED Open Fault Current Hysteresis [1]	$V_{CS(OPENHYS)}$	$V_{CSREG} = 200\text{ mV}$ start falling (PWM duty = max), $V_{ADIM} = V_{VCC}$ , $V_{FDSET} = V_{VCC}$		8	14	24	mV
Fault Deglitch Timer	$t_{FDG}$			30	50	65	$\mu\text{s}$
Fault Mask Timer	$t_{MASK}$			70	100	130	$\mu\text{s}$
FFn Pull-Down Voltage	$V_{FAULT(PD)}$	Fault condition asserted, pull-up current = 1 mA		–	–	0.4	V
FFn Pin Leakage Current	$I_{FAULT(LKG)}$	Fault condition cleared, pull-up to 5 V		–	–	1	$\mu\text{A}$
FFn Rising Timer [1]	$t_{RISE}$	Transition time Fault pin takes from Low to High		–	–	10	$\mu\text{s}$

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**ELECTRICAL CHARACTERISTICS (continued):** Valid at  $V_{VIN} = 12\text{ V}$ ,  $V_{VOUT} = 6\text{ V}$ ,  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , typical values at  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>FAULT (continued)</b>						
FFn Falling Timer [1]	$t_{FALL}$	Transition time Fault pin takes from High to Low	–	–	10	$\mu\text{s}$
Cool Down Timer for Fault Retry	$t_{RETRY}$		–	1	–	ms
<b>THERMAL SHUTDOWN</b>						
Thermal Shutdown Threshold [1]	$T_{SD}$		150	165	180	$^\circ\text{C}$
Thermal Shutdown Hysteresis [1]	$T_{SD(HYS)}$		–	25	–	$^\circ\text{C}$

[1] Determined by design and characterization. Not production tested.

[2] In test mode, a ramp signal is applied between CSH and CSL pins to determine the  $V_{CSH} - V_{CSL}$  regulation threshold voltage. In actual application, the average  $V_{CSH} - V_{CSL}$  voltage is regulated at  $V_{CSREG}$  regardless of ripple voltage.

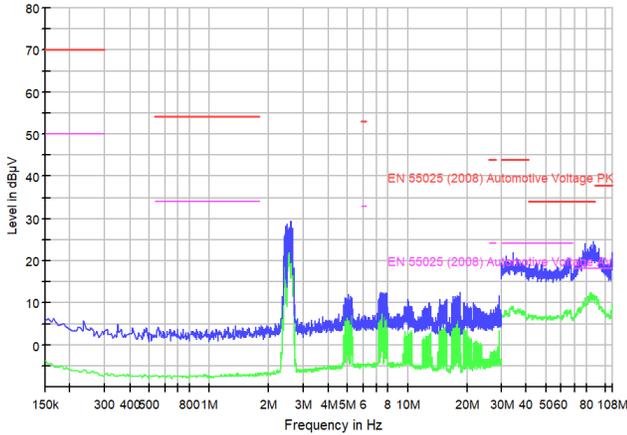
[3] Negative current is defined as coming out of (sourcing) the specified device pin or node.

[4] When  $V_{DR}$  change is less than  $\Delta V_{DR}$  specified here, the duty cycle is NOT changed.

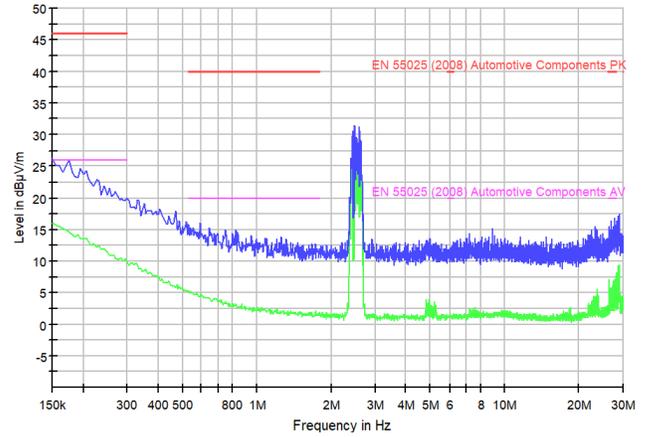
## EMC PERFORMANCE CHARACTERISTICS

$V_{VIN} = 12\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , Load = 2 series white LEDs,  $I_{LED} = 0.5\text{ A}$ , with EMI filters, as shown in Figure 3

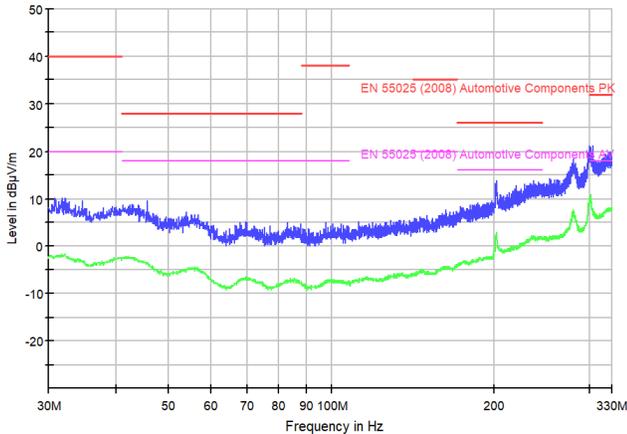
EN55025/CISPR25 Class 5 Peak and Average Conducted Emissions (150 kHz to 108 MHz)



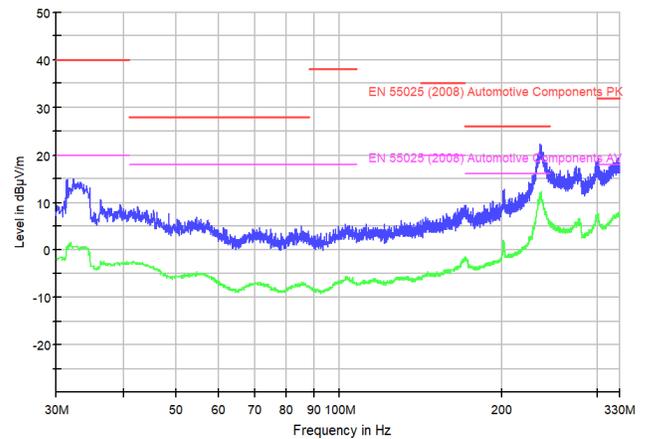
EN55025/CISPR25 Class 5 Peak and Average Rod Antenna Radiated Emissions (150 kHz to 30 MHz)



EN55025/CISPR25 Class 5 Peak and Average Biconical Radiated Emissions (Horizontal, 30 MHz to 330 MHz)



EN55025/CISPR25 Class 5 Peak and Average Biconical Radiated Emissions (Vertical, 30 MHz to 330 MHz)



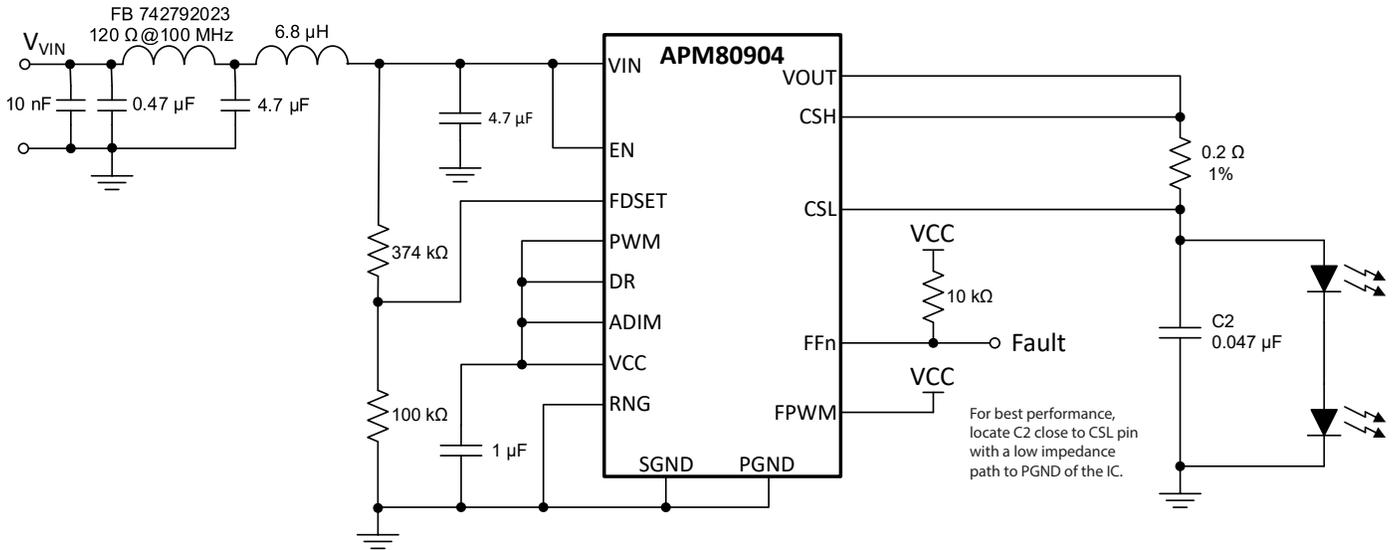
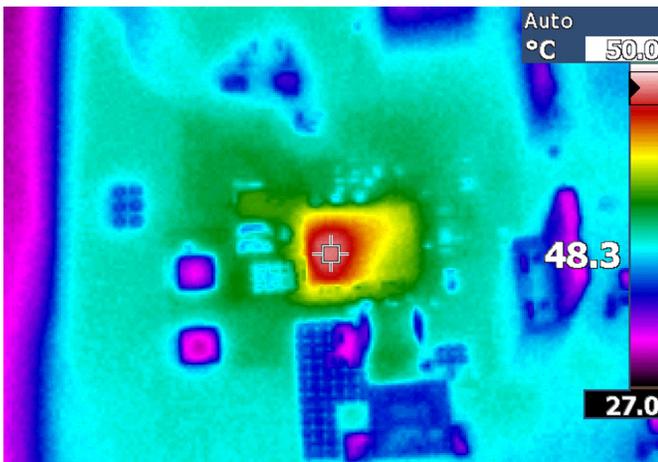


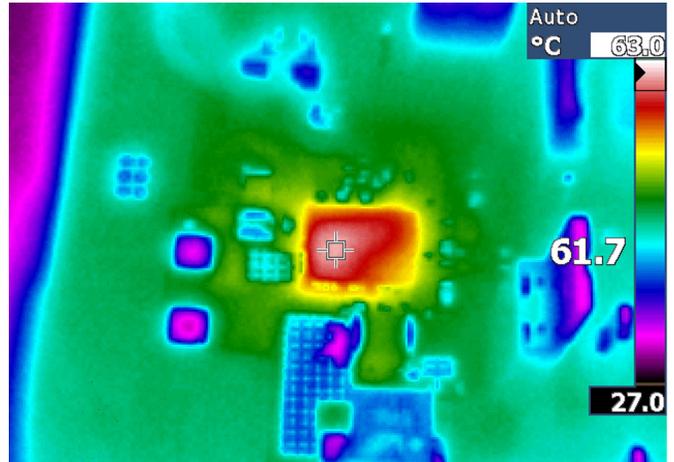
Figure 3: EMC test circuit

## THERMAL PERFORMANCE CHARACTERISTICS

$V_{VIN} = 12\text{ V}$ , 2 WLEDs / 1 A,  $\eta = 89\%$



$V_{VIN} = 24\text{ V}$ , 2 WLEDs / 1 A,  $\eta = 82\%$



## FUNCTIONAL DESCRIPTION

The APM80904 is a complete low-EMI synchronous buck regulator module designed for driving a high-current LED string. The operational  $V_{VIN}$  range is from 4.5 to 36 V, and it can withstand up to 40 V input transients. This module can regulate LED current from 200 mA to 1.5 A, depending on thermal management. It uses average current mode control to maintain constant LED current for consistent brightness.

The LED current level is easily programmable by selection of an external sense resistor, with a value determined as follows:

$$R_{SENSE} = V_{CSREG} / i_{LED}$$

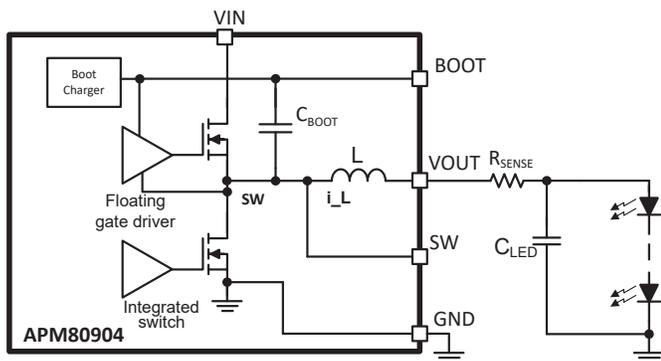
There are two options of  $V_{CSREG}$  for high or low output current range. If output LED current is between 0.6 and 1.5 A, the RNG pin should be connected to logic high signal (VCC) or left open. If output LED current is between 200 and 600 mA, the RNG pin should be connected to GND for reduced power dissipation.

**Table 1: RNG setting for suggested LED Output Current Range**

RNG	$V_{CSREG}$	$i_{LED}$
High	200 mV (typical)	0.6 to 1.5 A
Low	100 mV (typical)	200 to 600 mA

### Synchronous Regulation

The APM80904 integrates an N-channel DMOS as the low-side and high-side switches to implement synchronous regulation for LED drivers, as shown in Figure 4.



**Figure 4: Synchronous Buck LED Driver**

The synchronous configuration can effectively pull SW to GND by forcing the low-side synchronous switch on even with small inductor current. Therefore, the internal boot capacitor can be

charged normally every switch cycle to ensure the normal operation of the buck LED driver.

An extremely low switch deadtime ensures that minimal power is dissipated during the high-side switch turn-on transition. This low deadtime also reduces EMI. The integrated VIN to PGND capacitor significantly reduces the high-current input loop length, greatly reducing the radiated emissions.

### Switching Frequency

The APM80904 operates in fixed on-time mode during switching. The on-time (and hence switching frequency) is programmed by an internal circuit to keep switching frequency at around 2 MHz across the operating range. Note that  $t_{ON}$  must be greater than  $t_{ON(MIN)}$ , which is 80 ns (typical). If  $V_{VIN}$  is high enough to reach  $t_{ON(MIN)}$ , the APM80904 will maintain  $t_{ON(MIN)}$  even when  $V_{VIN}$  increases further.

$$t_{ON} = \max[t_{ON(MIN)}, 1/(2 \text{ MHz}) \times (V_{VOUT} / V_{VIN})]$$

The switching frequency of the converter may vary with output current due to voltage drop on the switches and inductor when conducting.

To minimize the peaks of switching frequency harmonics in EMC measurement, a spread spectrum feature is implemented. The spread spectrum range is internally set at  $\pm 5\%$ . The actual switching frequency is swept linearly between  $0.95 \times f_{SW}$  and  $1.05 \times f_{SW}$ , where  $f_{SW}$  is the programmed switching frequency. The rate of modulation for  $f_{SW}$  is fixed internally at 11.5 kHz.

### Enable and Dimming

The APM80904 is activated when a logic-high signal is applied to the EN (enable) pin and  $V_{VIN}$  is above UVLO threshold, 4.31 V. The buck converter ramps up the LED current to a target level set by  $R_{SENSE}$  when PWM pin = High.

The EN pin is high-voltage tolerant and can be directly connected to a power supply. However, if  $V_{EN}$  is higher than  $V_{VIN}$  at any time, a series resistor (10 k $\Omega$ ) is required to limit the current flowing into the EN pin. This resistor is helpful in preventing EN from damage in case of reverse battery connection. This series resistor is not necessary if EN is driven from a logic input.

The PWM pin is a logic input pin and is internally pulled down through a resistor. If the APM80904 is enabled before the PWM signal is asserted high, the output remains off until PWM signals start.

EN and PWM pins function as shown in Table 2.

**Table 2: EN and PWM Pin Function**

EN pin	PWM pin	VCC	LED
High	Low/Open	ON	OFF
High	High	ON	ON
Low ( $<t_{OFF(DELAY)}$ )	x	ON	OFF
Low ( $>t_{OFF(DELAY)}$ )	x	Shutdown	

When the EN pin is forced from high to low, the LED current is turned off, but the IC remains in standby mode for up to at least 10 ms. If EN goes high again within this period, the LED current is turned on immediately if PWM pin is high. If EN pin is low for more than  $t_{OFF(DELAY)}$ , the IC enters shutdown mode to reduce power consumption. The next high signal on EN will initialize a full startup sequence, which includes a startup delay of approximately 150  $\mu$ s. This startup delay is not present during PWM operation.

Active dimming of the LED is achieved with 2 options: by sending a PWM (pulse-width modulation) signal to the EN pin while PWM = High, or by sending a dimming PWM signal to the PWM pin while EN = High. The resulting LED brightness is proportional to the duty cycle of the applied PWM signal. A practical range for PWM dimming frequency is between 100 Hz (period 10 ms) and 2 kHz.

If the PWM dimming signal at the PWM pin is low when the EN pin is high, the LED will be off immediately, and the IC remains enabled, waiting for the next PWM pulse. The internal LDO is still on and can provide bias to the internal and external circuits.

### PWM Dimming Ratio

The brightness of the LED string can be changed by adjusting the PWM duty cycle as follows:

$$\text{Dimming ratio} = \text{PWM on-time} / \text{PWM period}$$

For example, by selecting a PWM period of 5 ms (200 Hz PWM frequency) and a PWM on-time of 5  $\mu$ s, a dimming ratio of 0.1% can be achieved. This is sometimes referred to as “1000:1 dimming.”

In an actual application, the minimum dimming ratio is determined by various system parameters, including:  $V_{VIN}$ ,  $V_{VOUT}$ , inductance, LED current, and PWM frequency. The device is easily capable of PWM on-time as short as 5  $\mu$ s; however, if fault flag for open/short LED detection is required, it should be above 130  $\mu$ s due to the fault mask timer.

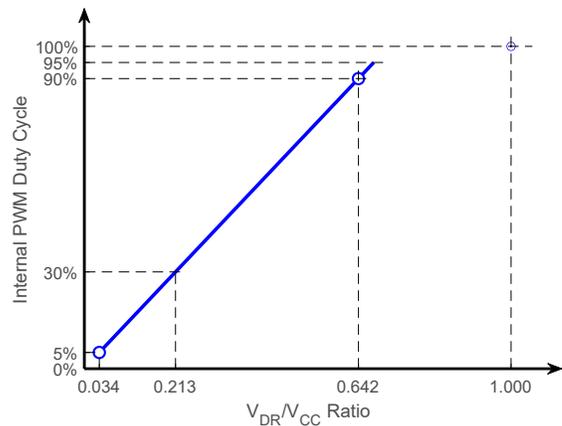
### Internal PWM Dimming

In addition to external PWM dimming through the PWM pin, the APM80904 can generate an internal PWM dimming signal in stand-alone mode. Frequency of the internal PWM signal can be set by connecting a resistor between FPWM pin and GND, as given by the following equation:

$$R_{FPWM} = 14,000 / f_{PWM}$$

with  $f_{PWM}$  in Hz, and  $R_{FPWM}$  in k $\Omega$ .

This frequency can be between 200 Hz and 1 kHz. The duty cycle of the internal PWM signal is linearly proportion to the voltage at DR (Dimming Ratio) pin. This is illustrated in Figure 5.



**Figure 5: Variation of Internal PWM Duty Cycle with respect to DR Pin Voltage**

It should be noted that the internal PWM duty cycle depends on the ratio between  $V_{VCC}$  and  $V_{DR}$ . The voltages shown in the chart are with  $V_{VCC} = 5$  V. For better accuracy, derive the DR pin voltage using a resistor divider connected between  $V_{CC}$  and GND.

A practical range of internal PWM duty cycle is between 5% ( $V_{DR}/V_{CC}$  ratio = 0.034) and 90% ( $V_{DR}/V_{CC}$  ratio = 0.642). Operation with internal PWM duty cycle up to 95% is acceptable but internal PWM duty cycles between 95% and 100% should be avoided. For operation with PWM at 100% duty cycle, tie DR to  $V_{CC}$  and hold PWM high.

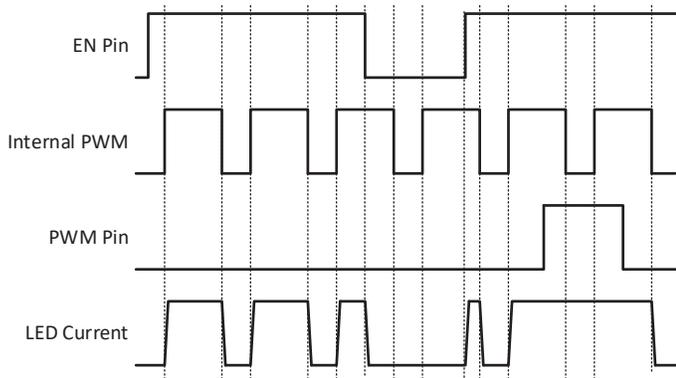
The following equation can be used to calculate the  $V_{DR}/V_{CC}$  ratio for a given target PWM value:

$$V_{DR} / V_{CC} \text{ Ratio} = (0.007153 \times \text{TargetPWM}) - 0.00176$$

where TargetPWM is in %.

To disable internal PWM generation, tie the DR pin to the  $V_{CC}$  pin. (Do NOT leave DR pin floating or connected to GND.) The FPWM pin can be either left open or tied to  $V_{CC}$ . Note that at

any time during stand-alone PWM dimming mode, the response to the PWM pin and EN pin differs. If the EN pin goes low, the LED is turned off immediately. If the PWM pin goes high, the LED remains on no matter the state of the internal PWM signal. This is illustrated in Figure 6.



**Figure 6: LED Current when both Internal and External PWM Dimming Signals are applied**

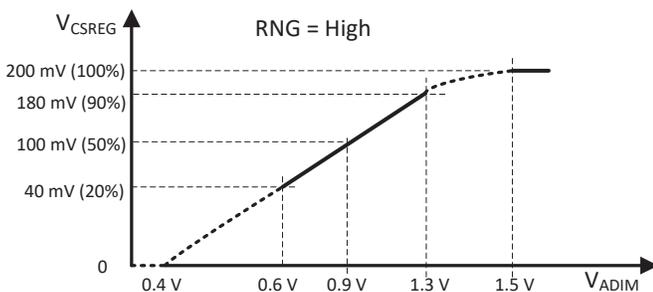
### Analog Dimming

In addition to PWM dimming, the APM80904 also provides an analog dimming feature.

If RNG = High, when  $V_{ADIM}$  is over 1.5 V, the LED current is at 100% level (as defined by the sense resistor  $R_{SENSE}$ ). When  $V_{ADIM}$  is between 0.6 and 1.3 V, the LED current changes linearly with  $V_{ADIM}$  from 20% to 90%. Within this range, the LED current reference voltage  $V_{CS}$  can be calculated as:

$$V_{CSREG} = (V_{ADIM} - 0.4 \text{ V}) / 5$$

This is shown in Figure 7.



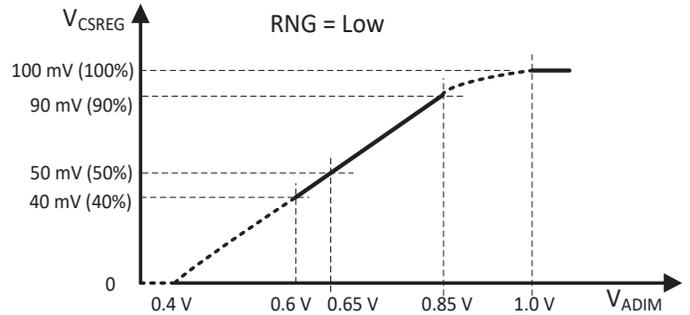
**Figure 7: ADIM Pin Voltage controls the LED Current Reference Voltage with RNG = High**

If RNG = Low, when  $V_{ADIM}$  is over 1.0 V, the LED current is at 100% level (as defined by the sense resistor  $R_{SENSE}$ ). When  $V_{ADIM}$  is between 0.6 to 0.85 V, the LED current changes linearly with  $V_{ADIM}$  from 40% to 90%. Within this range, LED current

reference voltage  $V_{CS}$  can be calculated as:

$$V_{CSREG} = (V_{ADIM} - 0.4 \text{ V}) / 5$$

This is shown in Figure 8.



**Figure 8: ADIM Pin Voltage controls the LED Current Reference Voltage with RNG = Low**

For accurate LED current level control, the APM80904 should operate with ADIM in the linear region of 0.6 to 1.3 V for RNG = High and 0.6 to 0.85 V for RNG = Low.

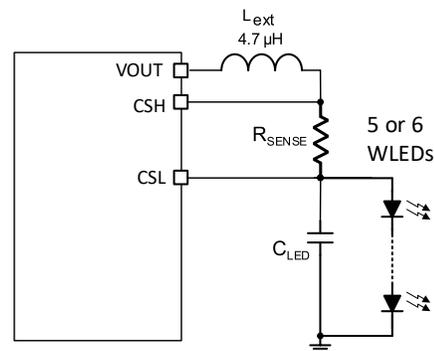
Note that the allowable voltage across the sensing resistor  $R_{SENSE}$  should lie within the range of  $-50$  to  $250$  mV to avoid saturating the internal current amplifiers. The expected minimum and maximum  $v_{CS}$  can be estimated by the following equations:

$$\min v_{CS} = [I_{LED} - \frac{(V_{IN} - V_{OUT})V_{OUT}}{19.6 \times V_{IN}}] \times R_{SENSE}$$

$$\max v_{CS} = [I_{LED} + \frac{(V_{IN} - V_{OUT})V_{OUT}}{19.6 \times V_{IN}}] \times R_{SENSE}$$

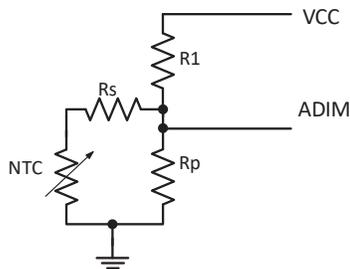
where  $I_{LED}$  is the expected LED output current.

In order to extend operation beyond  $V_{CS}$  limits, an external inductor of  $4.7 \mu\text{H}$  can be added to ensure proper operation with 5 or 6 WLEDs with  $V_{IN}$  up to 36 V, as shown in Figure 9.



**Figure 9: External inductor is added for 5 or 6 WLEDs operation with  $V_{IN}$  up to 36 V**

The ADIM pin can be used in conjunction with PWM dimming to provide wider LED dimming range over 1000:1. In addition, the IC can provide thermal foldback protection by using an external NTC (negative temperature coefficient) thermistor, as shown in Figure 10.



**Figure 10: Using an External NTC Thermistor to Implement Thermal Foldback**

Based on the equation below, ADIM voltage will be reduced to lower the LED current for less LED power when temperature rise due to LED heating causes the resistance reduction of NTC thermistor.

$$V_{ADIM} = V_{VCC} \times \left( \frac{[(R_{NTC}(T) + R_s) // R_p]}{[(R_{NTC}(T) + R_s) // R_p + R_1]} \right)$$

### Minimum and Maximum Output Voltages

With a typical minimum  $t_{OFF}$  of 100 ns, the maximum duty cycle is approximately 80%. So for  $V_{VIN} = 18$  V, the maximum output is approximately 14.4 V (based on the simplified equation of  $V_{VOUT} = V_{VIN} \times D$ ).

With a typical minimum  $t_{ON}$  of 80 ns, the minimum duty cycle is approximately 16%. That means with  $V_{VIN} = 18$  V, the theoretical minimum  $V_{VOUT}$  is just 1.8 V. However, the internal current sense amplifier is only designed to operate down to  $V_{VOUT} = 2.65$  V. Operating with  $V_{VOUT} < 2.65$  V will result in reduced current sense accuracy.

If the required output voltage is lower than that permitted by the minimum  $t_{ON}$ , the controller will automatically extend the  $t_{OFF}$ , in order to maintain the correct duty cycle. The result is that the switching frequency is reduced, in order to keep the LED current in regulation.

If the LED string is completely shorted ( $V_{VOUT} < 1.5$  V typical), the controller will continue to switch at minimum  $t_{ON}$  and will not enter Hiccup mode.

### Thermal Budgeting

The APM80904 can supply a 1.5 A current to the LED string.

However, depending on the duty cycle, the conduction loss in the high-side and low-side switches, and loss in the inductor may cause the package to reach the thermal shutdown threshold. Therefore, care must be taken to ensure the total power loss of the APM80904 is within budget. For example, if the maximum temperature rise allowed is  $\Delta T = 60^\circ\text{C}$  at the device case surface, then the maximum power dissipation of the module is 2 W when mounted to Allegro's 4-layer PCB which has an  $R_{\theta JA}$  of  $30^\circ\text{C/W}$ . When considering the switching and conduction losses within the APM80904, the estimated maximum LED current is limited to 1.5 A.

### Fault Handling

The APM80904 is designed to handle the following faults:

- Pin-to-ground short
- Pin-to-neighboring pin short
- Pin open
- Opens/shorts on some external components
- Output short to ground

### $R_{SENSE}$ Shorted Fault

$R_{SENSE}$  short detection detects shorts across the  $R_{SENSE}$  resistor, but is limited to hard shorts (very low impedance). A weak short will effectively reduce the value of the  $R_{SENSE}$  resistance, resulting in greater output current. If the inductor current limit is not reached, this will not register as a short, a fault will not be asserted, and the IC will continue to regulate at higher than programmed LED current.

### LED Open/Output Short Faults

The A80904 can detect an open LED string or output short fault and assert the fault flag by pulling the FFn pin low. The LED open fault is detected by monitoring the voltage,  $V_{CSREG}$ , across the current sense resistor while the PWM signal is high, and an LED short is detected when  $V_{OUT} < 1.5$  V while  $V_{ADIM} > 500$  mV. The fault must remain present for more than the fault deglitch time,  $t_{FDG}$ , for the A80904 to act on fault condition. A fault mask timer,  $t_{MASK}$ , starts at the rising edge of each PWM cycle to mask faults when the PWM cycle starts. If the PWM on-time is less than the fault mask timer, the fault flag will not assert. The fault flag state is latched when PWM goes low to maintain its high or low state until the next PWM rising edge.

If an open LED fault is detected, the regulator will enter hiccup mode and assert the fault flag. If the open LED fault condition is removed, the fault flag is released after the next PWM rising edge and completion of either the hiccup timer or current to regulation timer; see cases 5, 6, and 7 in the LED Open/Short fault timing diagrams. The open LED fault is masked and will not assert the fault flag if either of two conditions is met:  $V_{FDSET}$  is below  $V_{REF1}$

or  $V_{ADIM}$  is below 500 mV. If the fault flag was asserted prior to either of these conditions, the fault flag will remain asserted. If the fault is removed while  $V_{FDSET}$  is below  $V_{REF1}$  or  $V_{ADIM}$  is below 500 mV the fault flag will be released.

When an output short fault occurs, such as LED shorted to ground or output capacitor shorted to ground, the regulator will not enter hiccup mode and will continue to switch. When the short is removed, the APM80904 will return to normal operation.

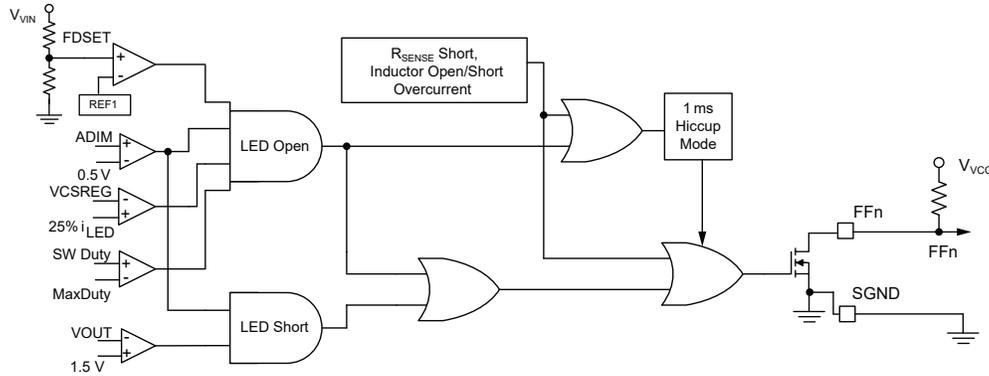


Figure 11: LED Open/Short Fault Block Diagram

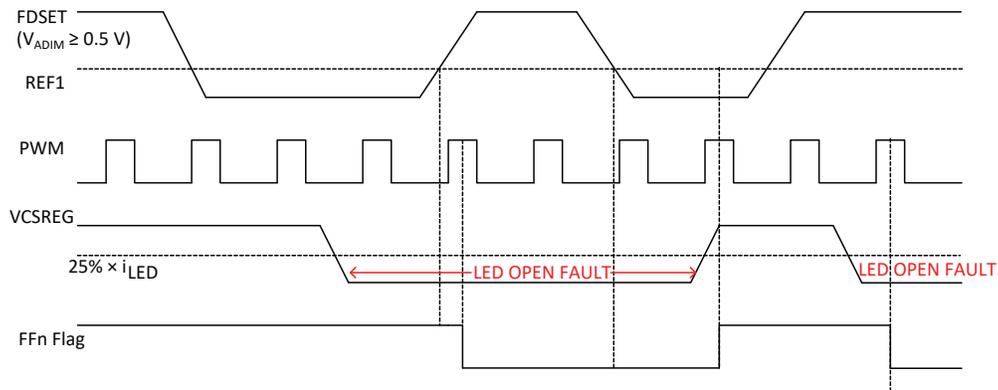


Figure 12: LED Open/Short Fault Timing Diagram

Table 3: LED Open Fault Truth Table

FFn (N)	FDSET	ADIM	LED Connection	PWM	FFn (N+1)	Note
<b>Previous LED open fault state does not matter</b>						
X	High	High	Closed Circuit	Next Rising Edge	1	Fault Flag does not assert (LEDs connected)
X	High	High	Open Circuit	Next Rising Edge	0	Fault Flag asserts on next PWM edge
<b>Previous LED open fault state high (not asserted)</b>						
1	Low	X	X	X	1	Fault flag does not assert when FDSET or ADIM are low
1	X	Low	X	X	1	
<b>Previous LED open fault state low (asserted)</b>						
0	Low	X	Open Circuit	X	0	Fault flag remains asserted if FDSET or ADIM go low after fault occurred
0	X	Low	Open Circuit	X	0	
0	Low	X	Closed Circuit	Next Rising Edge	1	Fault flag de-asserts if LEDs reconnect even when FDSET or ADIM is low
0	X	Low*	Closed Circuit	Next Rising Edge	1	

ADIM low is < 500 mV. FDSET low is when FDSET < VREF1 (typical 2.4 V).

\* must be > 400 mV for FF to go high.

The Fault deglitch time  $t_{FDG}$ , is fixed and is typically 50  $\mu$ s. The Fault mask time,  $t_{MASK}$ , is also fixed and is typically 100  $\mu$ s. (refer to Electrical Characteristics table). The Fault timing diagram is illustrated in Figure 13:

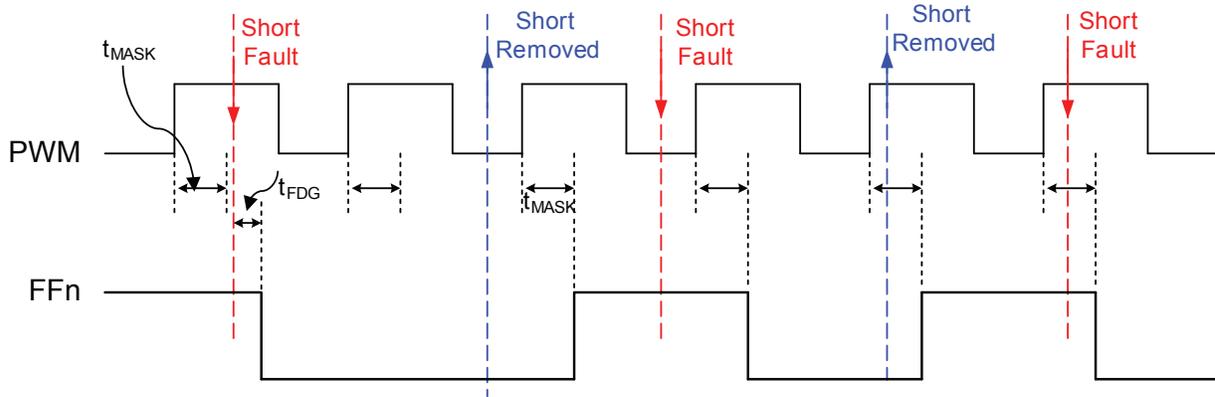


Figure 13a: LED Short Fault Timing Diagram Overview

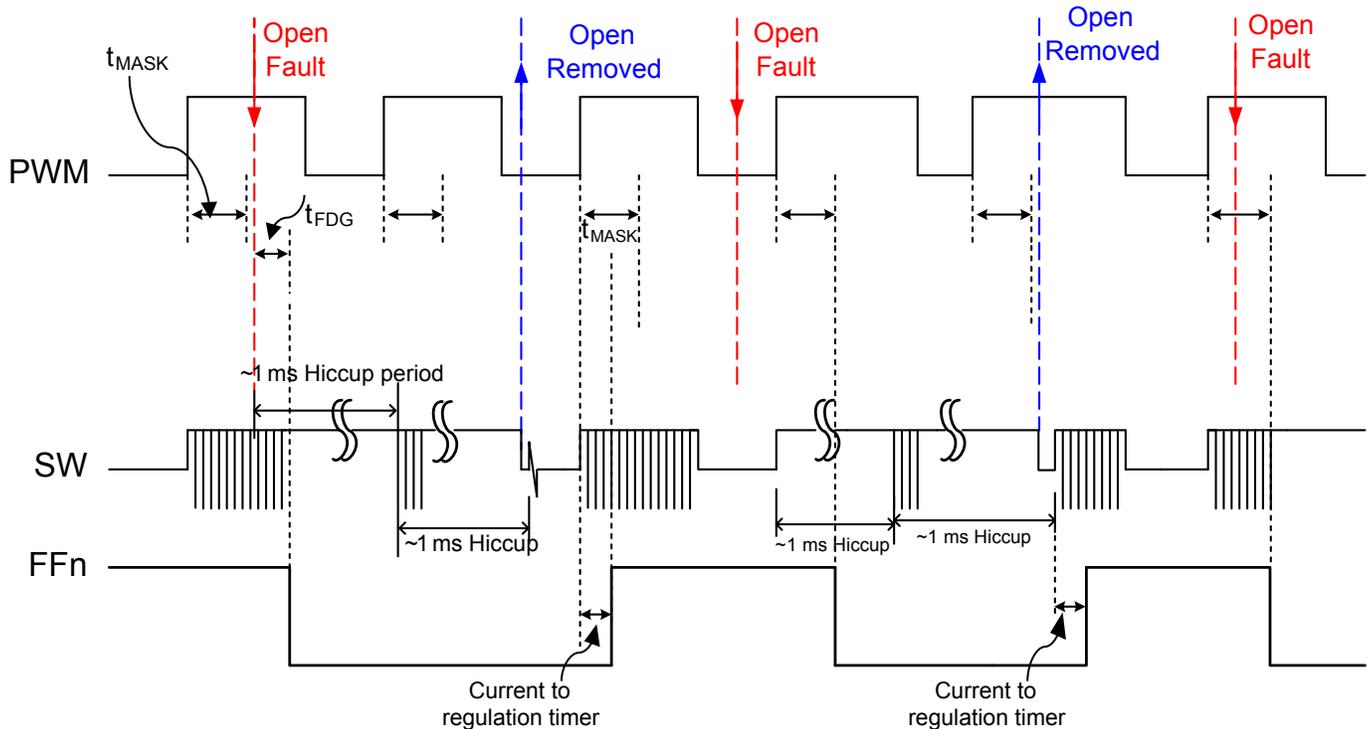
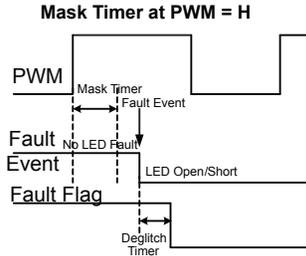


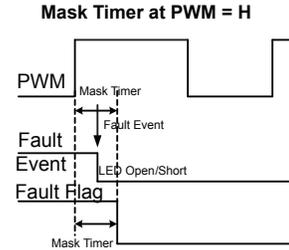
Figure 13b: LED Open Fault Timing Diagram Overview

The basic timing configurations are detailed below for LED Open/Short faults:

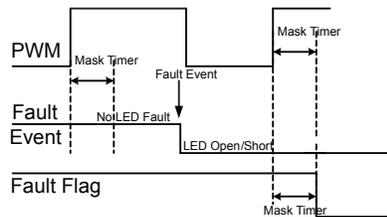
**Case 1: LED Open/Short Event is outside Mask Timer at PWM = H**



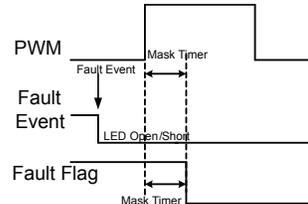
**Case 2: LED Open/Short Event is within Mask Timer at PWM = H**



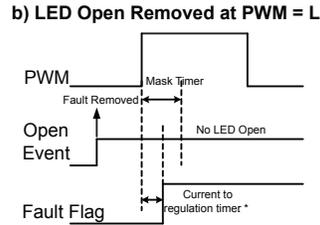
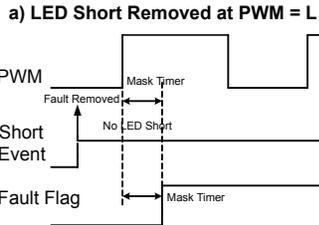
**Case 3: LED Open/Short Event is close to PWM ↓ at PWM = H**



**Case 4: LED Open/Short Event is at PWM = L**

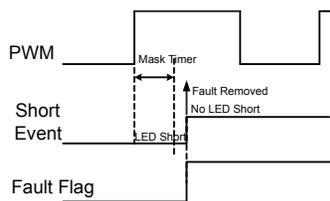


**Case 5: LED Open/Short Removed at PWM = L**

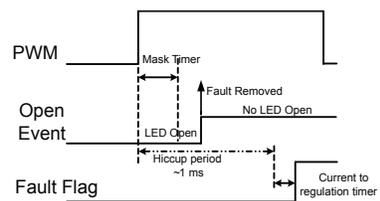


**Case 6: LED Open/Short Removed outside Mask Timer at PWM = H**

**a) LED Short Removed outside Mask Timer at PWM = H**

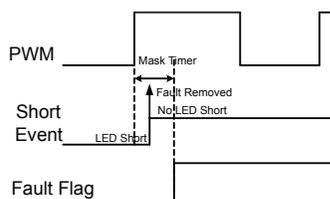


**b) LED Open Removed outside Mask Timer at PWM = H**

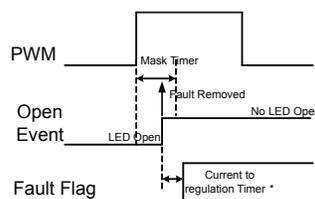


**Case 7: LED Open/Short Removed within Mask Timer at PWM = H**

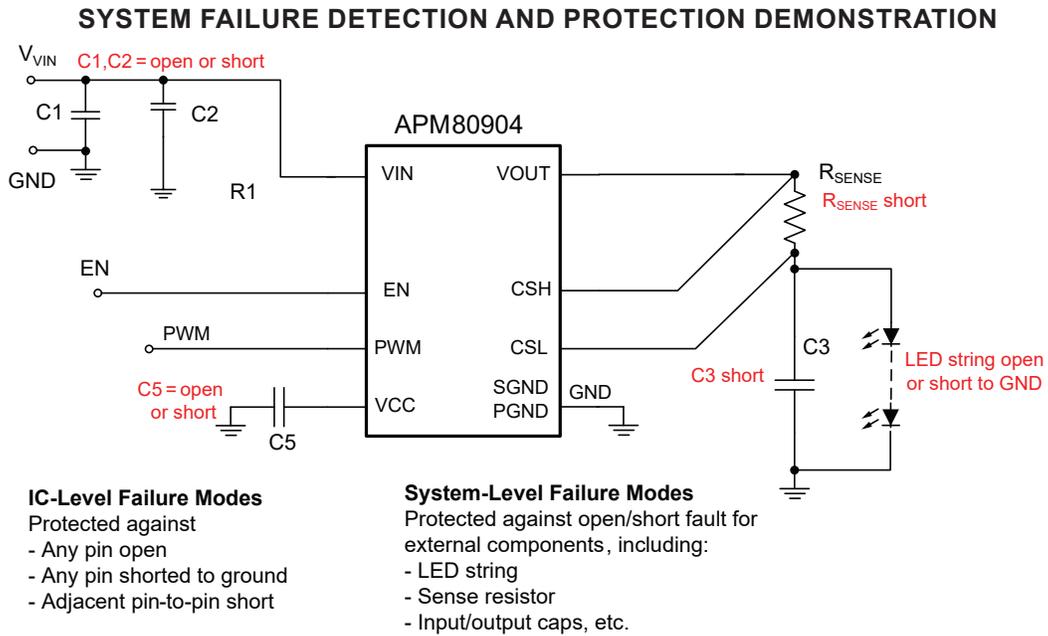
**a) LED Short Removed within Mask Timer at PWM = H**



**b) LED Open Removed within Mask Timer at PWM = H**



\* Current to regulation timer is 256 switching cycles.



**Figure 14: Demonstration of various possible fault cases in an application circuit**

**Table 4: System Failure Mode Table (partial)**

Failure Mode	Symptom Observed	FAULT flag asserted?	APM80904 Response
Sense resistor shorted	Dim light from LED	Yes	Triggers SW OCP fault, entering into Hiccup mode with about 1 ms retry period.
LED string open <sup>[2]</sup>	No light from LED	Yes <sup>[2]</sup>	Enter Hiccup mode with about 1 ms retry period.
LED string shorted <sup>[3]</sup> (Either LED shorted to GND or Output capacitor shorted to GND). < 1.5 V.	Dim light from LED	Yes	Continues switching at minimum $t_{ON}$ ; regulator will not enter Hiccup mode.

<sup>[1]</sup> When  $V_{CSL} - V_{CSH}$  is less than 0.2 V and PWM = H, Fault flag will not be asserted; when PWM is dimming and  $V_{CSL}$  is above 1.5 V, Fault flag will not be asserted.

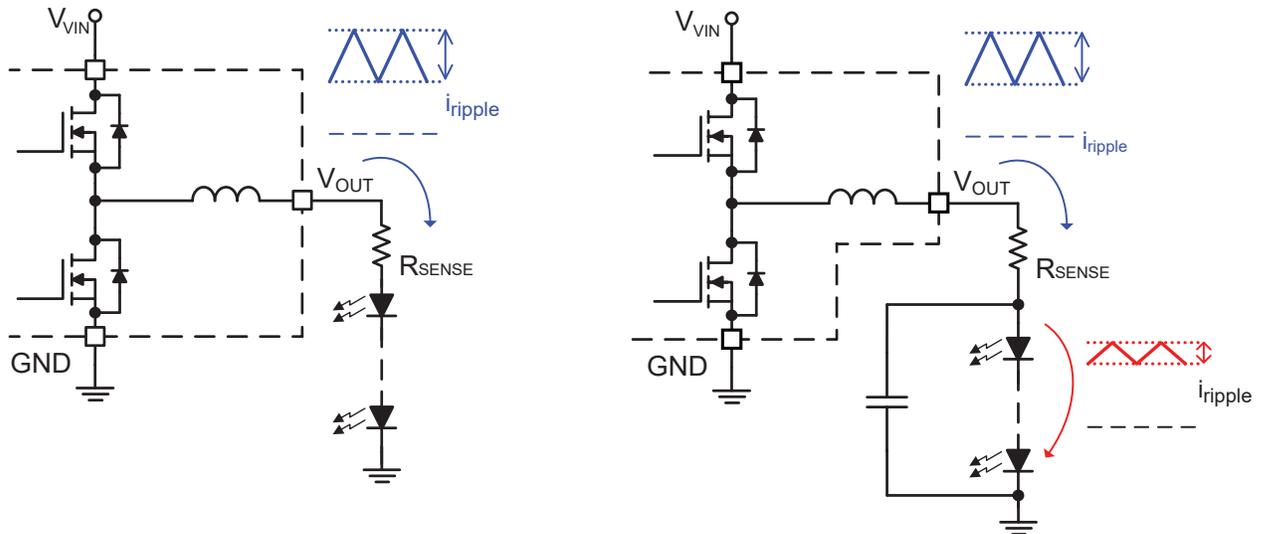
<sup>[2]</sup> For LED Open Fault, fault flag will not be asserted when  $V_{VIN}$  is below preset mask threshold,  $V_{ADIM}$  is below 500 mV or PWM dimming pulse width is below fault mask timer.

## Output Filter Capacitor

The APM80904 is designed to operate in current regulation mode. Therefore, it does not require a large output capacitor to stabilize the output voltage. This results in lower cost and smaller PCB area. In fact, having a large output capacitor is not recommended.

In most applications, however, it is beneficial to add a small filter capacitor (approximately 0.047  $\mu\text{F}$ ) very close to the CSL pin of the IC with a good connection to PGND. This capacitor serves as a filter to eliminate switching spikes seen by the LED string. This is very important in reducing EMI noises, and may also help in ESD testing.

## Effects of Output Capacitor on LED Ripple Current

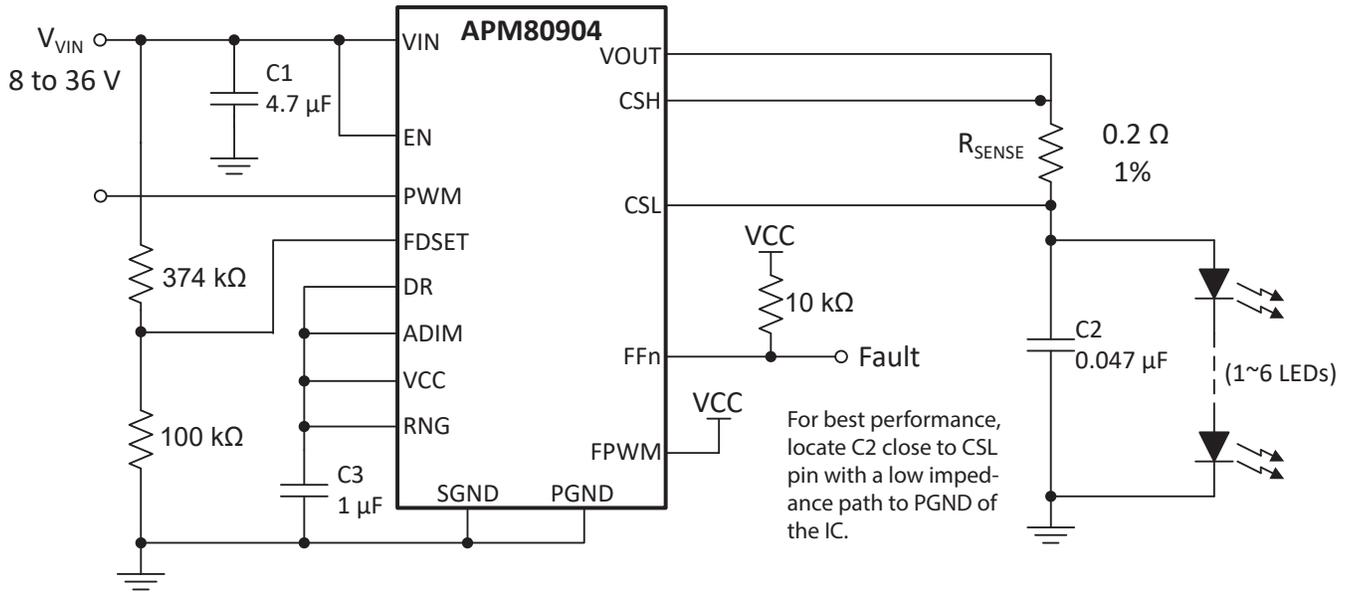


Without output capacitor:  
The same inductor ripple current flows through sense resistor and LED string.

With a small capacitor across LED string:  
Ripple current through LED string is reduced, while ripple voltage across  $R_{\text{SENSE}}$  remains high.

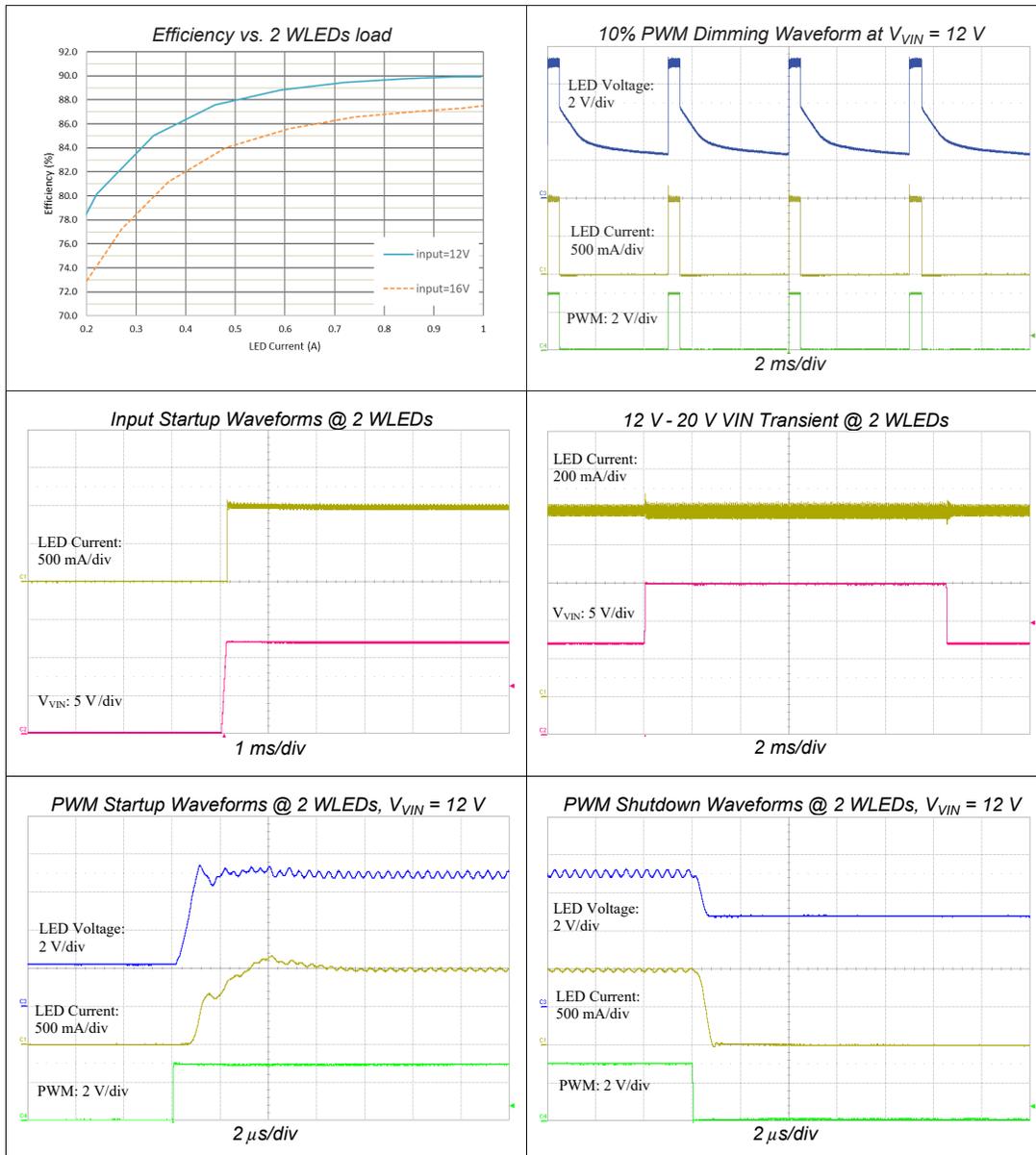
Figure 15: Using an Output Filter Capacitor to Reduce Ripple Current in LED String

### APPLICATION CIRCUIT DIAGRAMS

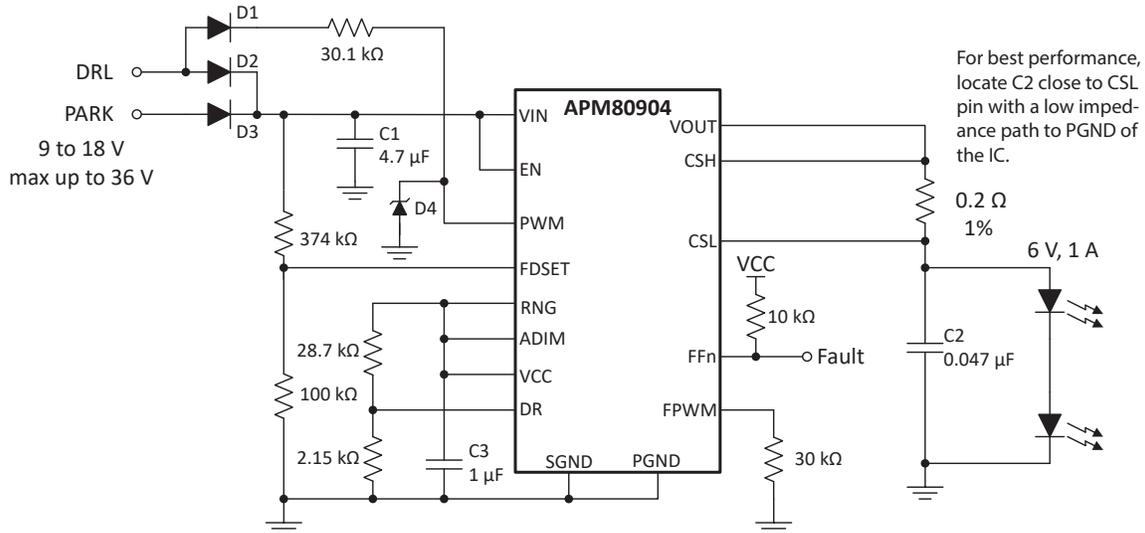


**Figure 16: Application circuit example for APM80904 with 1 A LED current.**  
The voltage divider between FDSET and VIN is set so that LED open fault will be masked when

C1	Ceramic capacitor, 4.7 μF, 50 V, 10%, X7S, 0805
C2	Ceramic capacitor, 0.047 μF, 50 V, 10%, X7R, 0805
C3	Ceramic capacitor, 1 μF, 16 V, 10%, X7R, 0603
R <sub>SENSE</sub>	Resistor, 0.2 Ω, 1/2 W, 1%, 1206
Fault Mask Threshold	$V_{VIN} \leq 2.4 V \times \left(1 + \frac{374 k\Omega}{100 k\Omega}\right) = 11.4 V$

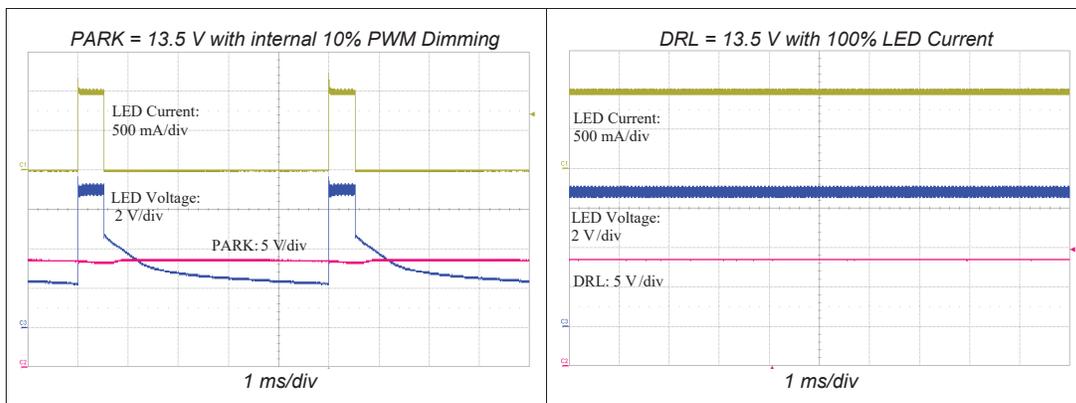


## APPLICATION CIRCUIT DIAGRAMS (continued)



**Figure 17: Application circuit example for APM80904 using 10% internal dimming for PARK and 100% LED current for DRL**

C1	Ceramic capacitor, 4.7 $\mu\text{F}$ , 50 V, 10%, X7S, 0805
C2	Ceramic capacitor, 0.047 $\mu\text{F}$ , 50 V, 10%, X7R, 0805
C3	Ceramic capacitor, 1 $\mu\text{F}$ , 16 V, 10%, X7R, 0603
R <sub>SENSE</sub>	Resistor, 0.2 $\Omega$ , 1/2 W, 1%, 1206
D1, D2, D3	Schottky diode 100 V, 2 A, SS2PH10-M3/84A
D4	Zener diode, 5.1 V, SZBZX84C5V1



## APPLICATION CIRCUIT DIAGRAMS (continued)

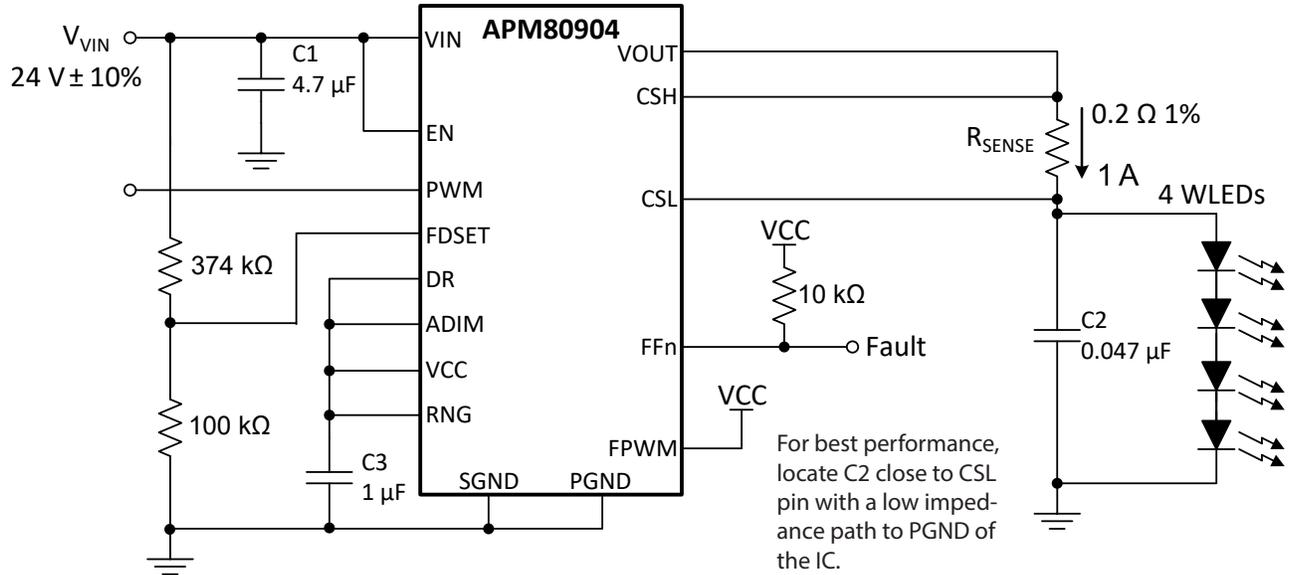
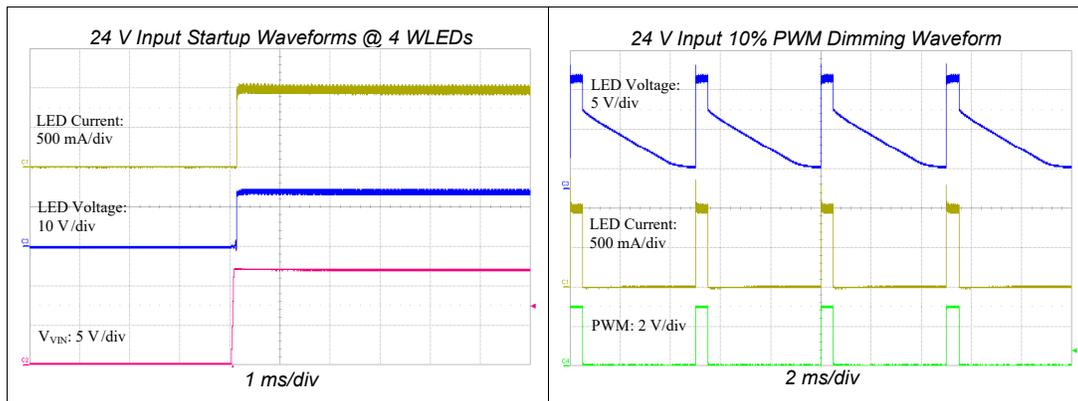
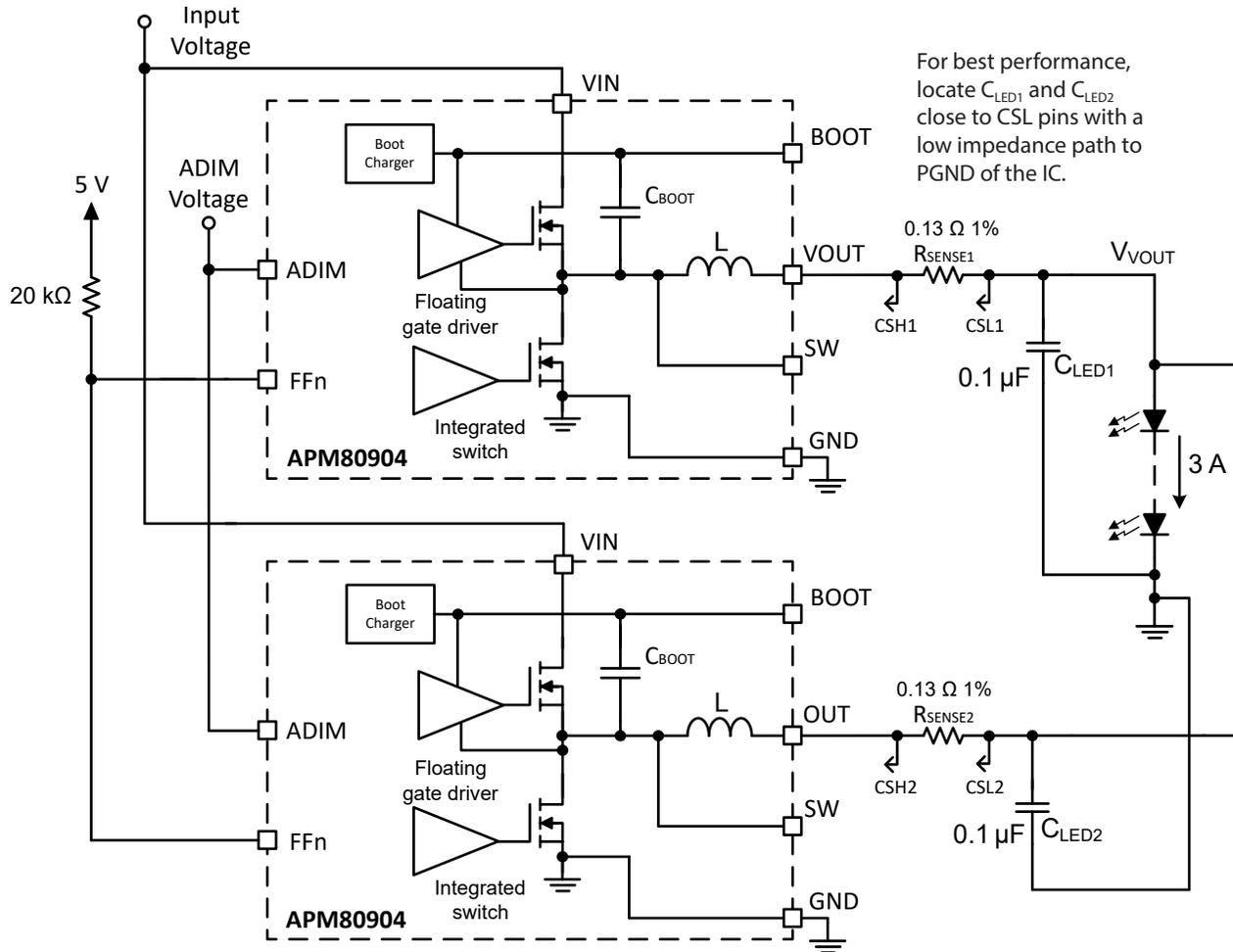


Figure 18: Application circuit example with  $V_{VIN} = 24\text{ V} \pm 10\%$ , 4 WLEDs @ 1 A

C1	Ceramic capacitor, 4.7 $\mu\text{F}$ , 50 V, 10%, X7S, 0805
C2	Ceramic capacitor, 0.047 $\mu\text{F}$ , 50 V, 10%, X7R, 0805
C3	Ceramic capacitor, 1 $\mu\text{F}$ , 16 V, 10%, X7R, 0603
$R_{SENSE}$	Resistor, 0.2 $\Omega$ , 1/2 W, 1%, 1206

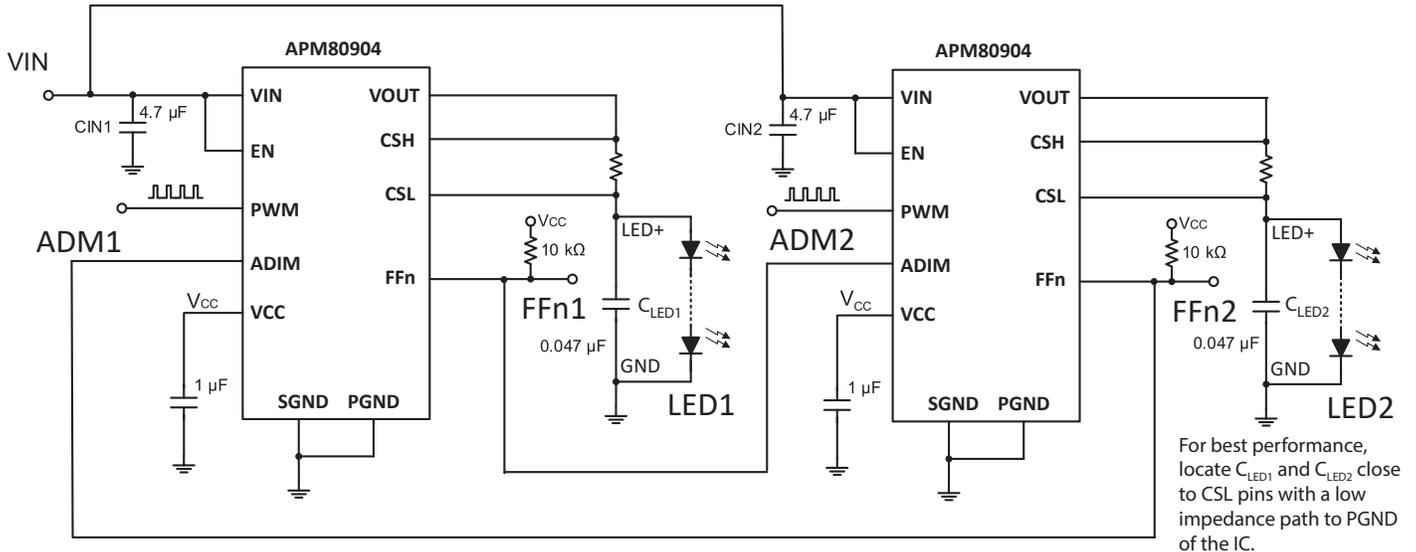


## APPLICATION CIRCUIT DIAGRAMS (continued)



**Figure 19: Using 2 (or more) APM80904s in parallel to drive the same LED string.  
Total LED current is the sum of currents from each LED driver.  
(Note: Each LED driver shares the same VIN and ADIM as illustrated.)**

## APPLICATION CIRCUIT DIAGRAMS (continued)



**Figure 20: “One Out All Out” functionality can be implemented with 2 APM80904s driving different LED strings:  
When one module fails (e.g. due to LED short or open),  
its FFn drives other module’s ADIM Low and forces to turn OFF LED current.**

## APPLICATION CIRCUIT DIAGRAMS (continued)

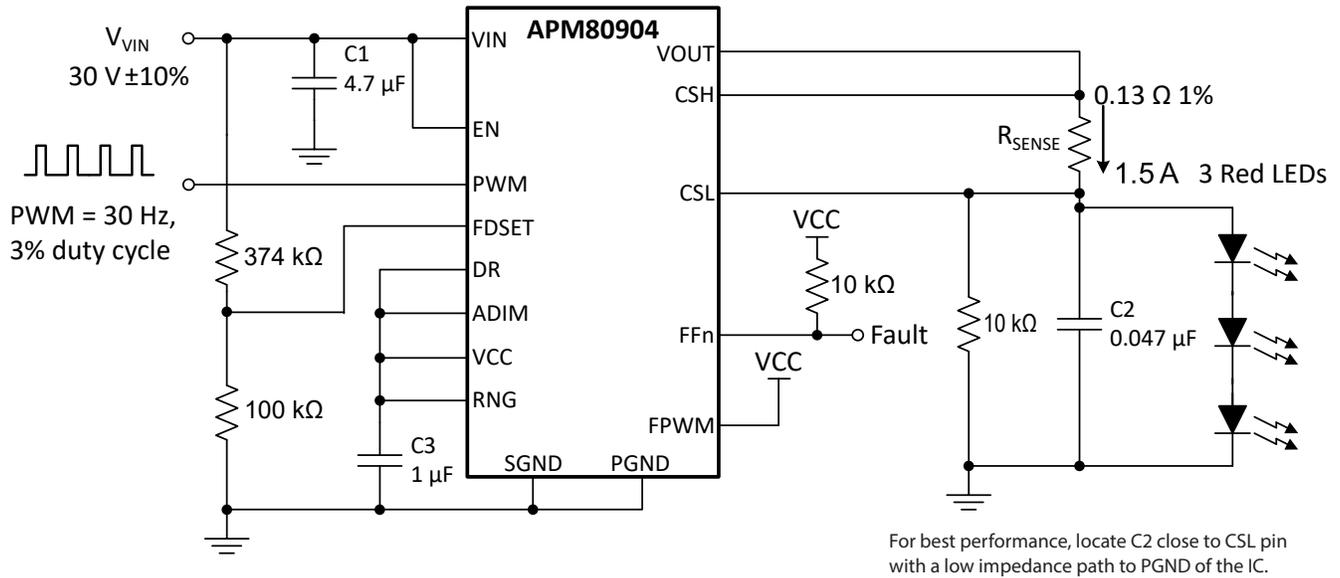
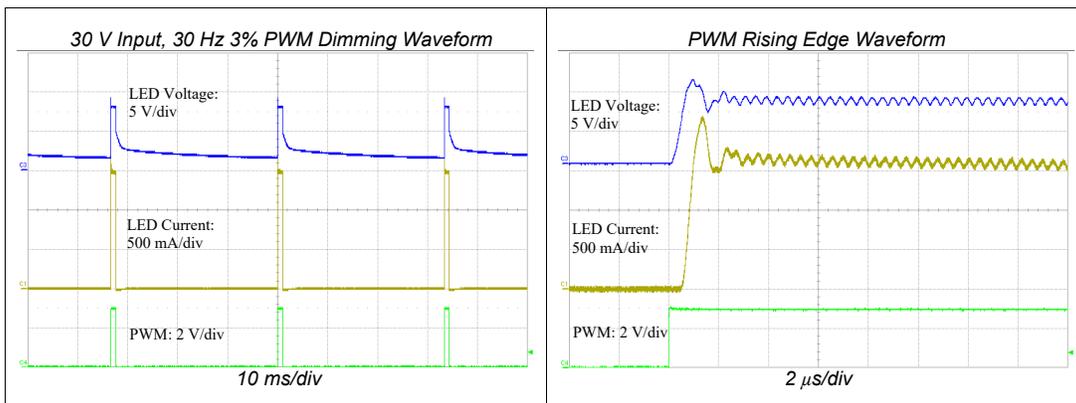


Figure 21: Application circuit example at  $V_{VIN} = 30\text{ V} \pm 10\%$  to drive 3 red LEDs @ 1.5 A with external PWM dimming at 30 Hz, 3% duty cycle.

C1	Ceramic capacitor, 4.7 $\mu\text{F}$ , 50 V, 10%, X7S, 0805
C2	Ceramic capacitor, 0.047 $\mu\text{F}$ , 50 V, 10%, X7R, 0805
C3	Ceramic capacitor, 1 $\mu\text{F}$ , 16 V, 10%, X7R, 0603
$R_{SENSE}$	Resistor, 0.13 $\Omega$ , 1/2 W, 1%, 1206



## PACKAGE OUTLINE DRAWING

### PRELIMINARY

For Reference Only; Not for Tooling Use  
(Reference DWG-0000753)

Dimensions in millimeters

Exact case and lead configuration at supplier discretion within limits shown

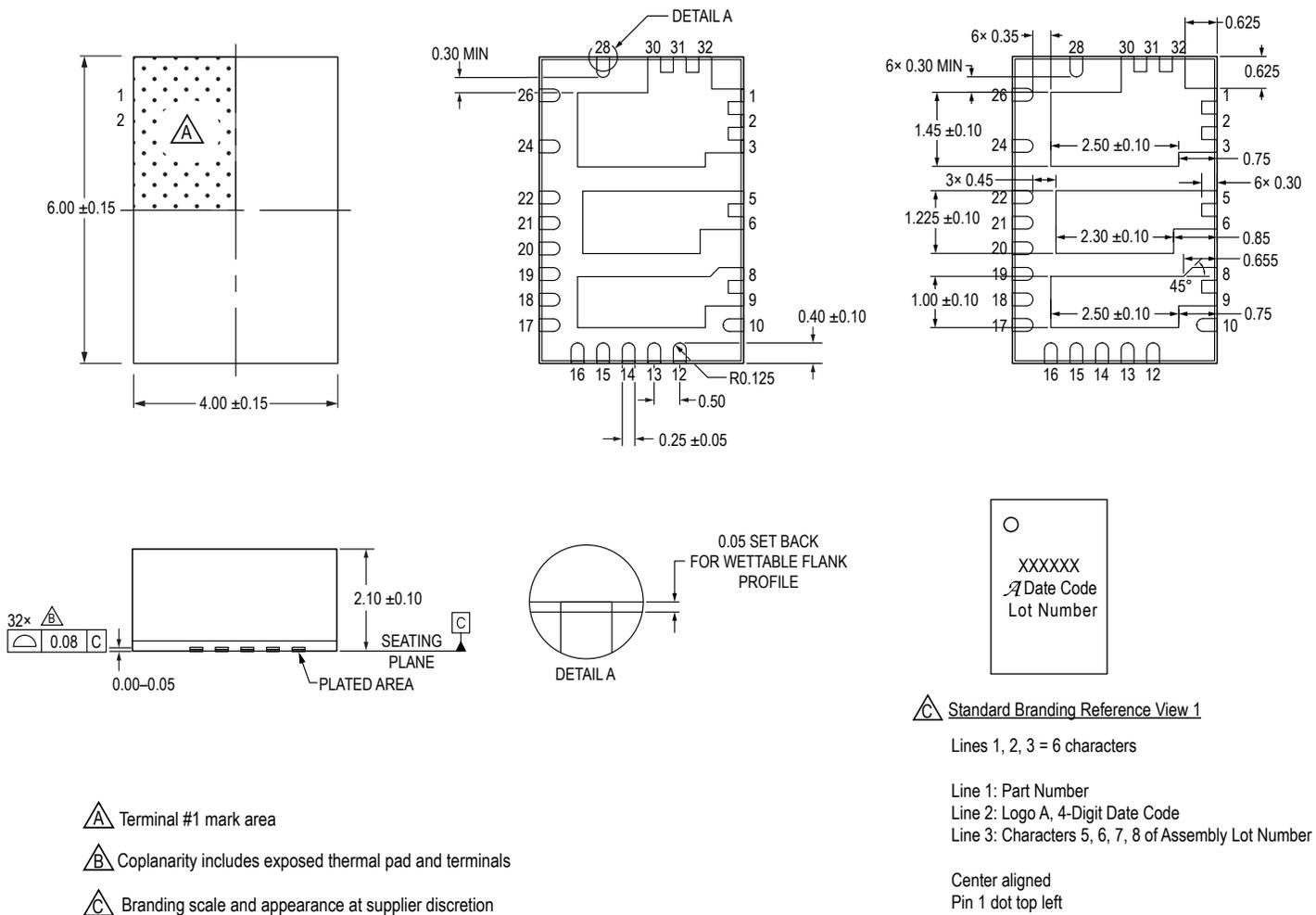
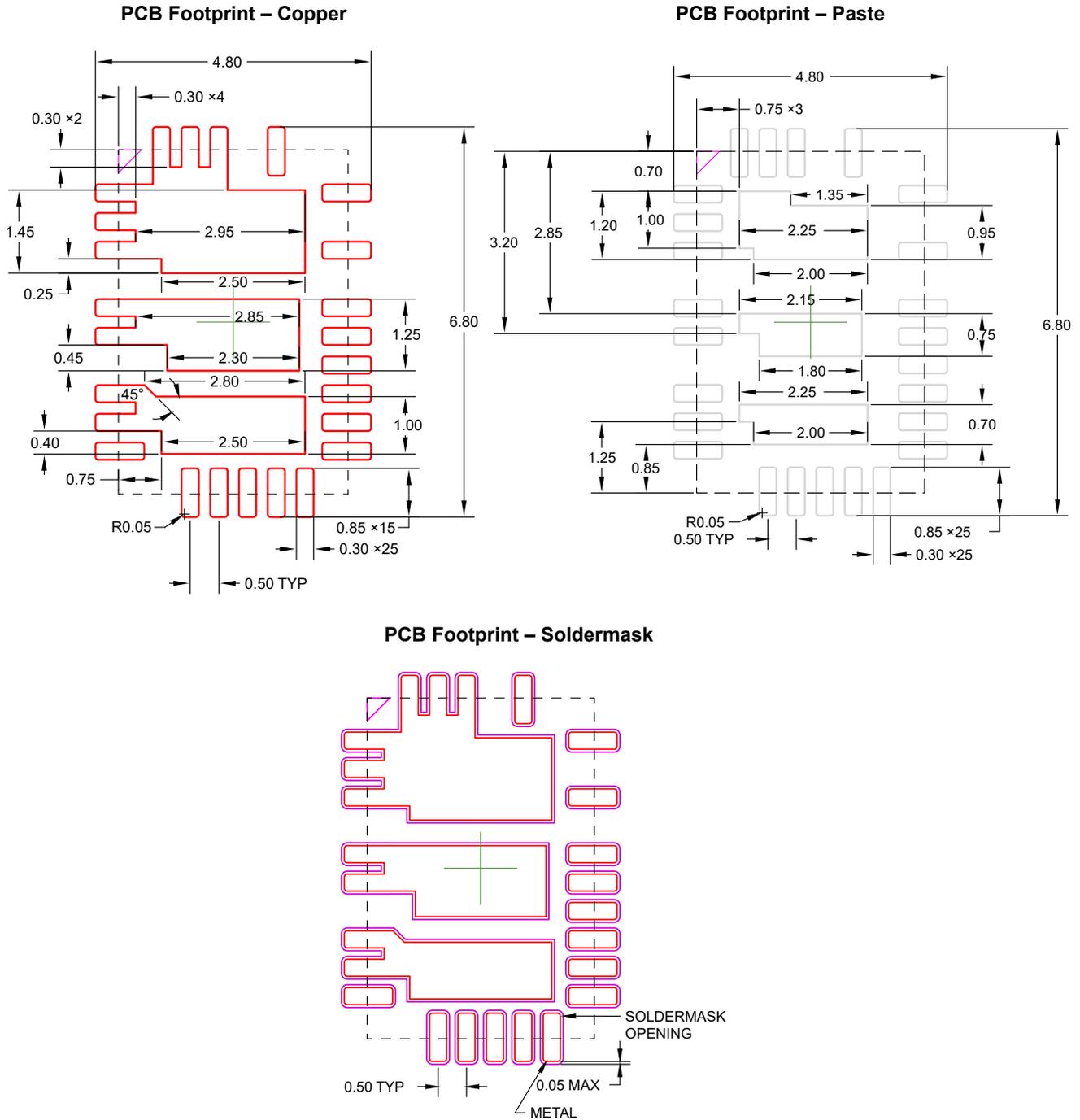


Figure 22: 32-pin 4 mm x 6 mm x 2.1 mm QFN with wettable flank (suffix NB)



**Figure 23: Recommended PCB Footprint**

Altium and Cadence schematic and layout library files for the APM80904 are provided on the APM80904 product page on [Allegromicro.com](http://Allegromicro.com).

## Revision History

Number	Date	Description
–	March 24, 2021	Initial release
1	March 30, 2021	Updated Figure 3 (page 9), Figure 11, (page 15), Figure 19 (page 24), and Figure 20 (page 25)
2	July 26, 2022	Removed Solder Reflow Considerations section
3	November 29, 2022	Added PCB footprint (page 28)

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