APM81815

80 V, 1.5 A, Synchronous Buck Regulator with Low EMI and 28 µA Quiescent Current

FEATURES AND BENEFITS

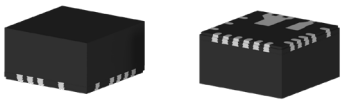
- AEC-Q100 Grade 1 qualified
- Functional safety capable: Documentation available to aid functional safety system design
- V_{IN} operating range: 5 to 72 V
- Continuous output current: 1.5 A
- V_{OUT} selectable: 3.3 V, 5 V, 5.35 V, or 12 V
- Integrated V_{IN} and boot capacitor to reduce component count and achieve ultra-low EMI
- Thermally enhanced and space saving 4 mm × 4 mm × 2.1 mm wettable-flank QFN package
- 28 µA no-load quiescent current (48 V_{IN} to 12 V_{OUT})
- < 2 µA V_{IN} shutdown current
- 2.15 MHz internally fixed and adjustable from 400 kHz to 2.4 MHz
- Average-current mode control
- Selectable frequency dithering to reduce EMI
- Accurate enable threshold
- Robust protection against:
  - □ Adjacent pin-to-pin short
  - □ Pin-to-ground short
  - □ Component open/short faults

APPLICATIONS

48 V Automotive Systems:

- Electric power steering
- DC-DC converters
- Battery-management systems
- Inverter and motor control
- Lighting and infotainment

PACKAGE



Not to scale

24-pin, 4 mm × 4 mm x 2.1 mm QFN with exposed thermal pads and wettable flank (suffix NB)

DESCRIPTION

The APM81815 is a highly integrated DC-DC regulator with very low electromagnetic interference (EMI) and an ultra-compact footprint. It is optimized to power low-voltage automotive electronics directly from the 48 V battery bus. The simple regulator design requires only a few external components. Critical power paths are contained within the package itself, which leads to very minimal EMI and ease of printed circuit board (PCB) layout. The bootstrap and high-frequency input capacitors are contained within the APM81815, which simplifies PCB design and improves EMI. The control-loop compensation is also internal, which further simplifies the PCB design. The APM81815 delivers up to 1.5 A at 3.3 V, 5 V, 5.35 V, or 12 V output voltages, selectable through pin configuration.

Flexibility to adjust functions—such as soft-start, switching frequency, or frequency dithering—is possible through pin configurations; alternatively, these pins can be tied to VCC or GND to minimize external components. The synchronous, low-EMI average-current mode-control scheme assures practical operation at the high ambient temperatures that are typical of the automotive under-hood environment. EMI mitigation and electromagnetic compatibility (EMC) are achieved with minimal filtering, and the frequency-dithering feature offers further reductions to easily achieve CISPR25 Class 5 compliance.

The comprehensive array of built-in protection and monitoring features include thermal shutdown, power good, output overvoltage/undervoltage (OV/UV), pulse-by-pulse current limit, and output short-circuit protection.

The APM81815 is offered in a space-saving 4 mm × 4 mm × 2.1 mm quad-flat no-lead (QFN) package with wettable flanks and exposed thermal pads.

EMC WITH EASE CLEARPOWER

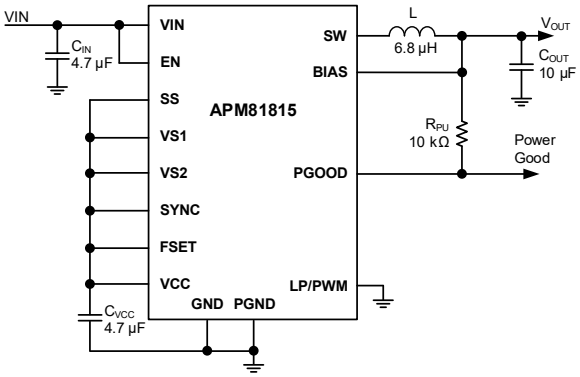


Figure 1: APM81815 Typical Application Circuit

SELECTION GUIDE

Part Number	Description	Packing [1]	Lead Finish
APM81815KNBJTR	24-pin, 4 mm × 4 mm × 2.1 mm QFN package with wettable flanks	3000 pieces per 13-inch reel	Matte Tin

[1] For additional packing options, contact Allegro.

ABSOLUTE MAXIMUM RATINGS [1]

Characteristic	Symbol	Notes	Rating	Unit
VIN, EN	V_{IN}, V_{EN}		–0.3 to 80	V
SW	V_{SW}	Continuous	–0.3 to (V_{IN} + 0.3) [2]	V
		V_{IN} ≤ 72 V, t < 50 ns	–1 V, V_{IN} + 2	V
BIAS	V_{BIAS}		–0.3 to 26	V
PGOOD	V_{PGOOD}		–0.3 to 17	V
VCC, VS1, VS2, SYNC, SS, FSET, LP/PWM			–0.3 to 4	V
Junction Temperature	T_J		–40 to 150	°C
Storage Temperature Range	T_{STG}		–55 to 150	°C

[1] Stresses beyond those listed in this table may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics table is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] This voltage is a function of temperature.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions [1]	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Package, 4-layer PCB based on JEDEC standard	56	°C/W
		Allegro evaluation board	33	°C/W

[1] Additional thermal information available on the Allegro website.

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PINOUT DIAGRAM AND TERMINAL LIST

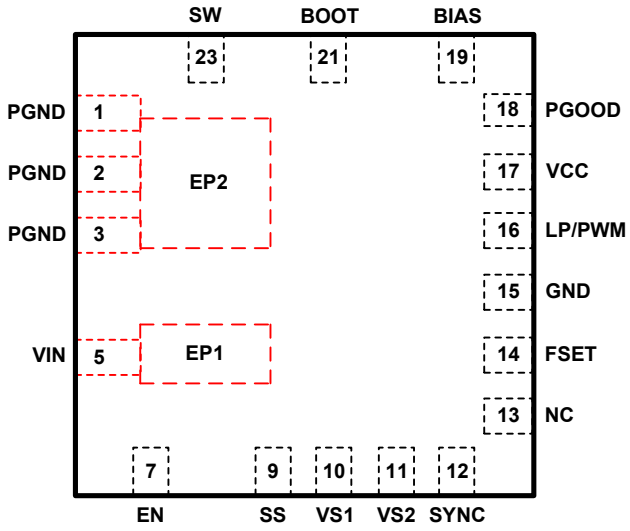

Figure 2: QFN-24 Pinout Diagram—24-Pin 4 mm × 4 mm × 2.1 mm Wettable Flank QFN Package

Number	Name	Description
1, 2, 3	PGND	Power ground pins.
5	VIN	Input voltage pin. Place a 4.7 µF ceramic bypass capacitor from VIN to PGND very close to this pin.
7	EN	Enable pin. Pull this pin high to enable the part. Connect EN directly to VIN for “always-on” applications.
9	SS	To use the internal soft-start ramp, connect SS to VCC. To configure a different soft-start time, connect a capacitor between SS and GND.
10	VS1	Output voltage selection pin 1.
11	VS2	Output voltage selection pin 2.
12	SYNC	Synchronization clock input and the frequency dither (spread spectrum) mode selection input. **Internal clock with dither:** To use internal 2.15 MHz clock and enable frequency dithering, connect SYNC to VCC. **Internal clock without dither**: To use internal 2.15 MHz clock without frequency dithering, connect SYNC to GND. **External clock without dither:** To synchronize the switching frequency to an external clock between 400 kHz and 2.5 MHz, apply an external clock to SYNC. Dithering is disabled in this mode.
13	NC	Connect this pin to ground or VCC.
14	FSET	Switching-frequency programming pin. To set the switching frequency, connect a resistor, R_{FSET}, from this pin to GND. To program a fixed 2.15 MHz (typical) frequency, connect FSET directly to VCC.
15	GND	Analog ground pin. Connect to PGND at the pad under the IC.
16	LP/PWM	Low-power mode/fixed-frequency PWM mode pin. **Low:** Allows the device to enter low-power (LP) mode at light loads. **High:** Forces fixed-frequency PWM mode.
17	VCC	Internal voltage regulator bypass capacitor pin. Connect a 4.7 µF ceramic capacitor from VCC to GND very close to this pin.
18	PGOOD	Power-good open-drain output signal. Connect a pull-up resistor to this pin. If the output voltage is out of range (undervoltage or overvoltage), this pin asserts low.
19	BIAS	Connect this pin to the output of the regulator. Provides output voltage feedback and powers the internal LDO when the output voltage level is in regulation.
21	BOOT	Do not connect external components to BOOT. This pin is provided for testing purposes.
23	SW	Regulator switch-node output pin. Connect this pin to the power inductor and keep this node small to minimize EMI.
EP1	Pad 1	This exposed back pad is connected to VIN. To optimize thermal dissipation, connect it to a plane under the device.
EP2	Pad 2	This exposed back pad is connected to PGND. To optimize thermal dissipation, connect it to a plane under the device.

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FUNCTIONAL BLOCK DIAGRAM

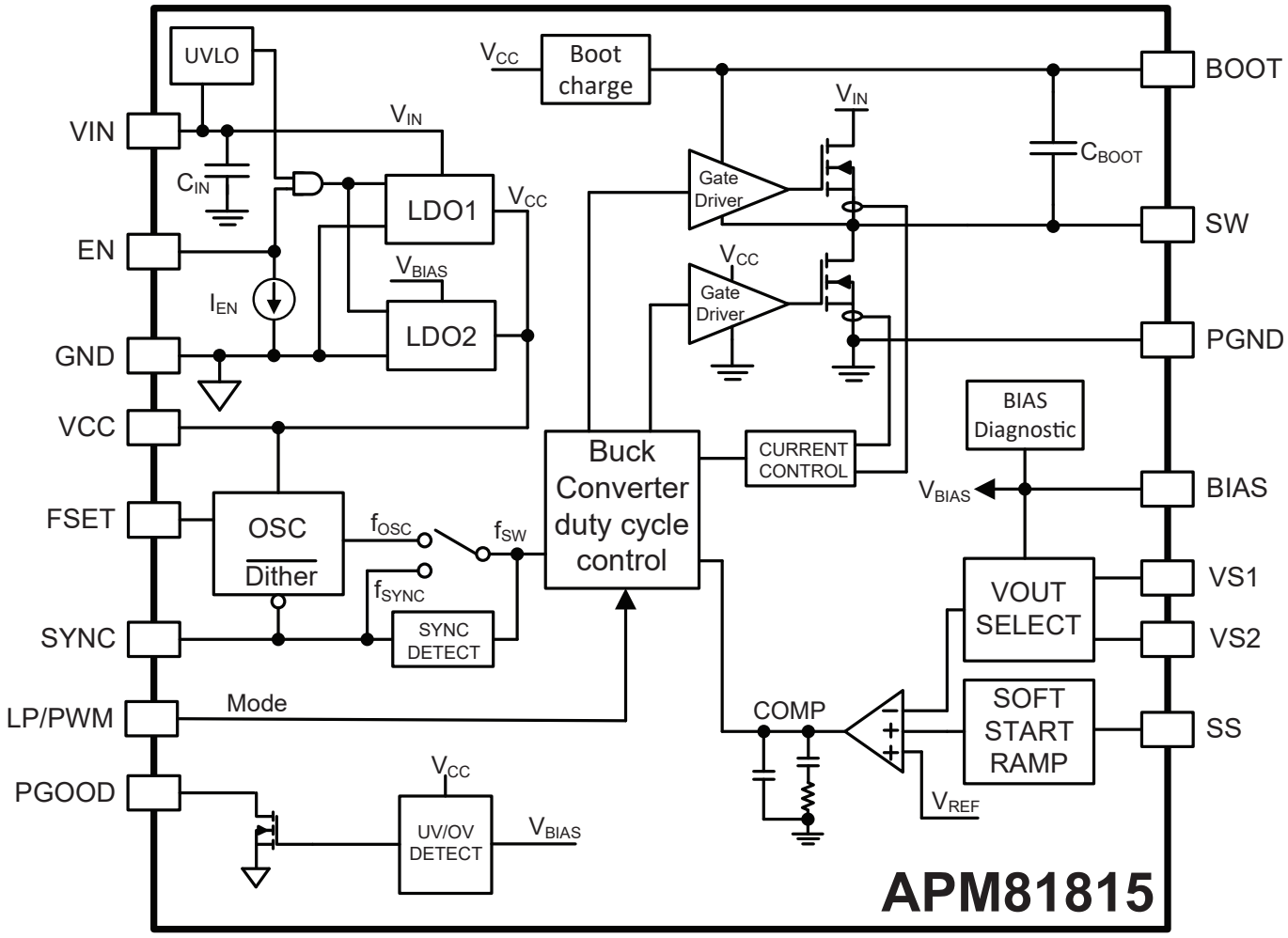

Figure 3: Functional Block Diagram

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ELECTRICAL CHARACTERISTICS: Valid for 5 V ≤ V_{VIN} ≤ 72 V, −40°C ≤ T_J ≤ 150°C, with typical values at 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INPUT SUPPLY						
Input Voltage Range	V_{VIN}	V_{EN} ≥ 2.5 V, after V_{VIN} > $V_{UVLO(ON,MAX)}$	5	–	72	V
Undervoltage Lockout (UVLO) Start	$V_{UVLO(ON)}$	V_{VIN} rising	4.2	4.8	5.4	V
Undervoltage Lockout (UVLO) Stop	$V_{UVLO(OFF)}$	V_{VIN} falling	3.8	4.3	5	V
Undervoltage Lockout Hysteresis	$V_{UVLO(HYS)}$		300	450	600	mV
LP MODE INPUT SUPPLY CURRENT						
Input Supply Current, LP Mode [1][2]	$I_{VIN(LP)}$	V_{VIN} = 12 V, V_{EN} ≥ 2.5 V, V_{OUT} = 3.3 V, no load, L = 6.8 µH	–	24	–	µA
		V_{VIN} = 12 V, V_{EN} ≥ 2.5 V, V_{OUT} = 5 V, no load, L = 6.8 µH	–	31	–	µA
		V_{VIN} = 48 V, V_{EN} ≥ 2.5 V, V_{OUT} = 12 V, no load, L = 6.8 µH	–	28	–	µA
Input Supply Current, PWM Mode [1][2]	$I_{VIN(PWM)}$	V_{VIN} = 48 V, V_{EN} ≥ 2.5 V, V_{OUT} = 12 V, f_{SW} = 2.15 MHz, no load	–	32	–	mA
		V_{VIN} = 48 V, V_{EN} ≥ 2.5 V, V_{OUT} = 12 V, f_{SW} = 400 kHz, no load	–	11	–	mA
Input Shutdown Current [1]	$I_{VIN(SD)}$	V_{VIN} = 48 V, V_{EN} = 0 V, T_J = 25°C	–	2	3	µA
REGULATION ACCURACY						
Output Voltage Accuracy	V_{VOUT1}	VS1 = 0, VS2 = 0	3.234	3.3	3.366	V
	V_{VOUT2}	VS1 = 0, VS2 = 1	4.9	5	5.1	V
	V_{VOUT3}	VS1 = 1, VS2 = 0	5.243	5.35	5.457	V
	V_{VOUT4}	VS1 = 1, VS2 = 1	11.76	12	12.24	V
SWITCHING FREQUENCY AND DITHERING						
Switching Frequency	$f_{SW(I)}$	V_{FSET} = V_{VCC}	1.9	2.15	2.4	MHz
	$f_{SW(E)}$	Resistor from FSET to GND = 220 kΩ	360	400	440	kHz
Frequency Dither Range	Δf_{SW}	V_{SYNC} = V_{VCC}	−6.5	–	6.5	% f_{OSC}
Minimum PWM Frequency with Dither	$f_{SW(MIN)}$	V_{FSET} = V_{VCC}	1.8	–	–	MHz
Dither Modulation Frequency	$f_{MOD(I)}$	V_{SYNC} = V_{VCC}, V_{FSET} = V_{VCC}	–	$f_{SW(I)}$ /256	–	MHz
	$f_{MOD(E)}$	V_{SYNC} = V_{VCC}, frequency set by resistor	–	$f_{SW(E)}$ /128	–	kHz
SYNCHRONIZATION INPUT (SYNC PIN)						
Synchronization Frequency Range	$f_{SW(SYNC)}$	V_{FSET} = V_{VCC}	0.4	–	2.4	MHz
SYNC Duty Cycle [3]	D_{SYNC}	V_{FSET} = V_{VCC}	–	–	90	%
SYNC Pulse Width [3]	t_{PWSYNC}	V_{FSET} = V_{VCC}	30	–	–	ns
SYNC Voltage Threshold [3]	$V_{SYNC(HI)}$	V_{SYNC} rising	–	–	1.5	V
	$V_{SYNC(LO)}$	V_{SYNC} falling	0.5	–	–	V
SYNC Pin Input Current [1]	I_{SYNC}	V_{SYNC} = 5 V	–	0.1	1	µA
PULSE WIDTH MODULATION (PWM) TIMING AND CONTROL						
Minimum Controllable SW On-Time [2]	$t_{ON(MIN)}$	V_{VIN} = 12 V, I_{OUT} = 1 A	–	–	35	ns
		V_{VIN} = 48 V, I_{OUT} = 1 A		–	60	ns
Minimum Controllable SW Off-Time [2]	$t_{OFF(MIN)}$	V_{VIN} = 12 V, I_{OUT} = 1 A	–	80	140	ns
LOW-POWER (LP) MODE						
LP Output Voltage Ripple [2]	$V_{PP(HLP)}$	8 V < V_{VIN} < 16 V, C_{OUT} = 47 µF, LP mode	–	65	–	mV

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ELECTRICAL CHARACTERISTICS (continued): Valid for 5 V ≤ V_{VIN} ≤ 72 V, −40°C ≤ T_J ≤ 150°C, with typical values at 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
INTERNAL MOSFET PARAMETERS						
High-Side On Resistance	$R_{DSON(HS)}$	V_{BOOT} – V_{SW} = 3.3 V, I_{DS} = 1 A, T_J = 25°C	–	150	190	mΩ
		V_{BOOT} – V_{SW} = 3.3 V, I_{DS} = 1 A, T_J = 150°C [2]	–	–	325	mΩ
Low-Side On Resistance	$R_{DSON(LS)}$	V_{VCC} = 3.3 V, I_{DS} = 1 A, T_J = 25°C	–	110	140	mΩ
		V_{VCC} = 3.3 V, I_{DS} = 1 A, T_J = 150°C [2]	–	–	240	mΩ
High-Side Leakage Current [2]	$I_{LKG(HS)}$	V_{VIN} = 48 V, V_{EN} = 0 V, V_{SW} = 0 V, T_J = 25°C	–	–	3.5	µA
Low-Side Leakage Current [2]	$I_{LKG(LS)}$	V_{VIN} = 48 V, V_{EN} = 0 V, V_{SW} = 48 V, T_J = 25°C	–	–	1.5	µA
Gate Drive Nonoverlap Time [2]	t_{NO}	V_{BOOT} – V_{SW} = 3.3 V	0.5	1.75	–	ns
Switch Node Rising Slew Rate [2]	SRHS	24 V ≤ V_{VIN} ≤ 48 V, V_{BOOT} – V_{SW} = 3.3 V	–	3	–	V/ns
MOSFET CURRENT PROTECTION THRESHOLDS						
Pulse-By-Pulse High-Side Current Limit [3]	$I_{LIM(HS)}$		2.1	2.6	3.2	A
Pulse-By-Pulse Low-Side Valley Current Limit	$I_{LIM(LS)}$	LS remains on until current reduces to less than $I_{LIM(LS)}$	–	2.75	–	A
Pulse-by-Pulse Low-Side Negative Current Limit	$I_{LIM(NEG)}$		–	–1	–	A
INDUCTOR CURRENT LIMITS						
Maximum Average Inductor Current Limit [1][2]	$I_{LIM(MAX)}$	V_{OUT} in regulation	–	2	–	A
Minimum Average Inductor Current Limit [1][2]	$I_{LIM(MIN)}$	PWM mode	–	–0.6	–	A
SOFT-START						
Soft-Start Delay Time [2]	t_{dSS}	C_{SS} = 2.2 nF	–	440	–	µs
Soft-Start Ramp Time [2]	$t_{SS(I)}$	V_{SS} = V_{VCC} Soft-start time is measured from 0 to 1.2 V	–	0.7	–	ms
	$t_{SS(E)}$	C_{SS} = 47 nF Soft-start time is measured from 0 to 1.2 V	–	12	–	ms
Soft-Start Pin Current	I_{SS}	V_{SS} = 0 V to 1.2 V	4.5	5	5.5	µA
OUTPUT VOLTAGE PROTECTION THRESHOLDS (BIAS OV/UV)						
OV Threshold Rising	$V_{VOUT(OVH)}$		105.5	107	108.5	% V_{OUT}
OV Threshold Falling	$V_{VOUT(OVL)}$		–	104	–	
OV Hysteresis	$V_{VOUT(OVHYS)}$		–	3	–	
UV Threshold Rising	$V_{VOUT(UVH)}$		–	98	–	% V_{OUT}
UV Threshold Falling	$V_{VOUT(UVL)}$		93.5	95	96.5	
UV Hysteresis	$V_{VOUT(UVHYS)}$		–	3	–	

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ELECTRICAL CHARACTERISTICS (continued): Valid for 5 V ≤ V_{VIN} ≤ 72 V, −40°C ≤ T_J ≤ 150°C, with typical values at 25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER GOOD OUTPUT (PGOOD PIN)						
OV Deglitch Time, V_{OUT} Rising	$t_{PGOOD(OVR)}$	Delay from V_{VOUT} = $V_{VOUT(OVH)}$ to PGOOD high-to-low	75	150	225	µs
OV Deglitch Time, V_{OUT} Falling	$t_{PGOOD(OVF)}$	Delay from V_{VOUT} = $V_{VOUT(OVL)}$ to PGOOD high-to-low	20	40	60	µs
UV Deglitch Time, V_{OUT} Rising	$t_{PGOOD(UVR)}$	Delay from V_{VOUT} = $V_{VOUT(UVH)}$ to PGOOD high-to-low	125	250	375	µs
UV Deglitch Time, V_{OUT} Falling	$t_{PGOOD(UVF)}$	Delay from V_{VOUT} = $V_{VOUT(UVL)}$ to PGOOD high-to-low	30	85	140	µs
PGOOD Initialization at Low VIN	$V_{PGOOD(INIT)}$	V_{VIN} = 1.5 V, V_{EN} = 0 V, I_{PGOOD} = 330 µA	–	–	400	mV
PGOOD Low-Output Voltage	$V_{PGOOD(L)}$	V_{VIN} ≥ 2.5 V, V_{EN} ≥ 2.5 V, I_{PGOOD} = 4 mA	–	150	400	mV
PGOOD Leakage Current [1]	I_{PGOOD}		–	0.1	6	µA
ENABLE INPUT						
EN High Threshold	$V_{EN(HI)}$	V_{EN} rising	1.15	1.2	1.25	V
EN Low Threshold	$V_{EN(LO)}$	V_{EN} falling	–	1.05	–	V
EN Input Hysteresis	$V_{EN(HYS)}$	$V_{EN(HI)}$ – $V_{EN(LO)}$	–	150	–	mV
Disable Delay	t_{DIS}	V_{EN} transitions low to when SW stops	–	60	–	µs
EN Pin Input Current [1]	I_{EN}	V_{EN} = 5 V	–	100	–	nA
INTERNAL REGULATOR (VCC PIN)						
VCC Regulation Voltage	V_{CC}	I_{VCC} ≤ 10 mA, external loading	3.1	3.3	3.5	V
VCC Maximum Load	$I_{VCC(CL)}$		–	–	10	mA
BIAS Pin Input Threshold	$V_{VOUT(TH)}$	If V_{OUT} exceeds this threshold and V_{IN} is greater than 6 V, the BIAS pin powers VCC	2.9	3.05	3.2	V
BIAS Pin Input Current [1]	I_{VOUT}	V_{VOUT} < $V_{VOUT(TH)}$ (2.7 V_{MIN})	–	4	–	µA
THERMAL SHUTDOWN PROTECTION (TSD)						
Thermal Shutdown Threshold [2]	T_{TSD}	T_J rising	160	175	190	°C
Thermal Shutdown Hysteresis [2]	T_{HYS}		–	20	–	°C

[1] For input and output current specifications, negative current is defined as coming out of the node or pin (sourcing), and positive current is defined as going into the node or pin (sinking).

[2] Ensured by design and characterization, not production tested.

[3] Limits ensured by design, characterization, and statistical correlation. Only functionally tested in production.

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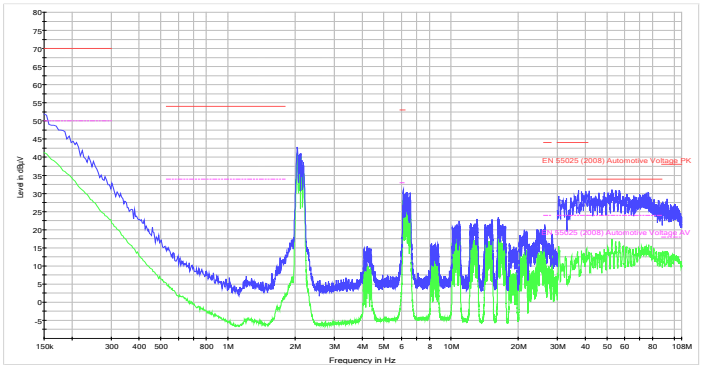
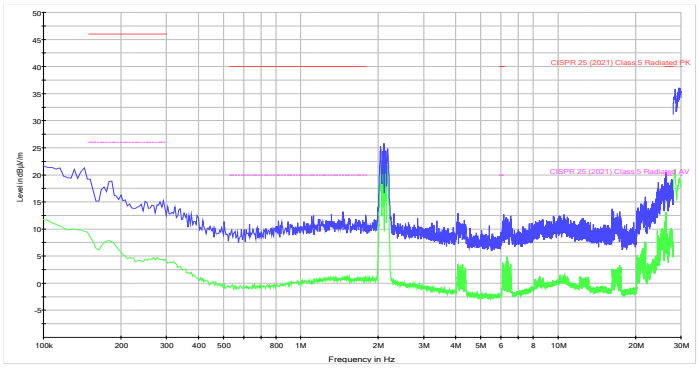
EMI/EMC PERFORMANCE CHARACTERISTICS

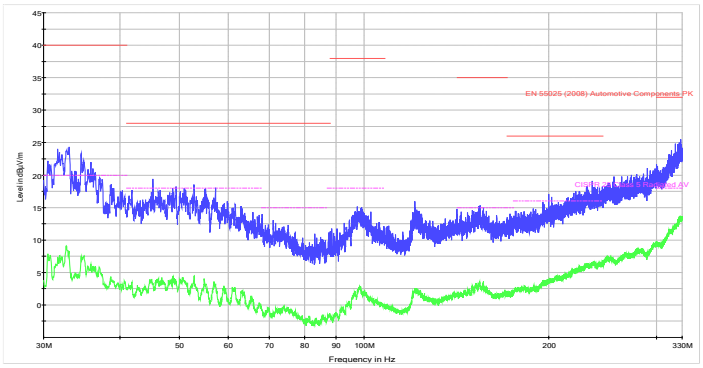
V_{IN} = 48 V, V_{OUT} = 12 V, f_{SW} = 2.15 MHz



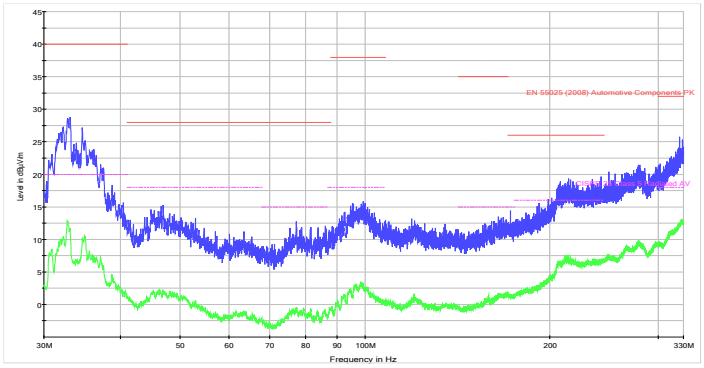
Conducted Emissions (150 kHz to 30 MHz)



Radiated Emissions (150 kHz to 30 MHz) (Monopole)



**Radiated Emissions (30 MHz to 330 MHz)
(Horizontal Biconical)**



**Radiated Emissions (30 MHz to 330 MHz)
(Vertical Biconical)**

NOTE: Allegro is not an accredited EMC laboratory. The information presented here is for reference only.

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FUNCTIONAL DESCRIPTION

Overview

The APM81815 is a 72 V operational and 1.5 A maximum output current, high performance synchronous buck regulator designed specifically for demanding automotive, industrial, and commercial applications. The device simplifies regulator design by minimizing the number of required external components and therefore minimizing PCB area. The regulator combines on-board high-frequency input filtering and switching frequency dithering to significantly reduce its EMI/EMC signature. The APM818185 provides excellent output voltage accuracy, uses average current-mode control to deliver quite low minimum on-times, and is capable of jitter-free operation.

The APM81815 can be pin configured for 3.3 V, 5 V, 5.35 V, or 12 V and uses internal compensation. The input voltage can be as high as 72 V and the switching frequency can be programmed from 400 kHz to 2.4 MHz or can be synchronized to an external clock. The regulator has a high-voltage tolerant input on the EN pin that can be tied directly to VIN and has very accurate enable and disable voltage thresholds. It has an internally fixed soft-start time of 0.7 ms when SS pin is connected to VCC and can be programmed for longer times as required by adding capacitor from SS pin to GND.

Protection features include VIN undervoltage lockout, cycle-by-cycle current limit, average current limit, short-circuit protection, output overvoltage and undervoltage protection, and thermal shutdown.

Output Voltage Accuracy and Selection

The APM81815 provides an output voltage accuracy of ±2% over the entire rated junction temperature, –40°C < TJ < 150°C. It also monitors VOUT directly, so its accuracy is not compromised by an external resistor divider between VOUT and a feedback pin. This exceeds the traditional approach of using a ±1% reference and an external resistor divider created with two ±1% resistors.

The APM81815 offers the most common output voltages: 3.3 V, 5 V, 5.35 V, and 12 V. The output voltage is determined by setting the VS1 and VS2 pins as shown in Table 1. The VS1 and VS2 pins are sampled at power-up and the output voltage is internally latched at that time; the output voltage cannot change during operation, which prevents noise or transients from erroneously altering the output voltage.

Table 1: APM81815 Output Voltage Configuration

VS1	VS2	VOUT (V)
GND	GND	3.3
GND	VCC	5.0
VCC	GND	5.35
VCC	VCC	12.0

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Average-Current Mode Control

The APM81815 uses average-current mode control to provide excellent noise immunity and very short minimum on-times, and it can deliver pulse widths that are virtually jitter free:

- Repeatable, closed-loop control with on-times of only 36 ns is demonstrated in Figure 4.
- Pulse-width jitter of 4.8 ns is shown in Figure 5.

The APM81815 employs internal compensation. This makes it very easy to use, reduces PCB area, and lowers cost. For optimal control-loop stability, select the external output LC filter components as follows:

Equation 1: $C_{OUT} = 164/(V_{OUT} \times f_{SW})$

where, C_{OUT} is in µF

Equation 2: $L = 7.25/f_{SW}$

where L is in µH and f_{SW} is in MHz. A minimal inductance value must be selected so that the inductor current ripple does not reach the high/low-side current peak limits at full load. To avoid this instability, the inductance value must not exceed 18 µH.

Compared to voltage mode control, current mode control is advantageous because it:

- Compensates for the effect of the output inductor, which reduces the order of the output filter.
- Offers better line and load regulation.
- Simplifies control-loop compensation.

Peak-current mode control:

- Suffers from subharmonic oscillations, typically when the power switch duty cycle exceeds 50%, where additional slope compensation is needed to stabilize the converter.
- Provides poor noise immunity because the peak current is measured and compared to a DC reference level, and noise on the peak current measurement or DC reference can result in jitter.
- Requires a blanking time on the rising edge of the switch current to prevent false triggering upon diode reverse recovery. This limits the minimum on-time and, therefore, how wide the conversion ratio can be.

In average-current mode control, these limitations are resolved, making it possible to regulate V_{OUT} with a constant switching frequency across a wide I_{OUT} and V_{IN} range.

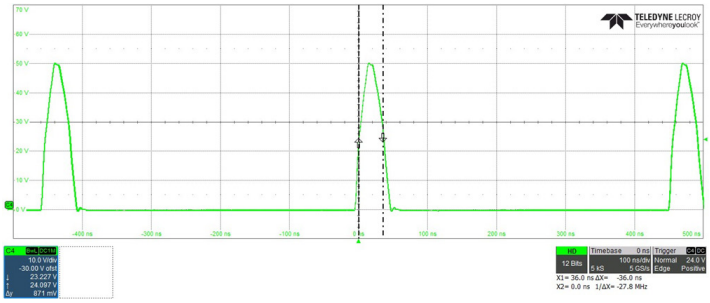

Figure 4: Repeatable, Controlled On-Times of Only 36 ns, 48 V_{IN}, 3.3 V_{OUT}, 2.2 MHz at 400 mA Load

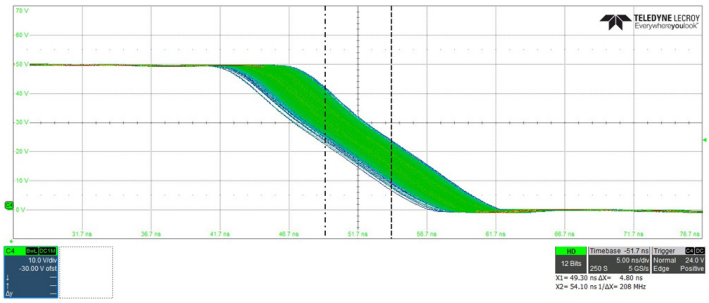

Figure 5: Pulse-Width Jitter with Dither Off, 48 V_{IN}, 5 V_{OUT}, 2.2 MHz at 1 A Load

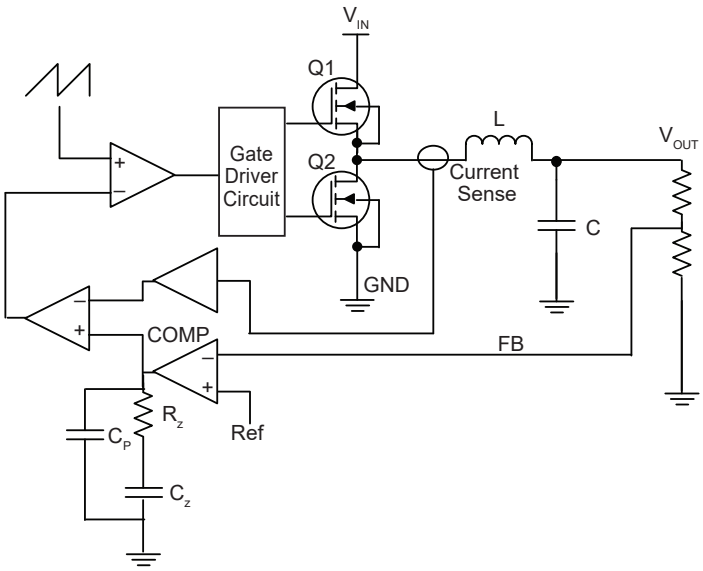

Figure 6:Typical Block Diagram of Average-Current Control Mode

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Low-Power Mode

Use the LP/PWM pin to configure the light-load operation of the APM81815. Set the LP/PWM pin to logic low to allow the APM81815 to enter low power (LP) mode when in a light load condition. Connect the LP/PWM pin to a logic high, such as to the VCC pin, to prevent automatic low-power mode operation and always force PWM mode.

The part switches from PWM mode to LP mode when all the following conditions are satisfied for at least three consecutive clock cycles:

- Soft-start is complete
- The output voltage is 3% higher than the nominal output voltage and lower than the overvoltage threshold.
- The compensation voltage (COMP in Figure 6) reduces to less than 0.5 V

The part switches back from LP mode to PWM mode when at least one of the following conditions is satisfied:

- The overvoltage condition is triggered
- The compensation voltage (COMP in Figure 6) exceeds 0.55 V for at least 200 ns

While in LP mode, the output voltage is regulated in a hysteretic manner within a ±3% window. When V_{OUT} reduces to less than 97% of the nominal value, the converter operates in critical-conduction mode, in which the inductor peak current is limited to 600 mA. When V_{OUT} reaches 103% of the nominal value, the converter stops switching until V_{OUT} again reduces to less than 97% of the nominal value.

Low-power mode improves light-load efficiency with a tradeoff for higher output voltage ripple. The input current as a function of I_{OUT} from 0 to 1 mA is reported in Figure 7. To prevent the device from ever entering LP mode, force the mode to PWM mode by tying the LP/PWM pin high.

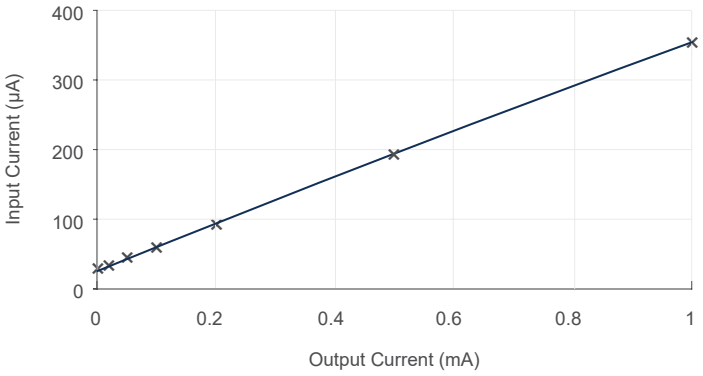

Figure 7: Low-Power Mode Input Current (V_{IN} = 48 V, V_{OUT} = 12 V, L = 6.8 µH)

Switching Frequency and Dithering

The switching frequency of the APM81815 can be set to an internally generated 2.15 MHz by connecting the FSET pin to VCC; or it can configured to a frequency between 400 kHz and 2.4 MHz with a resistor from the FSET pin to GND.

The value of the RFSET resistor connected from FSET pin to GND as a function of the switching frequency can be evaluated according to:

Equation 3: $$R_{FSET} = [79200/(f_{SW} - 27)] - 7.3$$

where R_{FSET} is in kΩ and f_{SW} is in kHz.

While choosing the PWM switching frequency, the designer should be aware of the minimum controllable on-time, $t_{ON(MIN)}$, of the APM81815. If the required on-time of the system is less than the minimum controllable on-time, pulse-skipping occurs and the output voltage exhibits increased ripple. The constant-frequency input voltage region for the four output voltage selection cases is shown in Figure 8.

A typical fixed-frequency PWM regulator creates distinct and narrow peaks of energy at the switching frequency and at the harmonics of the switching frequency. The APM81815 dithering feature spreads the spectrum across a wider frequency band, which reduces the peak magnitude of each harmonic.

The dithering sweep is internally set at ±5% typical (Δf_{SW}). This means the PWM switching frequency ramps from 0.95 to 1.05 times the internal switching frequency. However, the lowest switching frequency when using the FSET pin tied to VCC for f_{SW} = 2.15 MHz, $f_{SW(I)(min)} - \Delta f_{SW(max)}$, is guaranteed not to reduce to less than 1.8 MHz; thus, the harmonics are kept out of the AM band. The dither-modulation frequency (f_{MOD}) sweeps a triangular pattern that operates at approximately: $f_{SW}/256$ when the FSET pin is tied to VCC; or $f_{SW}/128$ when the FSET pin is tied to GND through a resistor.

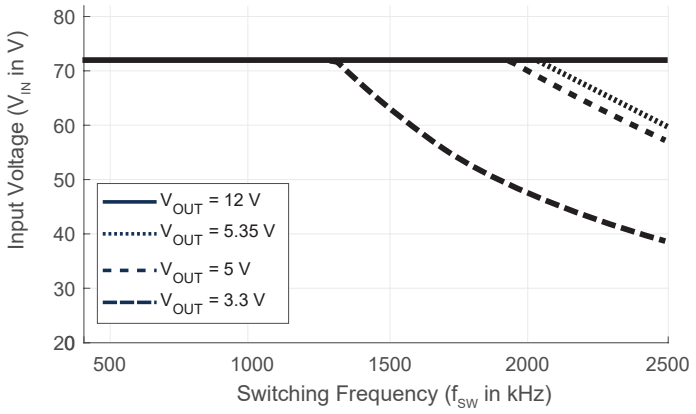

Figure 8: Input Voltage Limit to Prevent Pulse-Skipping Measured at I_{OUT} = 100 mA

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Synchronization Input

The SYNC pin has three possible operating states:

- To use the internal clock with frequency dithering, tie the SYNC pin high.
- To use the internal clock without dithering, tie the SYNC pin low.
- To synchronize the APM81815 switching frequency with an external clock, drive the SYNC pin with an external clock.

If the SYNC pin is connected to GND or if an external clock is applied to the SYNC pin, frequency dithering is disabled.

For the internal control-loop compensation to operate properly when the SYNC pin is driven with an external clock, the FSET pin must be configured to a switching frequency similar to that of the external clock.

Table 2: SYNC and FSET Configuration Truth Table

FSET Pin	SYNC Pin	Switching Frequency	Dither
VCC	VCC	2.15 MHz	Enabled
	GND		Disabled
Resistor to GND	VCC	Configurable, 400 kHz – 2.4 MHz	Enabled
	GND		Disabled
Resistor to GND	External Clock	External Clock	Disabled

Soft-Start

If a fault is not present and EN transitions high, the regulator begins its soft-start routine. When the SS pin is connected to VCC, the soft-start time is internally fixed at 0.7 ms. Longer soft-start times can be achieved with a capacitor from the SS pin to GND. The SS pin sources a 5 µA (typical) current to charge the external capacitor. The soft-start time can be set based on:

Equation 4: $t_{SS} = 0.22 \times C_{SS}$

where, t_{SS} is in ms, and C_{SS} is in nF. The total range for C_{SS} is 1 nF to 100 nF.

During soft-start, the APM81815 does not check the state of the LP/PWM pin and is forced into PWM mode; the device may operate in burst mode or discontinuous mode.

Dropout

The APM81815 is designed to operate at extremely low switching frequency during dropout conditions (low input voltage) in such a way as to minimize output voltage drop. The measured output voltage when V_{OUT} is set at 12 V in the forced PWM condition at 2.15 MHz with V_{IN} reducing to UVLO is shown in Figure 9.

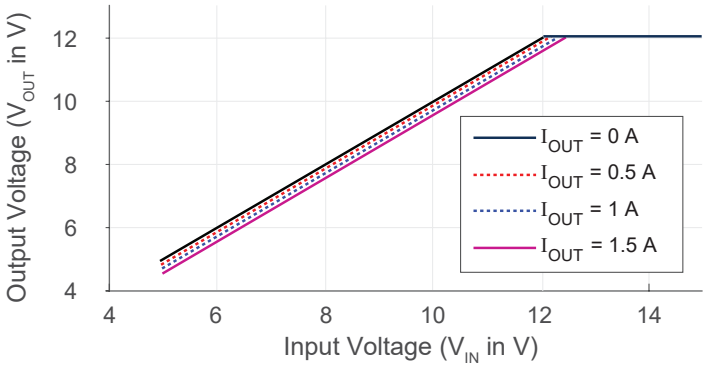

Figure 9: 12 V Output Voltage Dropout at Low V_{IN}

Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) comparator continuously monitors the voltage at the VIN pin and keeps the regulator disabled if the voltage is less than the lockout threshold, $V_{UVLO(ON)}$. The UVLO comparator incorporates enough hysteresis, 450 mV (typical), to prevent on/off cycling of the regulator due to voltage drop in the V_{IN} path during heavy loading or during startup.

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Enable/Undervoltage Lockout Function

The enable/undervoltage input (EN) pin allows the system to selectively enable and disable the regulator. The EN pin is rated to 80 V, so the regulator can be tied directly to VIN or the output of another regulator. If the EN pin is floating, an internal pull-down current pulls the voltage down and disables the regulator.

The enable input leads to a hysteretic comparator with a threshold to enable the device of 1.2 V (typical). Once enabled, the EN comparator has a typical hysteresis of 150 mV. If EN reduces to less than the turn-off threshold for a duration longer than t_{DIS} (disable delay), the APM81815 enters shutdown.

The EN pin can be used with a voltage divider from VIN to create a configurable undervoltage lockout threshold, as shown in Figure 10.

CEN is recommended to filter out any transients on the input line.

Select a convenient value for REN2 and calculate REN1 to estimate the rising enable threshold level using:

Equation 5:

$$R_{EN1} = \frac{V_{INTH(RISE)} - V_{EN(HI)}}{I_{EN} + \frac{V_{EN(HI)}}{R_{EN2}}}$$

where $V_{INTH(RISE)}$ is the desired threshold of rising input voltage to enable the APM81815 and I_{EN} is the EN pin input current.

Once both resistors are known, estimate the falling input voltage threshold level using:

Equation 6:

$$V_{INTH(FALL)} = (V_{EN(HI)} - V_{EN(HYS)}) \left(\frac{R_{EN1} + R_{EN2}}{R_{EN2}}\right) + I_{EN} R_{EN1}$$

For $V_{EN(HI)}$, $V_{EN(HYS)}$, and I_{EN}, refer to the Electrical Characteristics table.

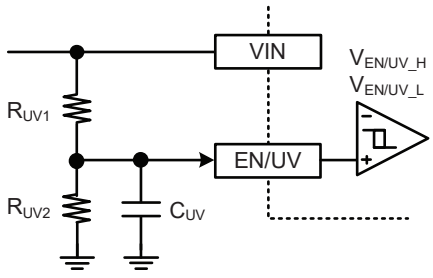

Figure 10: Input Undervoltage Lockout with EN Pin

Power Good (PGOOD)

PGOOD is an open-drain output that drives its output low when V_{OUT} is out of regulation. To enable the V_{OUT} status to be signaled, PGOOD must be pulled up to another voltage rail with a resistor:

- If V_{OUT} is within regulation, the PGOOD pin is in a high-impedance state and the output signal is pulled up to the external voltage.
- If V_{OUT} is out of regulation, PGOOD is pulled low to alert the system.
- If PGOOD is not used, the PGOOD pin can be left floating or grounded.

PGOOD operation is shown in detail in Figure 11. For time and voltage values, refer to the Electrical Characteristics table.

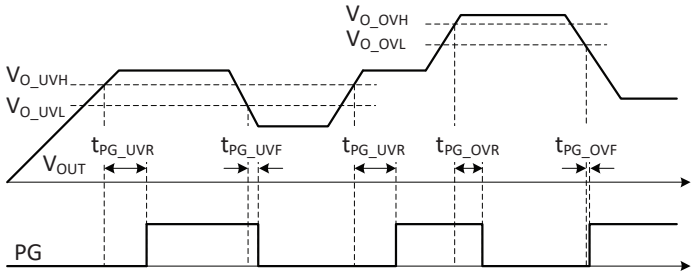

Figure 11: Power Good Operation

Pulse-by-Pulse Current Limit

The current in the high-side MOSFET is monitored on a cycle-by-cycle basis. If the high-side current exceeds $I_{LIM(HS)}$, the high-side MOSFET is turned off. Similarly, the current in the low-side MOSFET is monitored on a cycle-by-cycle basis. If the low-side current exceeds $I_{LIM(LS)}$, the low-side MOSFET is turned off. This protects the MOSFETs from excessive current, overheating, and possible damage.

Output Short-Circuit Protection

The APM81815 incorporates an output short-circuit protection to prevent device damage.

Referring to the Fault Mode Table, for the output short-circuit condition, the inductor should not saturate, given the highest peak current limit ($I_{LIM(HS)}$) at minimum duty cycle.

When this fail occurs, the device latches up; to restore the typical regulation behavior, it is necessary to toggle the EN pin.

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SW Pin Protection

If the SW pin is shorted to ground, very high current occurs in the high-side MOSFET. When the regulator detects this unusually high current ($I_{LIM(HS)}$), it instantly turns off the high-side MOSFET and latches-off the device. To restart the device, the enable or the input voltage must be cycled.

BOOT Pin Protections

To detect BOOT related faults, the APM81815 monitors the voltage across the internal BOOT capacitor. During faulty conditions, the converter remains off.

Overvoltage Protection (OVP)

The APM81815 provides a fundamental level of overvoltage protection. If V_{OUT} exceeds the overvoltage threshold (107%, $V_{OUT(OVH)}$) for longer than the deglitch time ($t_{PGOOD(OVR)}$), the high-side MOSFET shuts off. Also, to correct the overvoltage condition, the low-side MOSFET turns on and sinks current from VOUT. Each PWM cycle, the low-side MOSFET is allowed to be on until the inductor current reaches the negative current limit (–1 A, $I_{LIM(NEG)}$) of the low-side MOSFE .

Thermal Protection

The device protects itself from overheating by means of an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold (T_{TSD}, 175°C, typical), the high-side and low-side MOSFETs are shut off, the BOOT charger is shut down, and the internal control circuits are reset. When the junction temperature decreases more than the thermal shutdown hysteresis (T_{HYS}, 20°C, typical), the regulator automatically restarts.

Pin-to-Ground and Adjacent Pin Short Protections

The APM81815 is designed to satisfy the most demanding applications. For example, the device is designed to withstand a short circuit to ground at each pin without sustaining damage. In addition, care was taken when defining the device pinout to optimize protection against adjacent pin-to-pin short circuits. For example, logic pins and high-voltage pins are separated as much as possible. Inevitably, some low-voltage pins are located adjacent to high-voltage pins; however, in these instances, the low-voltage pins are designed to withstand unusually high voltages with clamps and/or series input resistance to prevent damage to the device.

A comprehensive summary of all fault conditions and the response of the regulator in each case is shown in the Fault Mode Table.

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FAULT MODE TABLE

Fault Mode	Internal Soft-Start	During Fault Counting		Boot Charging	Power Good	Latched Fault?	Reset Condition
		High-Side MOSFET	Low-Side MOSFET				
VIN Undervoltage	Pulled low via 2 kΩ resistor, no hiccup	Forced turn-off	Forced turn-off	Disabled	Depends on V_{OUT}	NO	Automatic, V_{IN} exceeds UV start threshold
Output/BIAS Pin Shorted to Ground	Not affected	Forced turn-off	Forced turn-off	Not affected	Pulled low	YES	Toggle VIN or EN
Output Overcurrent	Not affected	Responds to regulation	Turned-on if boot voltage is too low	Not affected	Depends on V_{OUT}	NO	Automatic
High-Side MOSFET Overcurrent (SW Short to GND)	Not affected	Forced turn-off	Forced turn-off	Not affected	Pulled low	YES	Toggle VIN or EN
Low-Side MOSFET Overcurrent (SW Short to VIN)	Not affected	Forced turn-off	Forced turn-off	Not affected	Pulled low	NO	Automatic, short removed
	For high V_{IN} values, the IC could be damaged						
Boot Pin Fault	Not affected	Forced turn-off	Forced turn-off	The device tries to recharge the boot capacitor	Depends on V_{OUT}	NO	Automatic, fault removed
Output Overvoltage	Not affected	Turned-off by regulation	Pulsed with minimum off-time	Disabled when V_{BIAS} is too high	Pulled low when V_{BIAS} is too high	NO	Automatic, after V_{OUT} returns to typical range
Output Undervoltage	Not affected	Active, responds to regulation	Turned-on if boot voltage is too low	Not affected	Pulled low when V_{OUT} is too low	NO	Automatic, after V_{OUT} returns to typical range
BIAS Pin Open	Not affected	Turned-off by regulation	Pulsed with minimum off-time	Disabled	Pulled low	NO	Automatic, after V_{BIAS} pin fault is removed
Thermal Shutdown (TSD)	Pulled low until $V_{SS} < V_{SSRST}$ and $T<T_{TSD}$	Forced turn-off	Forced turn-off	Disabled	Pulled low	NO	Automatic, part cools down

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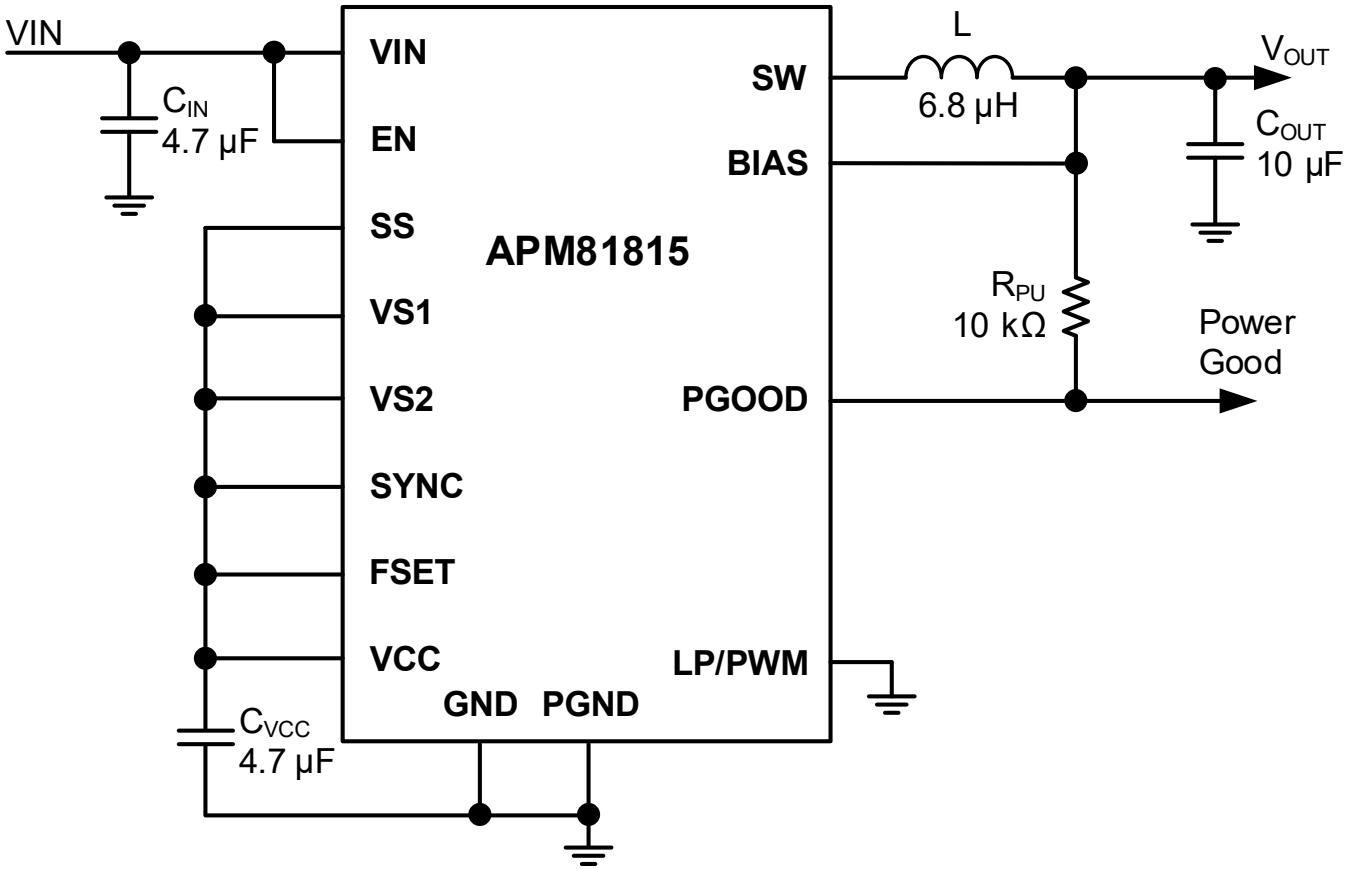
APPLICATION CIRCUIT



VIN	5 – 72	V
VOUT	12	V
LP Mode	Disabled	
f_{SW}	2.15	MHz
Dithering	Enabled	
Soft-Start Time	0.7	ms

Figure 12: Application Circuit

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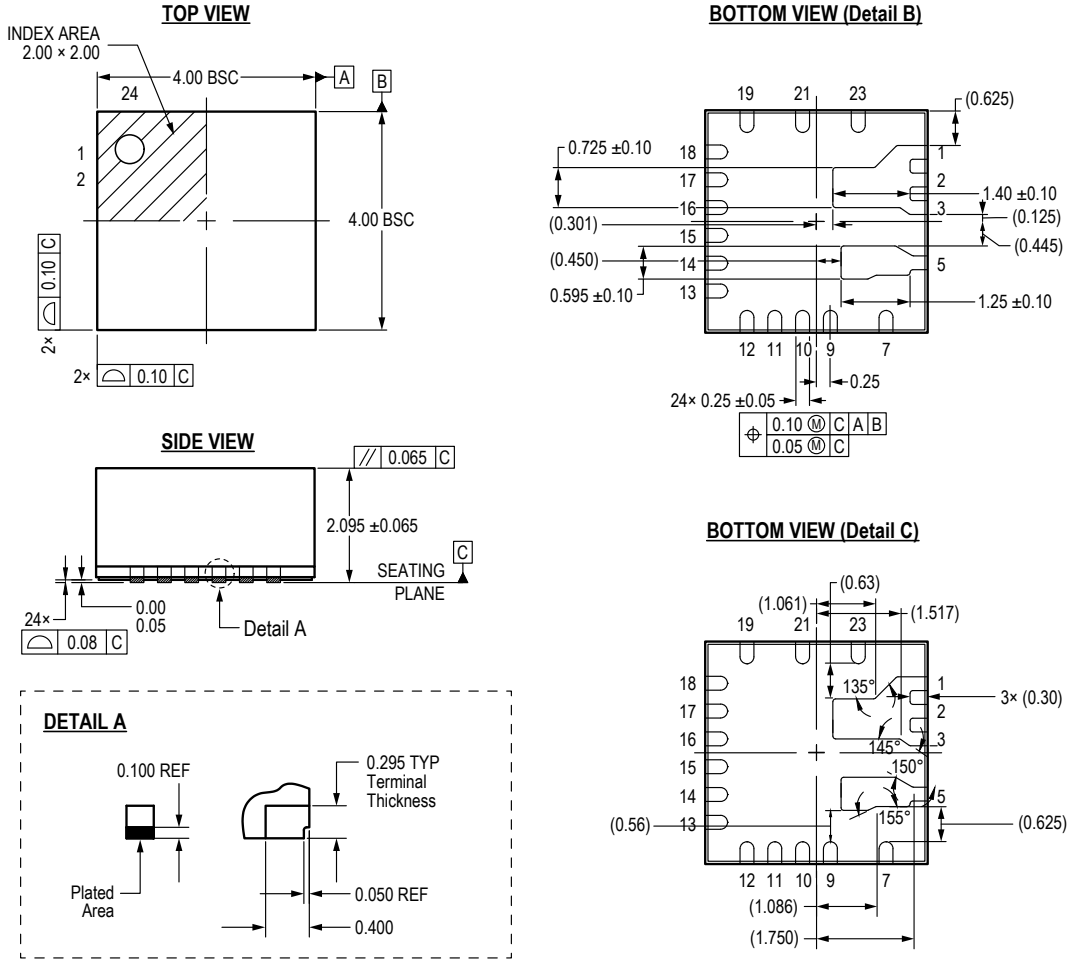
PACKAGE OUTLINE DRAWING AND RECOMMENDED PCB FOOTPRINT

For Reference Only – Not for Tooling Use

(Reference Allegro DWG-0000820, Rev. 2, incl. Appendix: APM81815)

NOT TO SCALE
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



STANDARD BRANDING REFERENCE VIEW

Line 1: Part Number
Line 2: Logo A, 4 digit Date Code
Line 3: Assembly Lot Number

Figure 13: 24-Lead 4 mm × 4 mm QFN (Suffix NB)

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PCB LAYOUT GUIDELINES

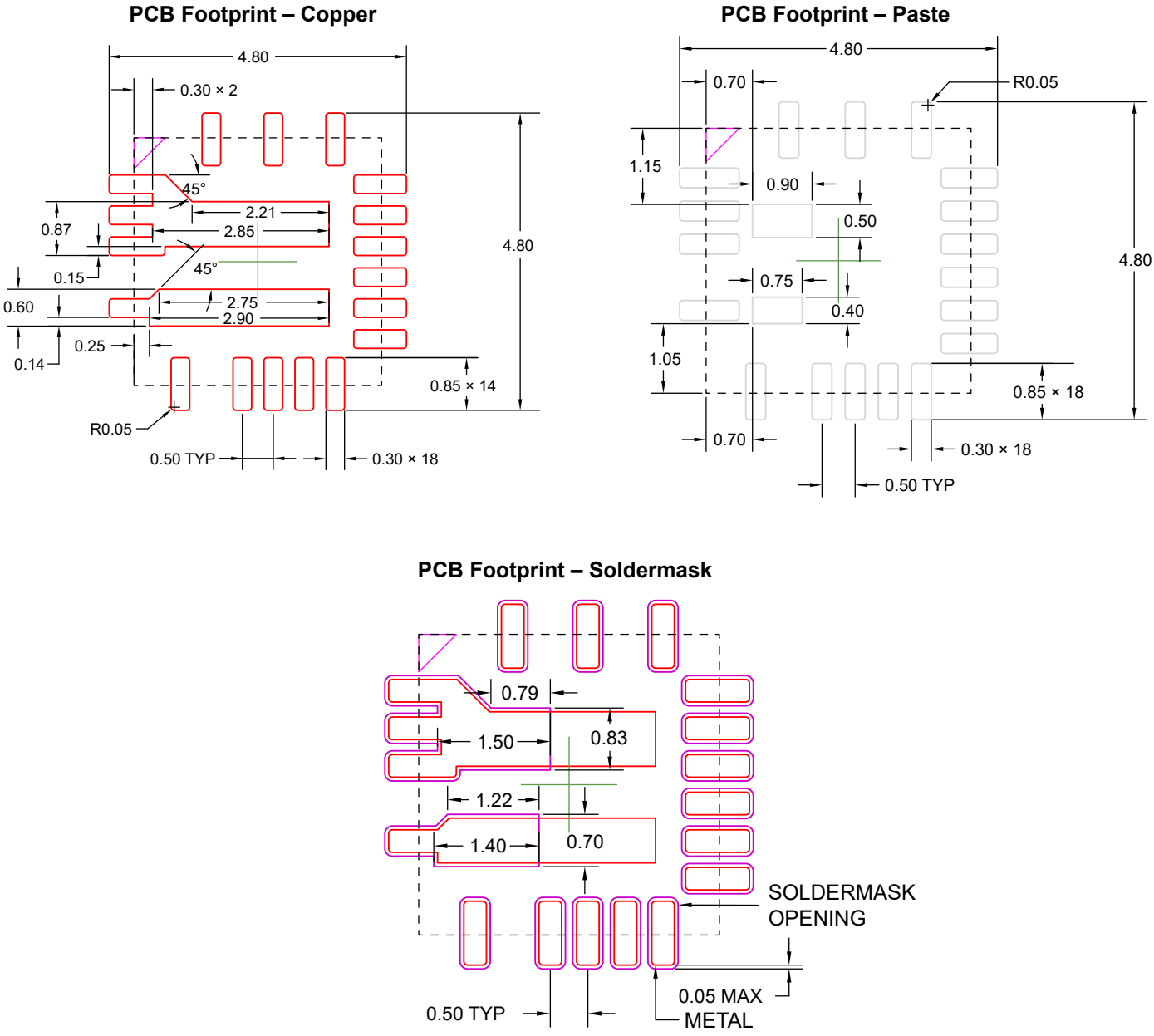

Figure 14: Recommended PCB Footprint

Altium and Cadence schematic and layout library files for the APM81815 are provided on the APM81815 product page on Allegromicro.com.

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Revision History

Number	Date	Description
–	October 17, 2024	Initial release
1	January 6, 2025	Updated characteristics of package thermal resistance (page 2) and input supply current, PWM mode (page 5)
2	March 18, 2025	Added footnote 2 to Input Supply Current, PWM Mode characteristic (page 5)

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