ATS17501

Dual Output Differential Speed and Direction Sensor IC

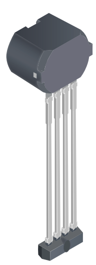
FEATURES AND BENEFITS

- High-speed switching bandwidth up to 40 kHz
- Two independent output channels with options for high-resolution XOR speed, pulse, and direction protocol
- ASIL-Compliant: ASIL B SEooC developed in accordance with ISO 26262, when used as specified in the safety manual
- Immune to common external magnetic disturbance
- EEPROM enables factory traceability throughout product life cycle
- Also available without integrated magnet (see the A17501 datasheet)

ISO 26262 ASIL Compliant

SOLIDSPEED DIGITAL ARCHITECTURE

PACKAGE:



4-Pin SIP (suffix SG)

Not to scale

DESCRIPTION

The ATS17501 is a single IC solution designed for rotational position sensing of a ferrous gear target found in automotive and industrial electric-motor applications (often with specific application and safety requirements). The IC is housed in an SG package that incorporates a rare-earth magnetic pellet for ease of manufacturing, consistent application performance over temperature, and enhanced reliability.

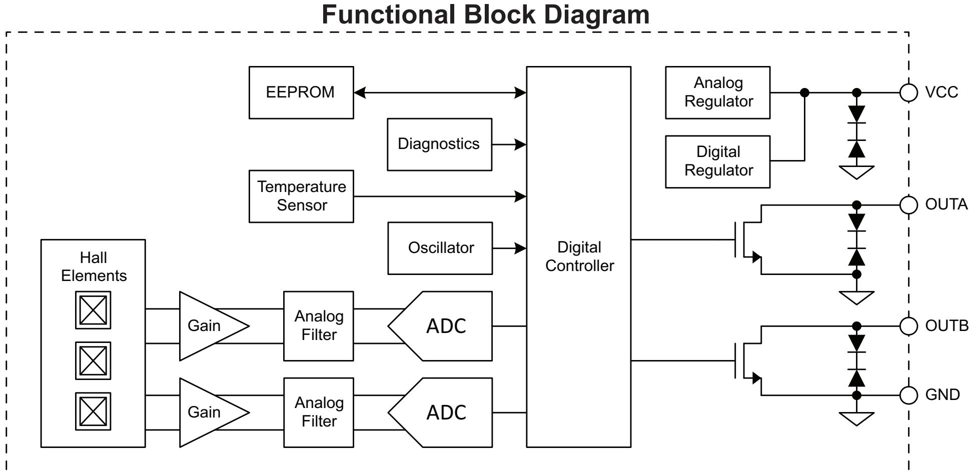
Three Hall elements are incorporated to create two independent differential channels. These inputs are processed by digital circuits and robust algorithms designed to eliminate the detrimental effects of magnetic and system offsets, and to address false output transitions caused by target vibrations in electric motors at startup and low-speed operation. The differential signals are used to produce a highly accurate speed output and, if desired, provide data regarding the direction of rotation.

Advanced calibration techniques are used to optimize signal offset and amplitude. This calibration, combined with the digital tracking of the signal, results in accurate switch points over air gap, speed, and temperature.

The IC can be programmed for a variety of applications requiring dual-phase gear speed and position signal data or simultaneous high-resolution gear speed and direction data. It can be configured to enable fault-detection mode for ASIL B utilization. The ATS17501 was developed in accordance with ISO 26262 as a hardware safety element out of context (SEooC) with ASIL B capability for use in automotive safety-related systems when integrated and used in the manner prescribed in the applicable safety manual and datasheet.

The ATS17501 SG package is a lead (Pb) free 4-pin single inline package (SIP) with an integrated back-biasing magnet and a 100% matte-tin-plated lead frame.

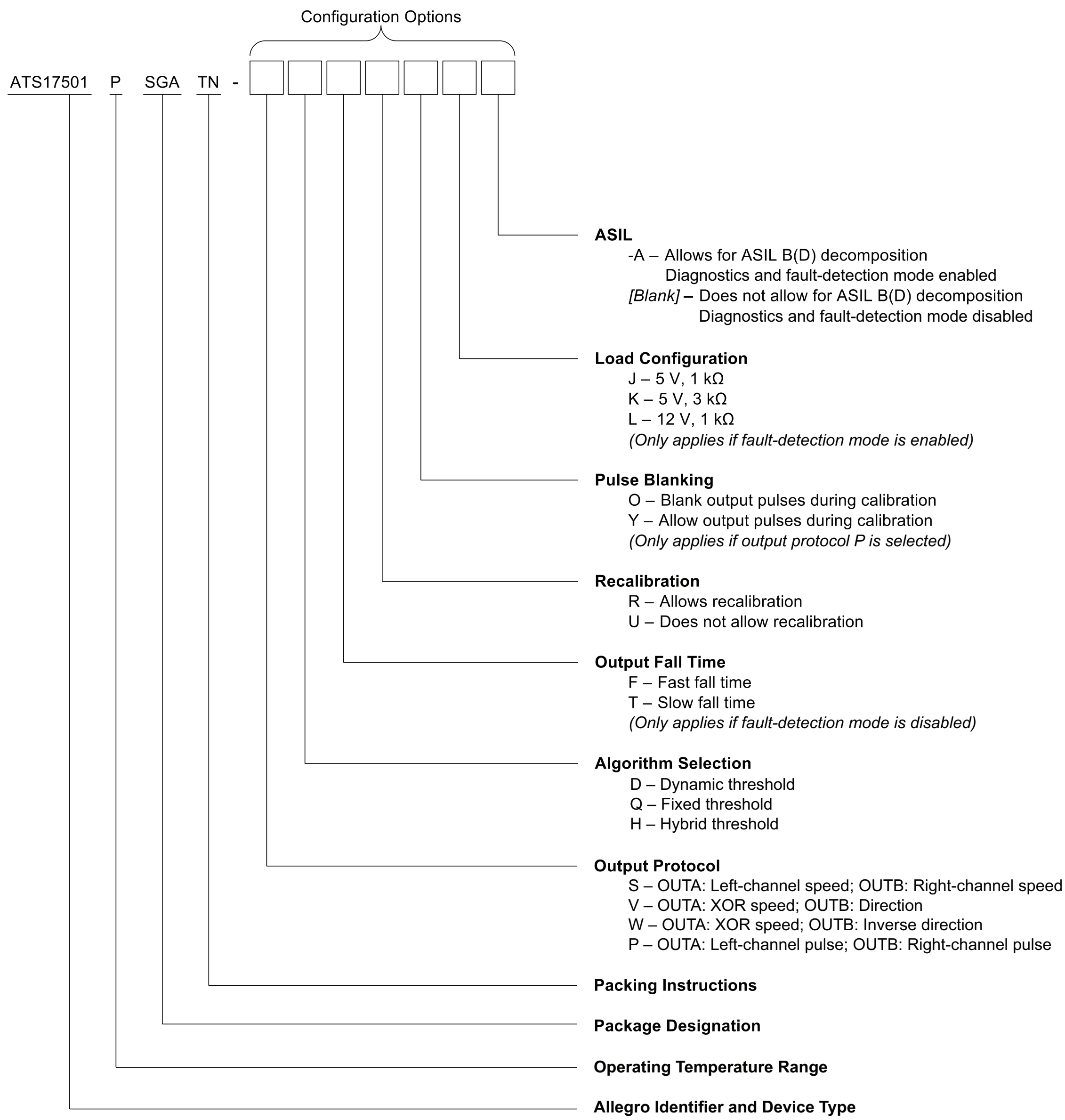
Functional Block Diagram



SELECTION GUIDE [1]

Part Number	Packing
ATS17501PSGATN-SDFUYJ	800 pieces per 13-inch reel
ATS17501PSGATN-VDFUYJ	
ATS17501PSGATN-WDFUYJ	
ATS17501PSGATN-SDFUYK-A	

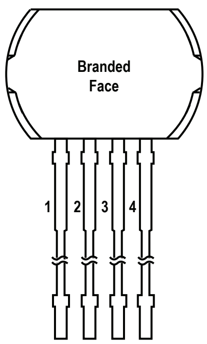
[1] Not all selectable combinations are available, contact Allegro for additional selections and packing options.



ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}	Refer to the Power Derating section	28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Output Voltage	V_{OUT}	Each output pin	28	V
Reverse Output Voltage	V_{ROUT}	Each output pin; R_{PULLUP} ≥ 1 kΩ	–0.5	V
Output Sink Current	I_{OUT}	Short-term output current for OUTA and OUTB independently; not intended for continuous operation	50	mA
Operating Ambient Temperature Range	T_A		–40 to 160	°C
Junction Temperature	T_J		175	°C
Storage Temperature Range	T_{stg}		–65 to 170	°C

PINOUT DIAGRAM



SG Package, 4-Pin SIP

PINOUT TABLE

Name	Pin	Function
VCC	1	Supply Voltage
OUTA	2	Configurable Output A
OUTB	3	Configurable Output B
GND	4	Ground

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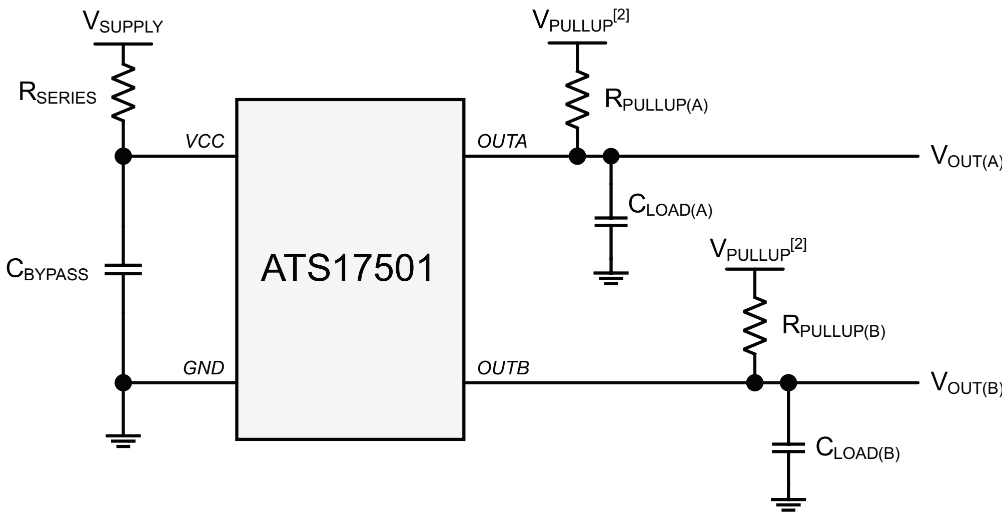
TYPICAL APPLICATION CIRCUIT



COMPONENTS [3]

Characteristic	Symbol	Notes	Value (Typ.)	Unit
Series Resistance	R_{SERIES}	Recommended for typical EMC requirements	100	Ω
OUTA Pullup Resistance	$R_{PULLUP(A)}$	Required for functional operation; recommended value dependent on programming options	1	kΩ
OUTB Pullup Resistance	$R_{PULLUP(B)}$	Required for functional operation; recommended value dependent on programming options	1	kΩ
Bypass Capacitance	C_{BYPASS}	Recommended for typical EMC requirements	100	nF
OUTA Load Capacitance	$C_{LOAD(A)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF
OUTB Load Capacitance	$C_{LOAD(B)}$	Recommended for typical EMC requirements; required for certain programming options	2.2	nF

[2] V_{PULLUP} may be connected to V_{CC} if V_{CC} meets V_{PULLUP} requirements. See the Operating Characteristics section.
[3] Components listed are typical recommended values and are not suited for all applications and/or programmable options. For more information, see the Operating Characteristics section and the Selection Guide.

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OPERATING CHARACTERISTICS : Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [4]	Max.	Unit
ELECTRICAL SUPPLY CHARACTERISTICS							
Supply Voltage [5]	V_{CC}	Voltage across VCC and GND		4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$			–	–	3.99	V
Supply Current	I_{CC}			–	10	15	mA
Reverse Supply Current	I_{RCC}	V_{CC} = –18 V		–10	–	–	mA
ELECTRICAL PROTECTION CHARACTERISTICS							
Supply Clamp Voltage	$V_{CSUPPLY}$	T_A = 25°C; I_{CC} = 18 mA		28	–	–	V
Reverse Supply Clamp Voltage	$V_{RCSUPPLY}$	T_A = 25°C; I_{CC} = –3 mA		–	–	–18	V
Output Clamp Voltage	V_{COUT}	T_A = 25°C; I_{OUT} = 3 mA		28	–	–	V
Output Current Internal Limiter	$I_{OUT(LIM)}$	Current limited by design for short-circuit event on OUTA and OUTB independently; low-impedance output state		30	55	85	mA
POWER-ON CHARACTERISTICS							
Power-On State	POS	For OUTA and OUTB		$V_{OUT(HIGH)}$			V
Power-On Time	t_{PO}	Time from when V_{CC} > $V_{CC(min)}$ to when sensor IC output is valid		–	–	1	ms
CALIBRATION CHARACTERISTICS							
First Output Edge	–	Amount of target rotation with constant direction following t_{PO} until first electrical output transition; -D algorithm selection; see Figure 1		–	1	–	T_{CYCLE}
Initial Calibration	–	Amount of target rotation with constant direction following t_{PO} until first valid speed and direction output; -D algorithm selection; see Figure 1		–	2	–	T_{CYCLE}
OUTPUT CHARACTERISTICS [6]							
Output Low Voltage	$V_{OUT(LOW)}$	Fault-detection mode disabled; I_{OUT} = 10 mA		–	0.165	0.35	V
		Fault-detection mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	0.5	–	1.25	V
			12 V, 1 kΩ option	1.2	–	3.6	V
Output High Voltage	$V_{OUT(HIGH)}$	Fault-detection mode disabled		–	V_{PULLUP}	–	V
		Fault-detection mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	3.75	–	4.5	V
			12 V, 1 kΩ option	8.4	–	10.8	V

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[4] Typical values are at T_A = 25°C and V_{CC} = 5 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[5] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative for Power Derating discussions.
[6] Output characteristics are valid for each output independently, unless otherwise specified.

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OPERATING CHARACTERISTICS (continued): Valid throughout operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [7]	Max.	Unit
OUTPUT CHARACTERISTICS (continued) [8]							
Fault Voltage [9]	V_{FAULT}	Fault-detection mode enabled; 5 V, 1 kΩ or 5 V, 3 kΩ option	High fault ($V_{FAULT(HIGH)}$)	4.5	–	–	V
			Mid fault ($V_{FAULT(MID)}$)	1.25	–	3.75	V
			Low fault ($V_{FAULT(LOW)}$)	–	–	0.5	V
		Fault-detection mode enabled; 12 V, 1 kΩ option	High fault ($V_{FAULT(HIGH)}$)	10.8	–	–	V
			Mid fault ($V_{FAULT(MID)}$)	3.6	–	8.4	V
			Low fault ($V_{FAULT(LOW)}$)	–	–	1.2	V
Allowable Pullup Voltage	V_{PULLUP}	Fault-detection mode disabled		4	–	24	V
		Fault-detection mode enabled	5 V, 1 kΩ or 5 V, 3 kΩ option	4.75	–	5.25	V
			12 V, 1 kΩ option	11.4	–	12.6	V
Allowable Pullup Resistor [10]	R_{PULLUP}	Fault-detection mode disabled		–	1	–	kΩ
		Fault-detection mode enabled	5 V, 1 kΩ option	0.8	–	1.46	kΩ
			5 V, 3 kΩ option	1.46	–	3.4	kΩ
			12 V, 1 kΩ option	0.9	–	1.1	kΩ
Allowable Load Capacitor [11]	C_{LOAD}	Fault-detection mode enabled		1	–	–	nF
Output Leakage Current	$I_{OUT(OFF)}$	Fault-detection mode disabled; $V_{OUT} = V_{OUT(HIGH)}$		–	–	10	µA
Duty Cycle	D	Using reference target 60-0; dynamic threshold option; f_{OP} < 1 kHz; -SD output protocol and algorithm selection		45	50	55	%
Output Rise Time	t_r	10%→90%; V_{PULLUP} = 5 V; R_{PULLUP} = 1 kΩ; C_{LOAD} = 2.2 nF		–	5	–	µs
Output Fall Time	t_f	90%→10%; V_{PULLUP} = 5 V; R_{PULLUP} = 1 kΩ; C_{LOAD} = 2.2 nF	Fault-detection mode disabled; Fast fall time option	–	0.5	–	µs
			Fault-detection mode disabled; Slow fall time option	–	3.5	–	µs
			Fault-detection mode enabled	–	6	–	µs
Forward Pulse Width [12]	$t_{w(FWD)}$	-P output protocol; Target features pass by sensor IC branded face pin 1 to pin 4		38	45	52	µs
Reverse Pulse Width [12]	$t_{w(REV)}$	-P output protocol; Target features pass by sensor IC branded face pin 4 to pin 1		76	90	104	µs
Propagation Delay	t_d	Delay from the magnetic signal crossing a switch point threshold to the start of the output transition		–	8	–	µs

Continued on next page...

[7] Typical values are for V_{CC} = 5 V and T_A = 25°C, unless otherwise specified.
[8] Output characteristics are valid for each output independently, unless otherwise specified.
[9] Valid with fault-detection mode enabled and correct programming of the fault-detection load circuit option; see the Selection Guide.
[10] See the Typical Application Circuit section.
[11] Minimum capacitor required when fault-detection mode is enabled to ensure correct output levels over operating conditions. Increased load capacitance directly impacts maximum operating frequency due to the increased rise and fall times; see the Typical Application Circuit section..
[12] Time from start of output transition from $V_{OUT(HIGH)}$ to $V_{OUT(LOW)}$ to start of output transition from $V_{OUT(LOW)}$ to $V_{OUT(HIGH)}$. Measured pulse width varies with load-circuit configurations and measurement thresholds. Valid with pulse or pulse inverted output protocol; see the Programming Options section.

OPERATING CHARACTERISTICS (continued): Valid over operating ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions		Min.	Typ. [14]	Max.	Unit
SWITCH POINT CHARACTERISTICS							
Operate Point	B_{OP}	% of $B_{DIFF(pk-pk)}$; $V_{OUT} = V_{OUT(LOW)} \rightarrow V_{OUT} = V_{OUT(HIGH)}$; -D algorithm selection		–	70	–	%
Release Point	B_{RP}	% of $B_{DIFF(pk-pk)}$; $V_{OUT} = V_{OUT(HIGH)} \rightarrow V_{OUT} = V_{OUT(LOW)}$; -D algorithm selection		–	30	–	%
Hysteresis	B_{HYS}	ΔB_{DIFF} after switch point to allow next output transition	% of $B_{DIFF(pk-pk)}$; -D algorithm selection	–	40	–	%
			-Q algorithm selection	–	10	–	G
INPUT CHARACTERISTICS							
Operating Frequency	f_{OP}	Fundamental frequency of the input magnetic signal	-S output protocol	0	–	40	kHz
			-V or -W output protocol	0	–	20	kHz
Forward Pulse Operating Frequency	$f_{OP(FWD)}$	-P output protocol		0	–	9	kHz
Reverse Pulse Operating Frequency	$f_{OP(REV)}$	-P output protocol		0	–	6	kHz
Operating Magnetic Input Signal Variation [15]	$\Delta B_{DIFF(pk-pk)}$	Bounded amplitude ratio within T_{WINDOW}; no missed output transitions; possible incorrect direction data and/or reduction in switch-point accuracy; see Figure 3 and Figure 4		0.6	–	2	–
Operating Magnetic Input Signal Variation Window	T_{WINDOW}	Rolling window in which $\Delta B_{DIFF(pk-pk)}$ cannot exceed bounded ratio; see Figure 3 and Figure 4		8	–	–	T_{CYCLE}
Operating Air Gap [16]	AG	Using Reference Target 60-0; f_{OP} < 10 kHz; -D algorithm selection	Fault-detection mode disabled	0.75	–	3	mm
			Fault-detection mode enabled	0.75	–	2.75	mm
THERMAL CHARACTERISTICS							
Package Thermal Resistance	$R_{\theta JA}$	Minimum-K PCB, single-layer, single-sided, with copper limited to solder pads		–	126	–	°C/W
		Low-K PCB, single-layer, single-sided, with copper limited to solder pads and 3.57 in.^{2} (23.03 cm^2) of copper area each side		–	84	–	°C/W

[14] Typical values are for V_{CC} = 5 V and T_A = 25°C, unless otherwise specified.
[15] Operating magnetic input variation is valid for symmetrical peak variation about the signal offset. $B_{DIFF(pk-pk)}$ must always be greater than $B_{DIFF(pk-pk,min)}$.
[16] Operating air gap is dependent on the available magnetic field. The available magnetic field is target geometry, material, and speed dependent. Operational air gap should be independently characterized for each target.

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REFERENCE

Definition of Terms

T_{CYCLE}

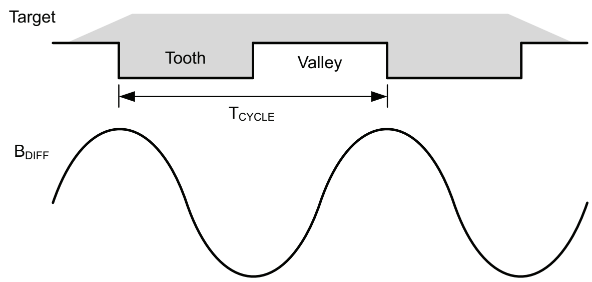

Figure 1: Definition of T_{CYCLE}

T_{CYCLE} = Target Cycle; the amount of rotation that moves one tooth and valley across the sensor.

B_{DIFF} = The differential magnetic flux density sensed by the IC.

Differential Magnetic Input

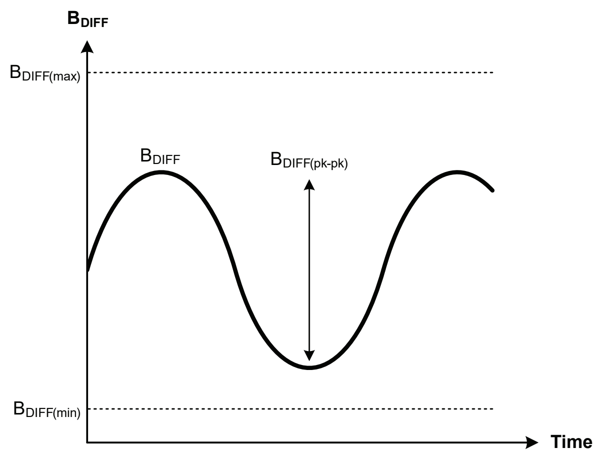

Figure 2: Differential Magnetic Input

$B_{DIFF(pk-pk)}$ = The peak-to-peak magnetic flux density sensed by the IC.

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Operating Magnetic-Signal Variation and Window

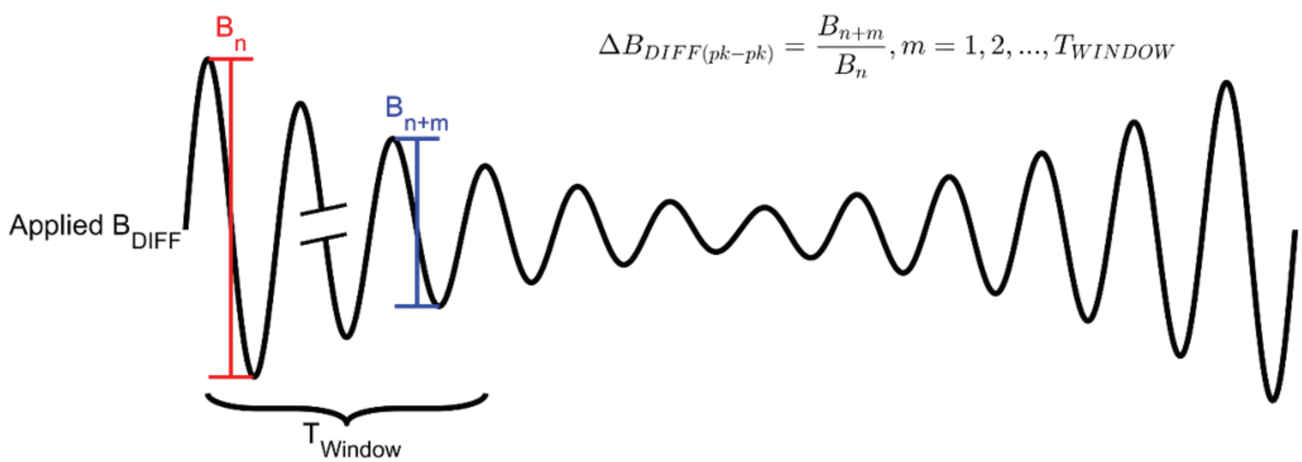

Figure 3: Repeated-Period Variation

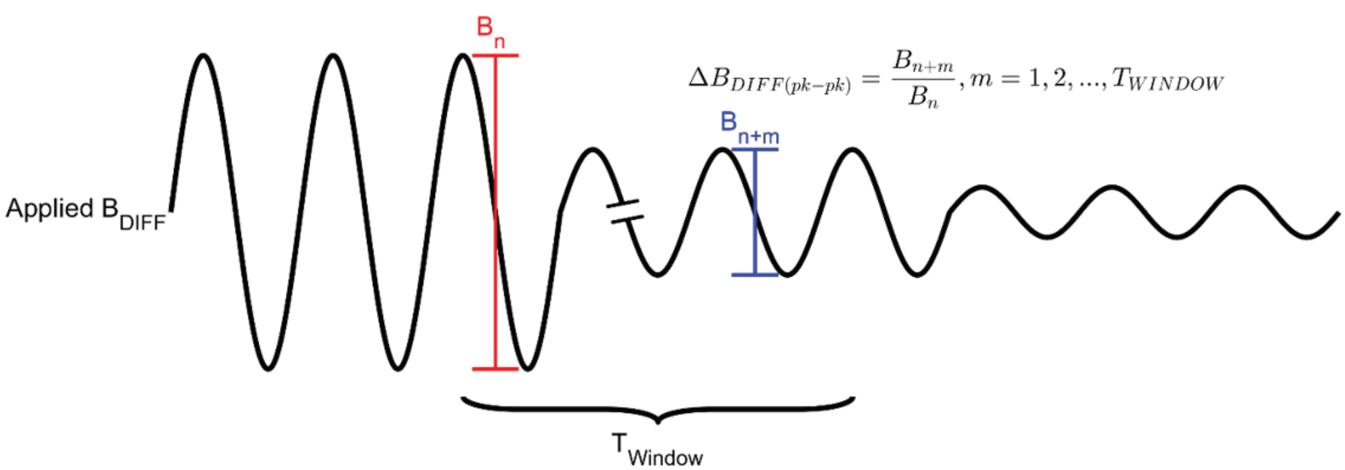

Figure 4: Single-Period Variation

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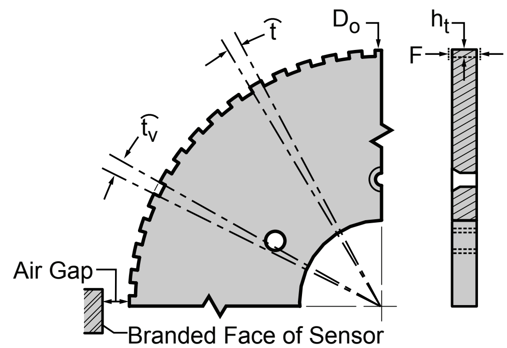
REFERENCE TARGET CHARACTERISTICS: Allegro Reference Target 60-0

Characteristics	Symbol	Test Conditions	Typ.	Units	Symbol Key
Outside Diameter	D_o	Outside diameter of target	120	mm	
Face Width	F	Breadth of tooth, with respect to branded face of the Sensor IC	6	mm	
Circular Tooth Length	t	Length of tooth, with respect to branded face of the Sensor IC	3	degrees	
Circular Valley Width	t_v	Length of valley, with respect to branded face of the Sensor IC	3	degrees	
Tooth Whole Depth	h_t		3	mm	
Material		Low Carbon Steel	–	–	

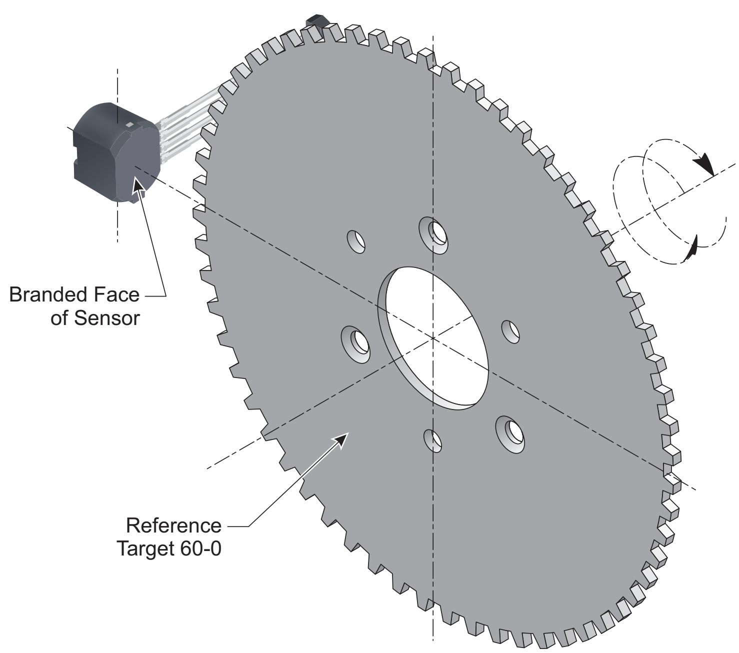


Figure 5: Reference Target 60-0

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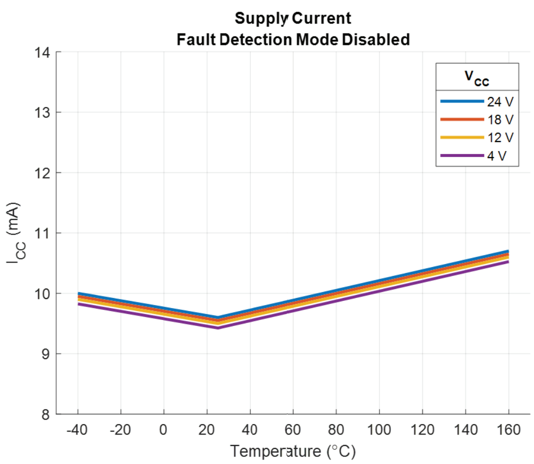
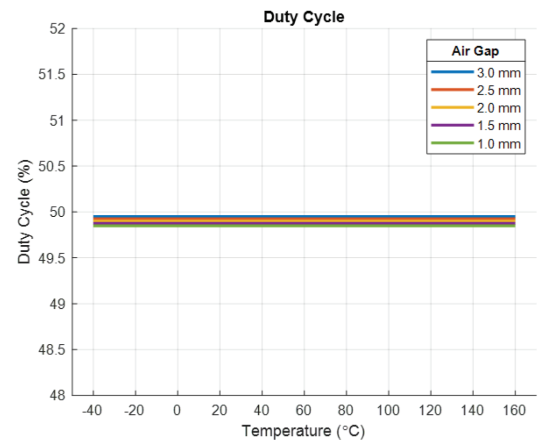
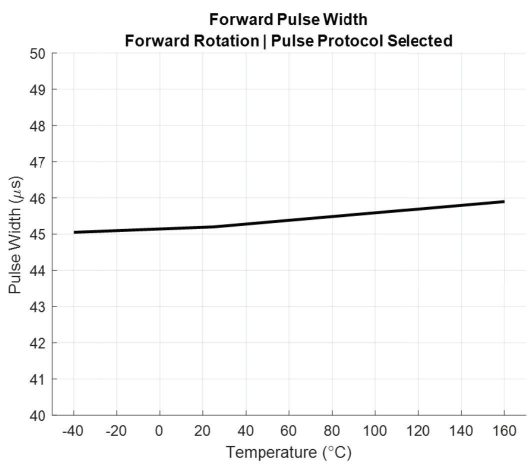
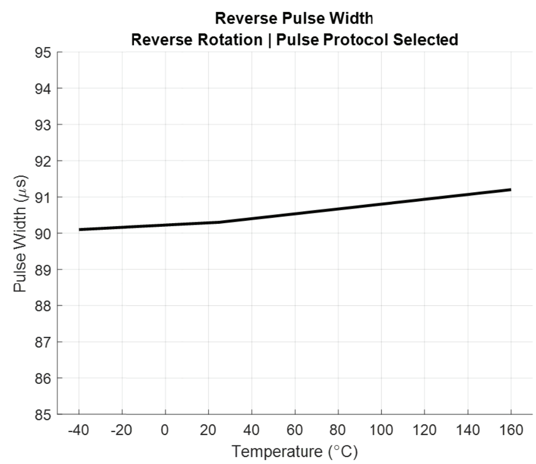
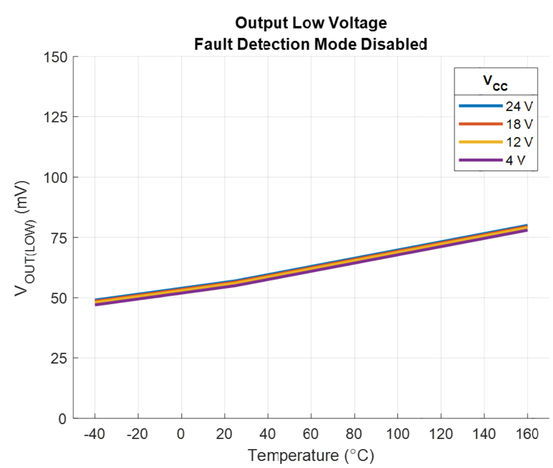
CHARACTERIZATION PLOTS [18]











[18] Characterization data representative of distribution averages. Characterization tested with dynamic threshold algorithm at f_{OP} = 1 kHz, V_{CC} = 5 V, V_{PULLUP} = 5 V, R_{PULLUP} = 1 kΩ, and C_{LOAD} = 2.2 nF unless otherwise specified.

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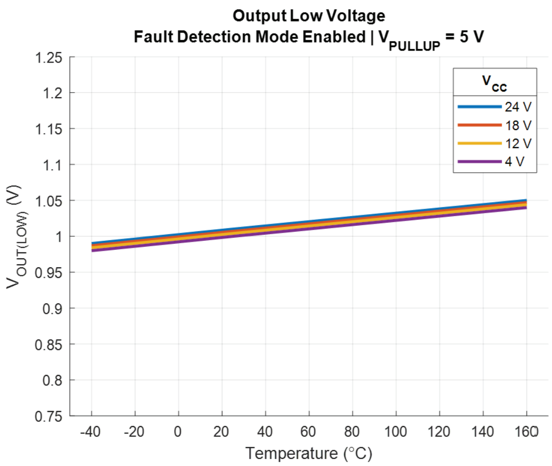
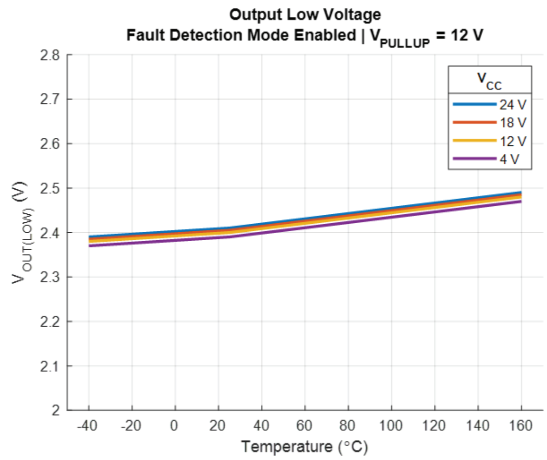
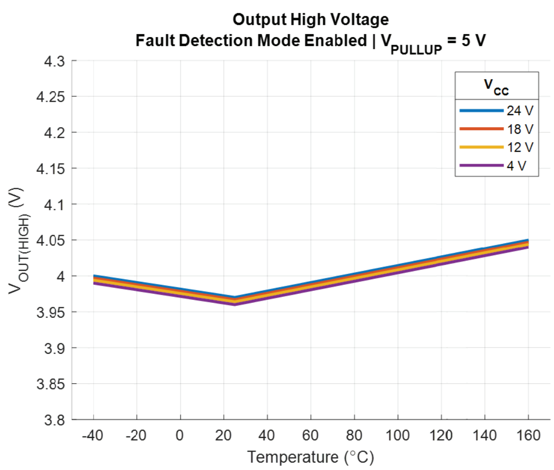


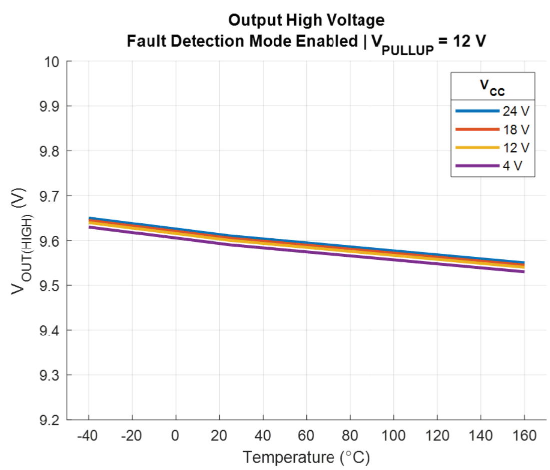
Output Low Voltage
Fault Detection Mode Enabled | V_PULLUP = 5 V
V_CC
24 V
18 V
12 V
4 V
V_OUT(LOW) (V)
Temperature (°C)



Output Low Voltage
Fault Detection Mode Enabled | V_PULLUP = 12 V
V_CC
24 V
18 V
12 V
4 V
V_OUT(LOW) (V)
Temperature (°C)



Output High Voltage
Fault Detection Mode Enabled | V_PULLUP = 5 V
V_CC
24 V
18 V
12 V
4 V
V_OUT(HIGH) (V)
Temperature (°C)



Output High Voltage
Fault Detection Mode Enabled | V_PULLUP = 12 V
V_CC
24 V
18 V
12 V
4 V
V_OUT(HIGH) (V)
Temperature (°C)

FUNCTIONAL DESCRIPTION

General

The ATS17501 sensor module contains a single-chip, dual differential Hall-effect sensor IC, a rare-earth pellet, and a flat ferrous pole piece (concentrator). As shown in Figure 6, the Hall-effect sensor IC supports three Hall elements that sense the magnetic profile of the ferrous gear target simultaneously but at different points (each channel spaced at 1.75 mm pitch), generating two differential internal signals processed for precise switching of the digital output signals. Direction of rotation can be determined based on the phase relationship of the two differential internal signals. The ATS17501 is intended for use with ferromagnetic targets.

The Hall-effect sensor IC is self-calibrating and possesses a temperature-compensated amplifier as well as a full-range analog-to-digital converter (ADC). This allows for accurate processing of a wide range of target magnetic-profile amplitudes and offsets. The on-chip voltage regulator provides supply-noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect the ATS17501 due to the stable amplifier design and full-range ADC. The Hall elements and signal-processing electronics are integrated on the same silicon substrate.

The ATS17501 is capable of providing digital data representative of the mechanical features of a rotating target gear. The automatic translation of the mechanical profile to the digital output signal is shown in Figure 6. Additional optimization is not needed, and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

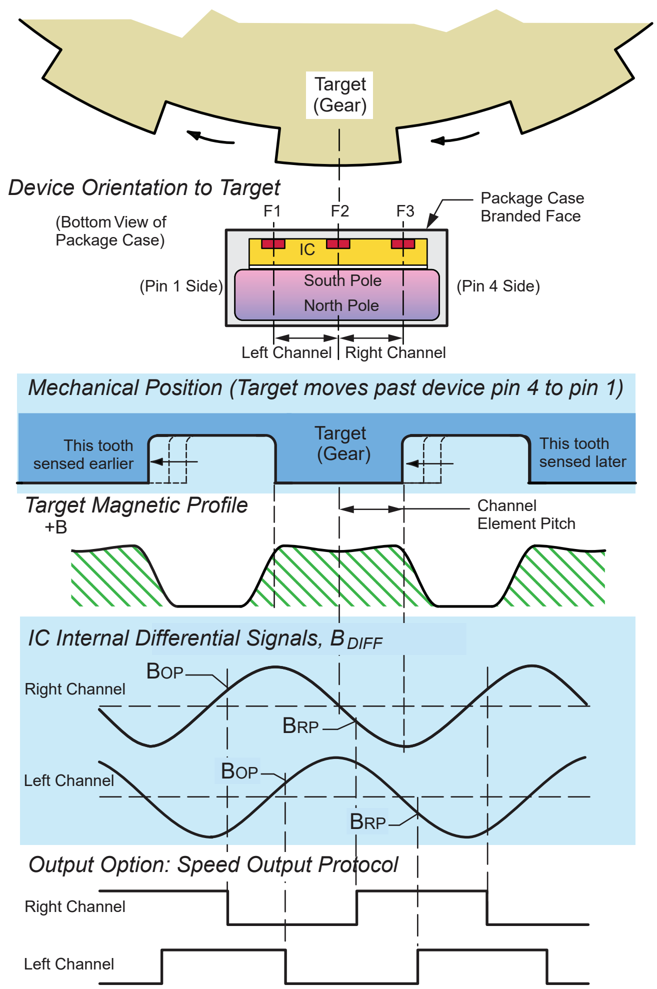


Figure 6: Magnetic Profile and Switch Points (B_{OP} = 70%, B_{RP} = 30%)

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Threshold Algorithms

The ATS17501 contains selectable algorithms for determining when to produce an output transition from the magnetic input signal. For all options, a threshold is set within the sensor IC that triggers the output transition when crossed by the digitized magnetic signals (switch point).

Dynamic Threshold

With the ATS17501 programmed for the dynamic threshold option, each switch point is calculated from data obtained from the previous target feature. This algorithm allows for robust tracking to produce accurate output transitions for inconsistent magnetic input signals (offset drift, amplitude changes, etc.).

After power-on, the magnetic input signal is tracked to find the peaks of the signal. After each new peak is found, the switch points are updated based on a percentage of the previous two peaks.

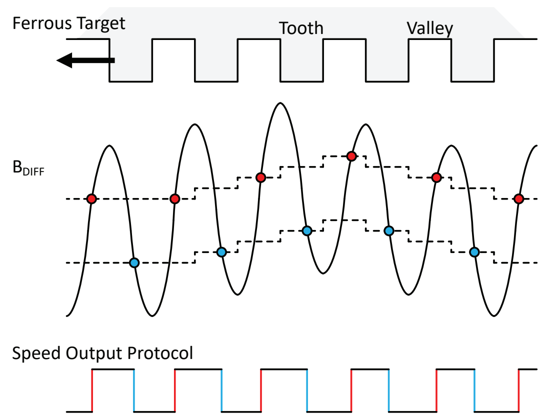

Figure 7: Dynamic Threshold Option Switch Point Algorithm (B_{OP} = 70%, B_{RP} = 30%)

Fixed Threshold

With the ATS17501 programmed for the fixed threshold option, an absolute threshold stored in memory is used to set the switch point for both the operate point and the release point. This algorithm allows for accurate output transitions immediately after power-on for consistent magnetic input signals without the need to "learn" the signal. The threshold stored in memory and loaded during power-on contains threshold levels over temperature to allow for offset drift adjustment of the magnetic input signal over temperature. The ATS17501 sensor IC contains a temperature sensor used continuously to adjust the switch point over temperature as needed by the application.

The fixed thresholds stored in memory can be preprogrammed for unique switch points over temperature for each application. Additionally, the ATS17501 can find and set the threshold for each installation over temperature during end-of-line calibration.

If, during the application, the magnetic input signal offset does not match the programmed threshold stored in memory (due to inaccurate programming, mechanical shift, etc.), the ATS17501 identifies the threshold as out of range, calculates the threshold for the current temperature, and updates the threshold to produce correct output transitions. After the update, algorithms use the current temperature to recharacterize the threshold over the operational temperature range. This prevents the update from overcompensating the threshold at a distant temperature relative to the update temperature. After the updated threshold is confirmed to be within the magnetic input signal's switch point range over several target features, the updated threshold is stored into memory such that it can be used for subsequent power-on cycles.

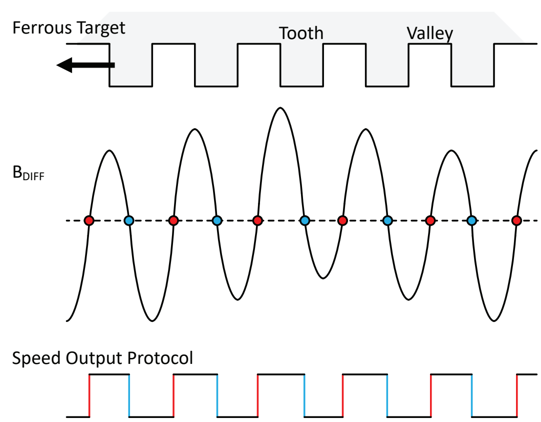

Figure 8: Fixed Threshold Option Switch Point Algorithm

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Hybrid Threshold

With the ATS17501 programmed for the hybrid threshold option, the threshold is determined from the fixed threshold option at startup, then transitions to the dynamic threshold option after tracking signals have correctly acquired the magnetic input signals. This algorithm allows for both accurate output transitions immediately following power-on for consistent magnetic input signals as well as robust tracking to produce accurate output transitions of inconsistent magnetic input signals (offset drift, amplitude changes, etc.).

Once the tracking signals have identified consistent peak values from the magnetic input signal, the algorithm transitions from using the fixed threshold switch point to using the dynamic threshold switch points. This transition occurs only when the magnetic input signal is near a maximum or minimum value, such that double-switching on the transition can be avoided.

While the majority of the power-on uses the dynamic threshold option for robust signal tracking, the ATS17501 continues to monitor the fixed threshold for comparison to the fixed threshold stored in memory. Should the fixed threshold require an update, the ATS17501 updates and writes the new threshold to memory for use in subsequent power-on cycles.

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Output

Output Protocol

The ATS17501 contains several selectable options to change the output protocol or adjust the output behavior. These options allow for the ATS17501 to be programmed to application-level needs; see Figure 9. If the datasheet output protocol options are not quite fit for the application, consult Allegro MicroSystems about custom sensor programmability.

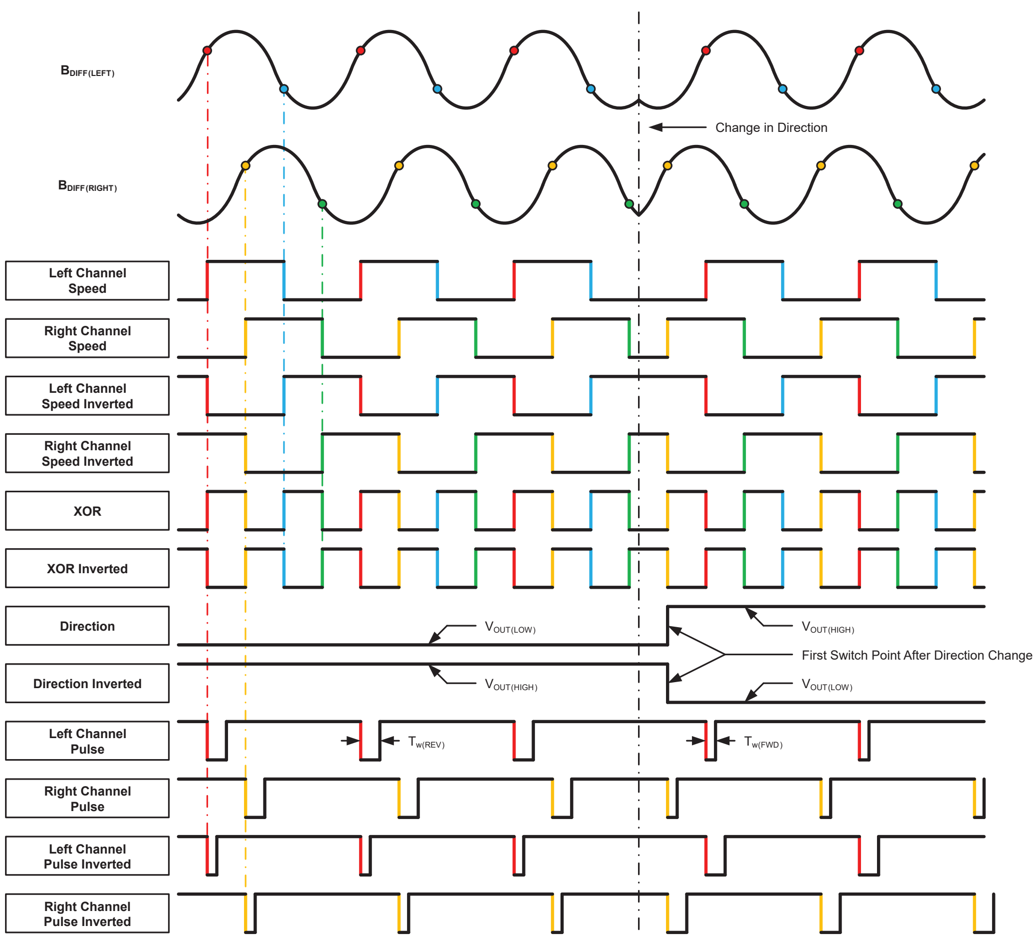

Figure 9: Output Protocol Options

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Fault-Detection Mode

The ATS17501 allows for the output to transition between one of two sets of values. With fault-detection mode disabled, the output transitions between approximately 0% and 100% of V_{PULLUP}; see Figure 10. With fault-detection mode enabled, the output transitions between approximately 20% and 80% of V_{PULLUP}; see Figure 11.

At the beginning of power-on, the ATS17501 outputs initialize to the V_{PULLUP} level. With fault-detection mode enabled, the output levels transition from V_{PULLUP} to V_{HIGH} before the end of power-on. After power-on, the output transitions as determined by the programmed algorithm and output protocol between $V_{OUT(HIGH)}$ and $V_{OUT(LOW)}$.

Enabling fault-detection mode allows for additional communication for cases of open wire or short circuit, as well as allowing for the ATS17501 to communicate a fault detected from the internal diagnostics. For a typical application load circuit, these cases can be detected by observing either OUTA or OUTB transition to approximately 0 V or V_{PULLUP} after t_{PO}.

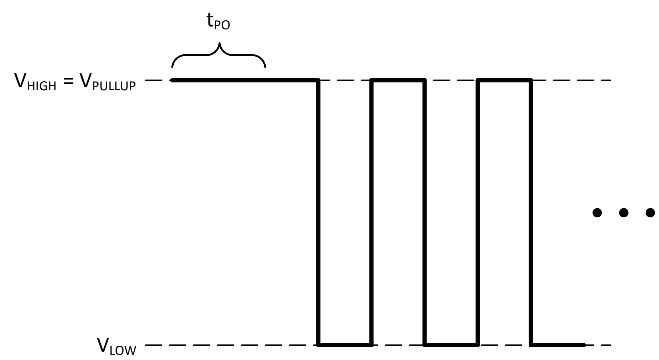

Figure 10: Fault-Detection Mode Disabled Output

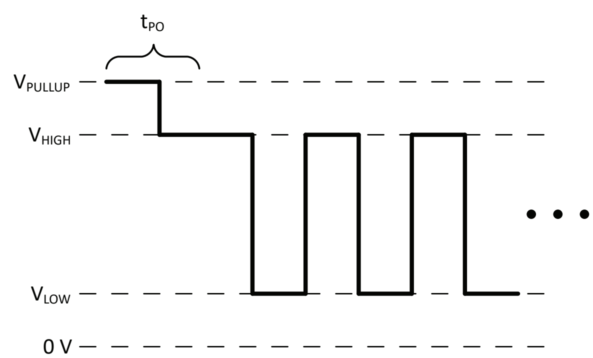

Figure 11: Fault-Detection Mode Enabled Output

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Fault Voltage

The ATS17501 communicates a fault condition by configuring either output to hold within one of three V_{FAULT} ranges (high, mid, and low) for greater than 1 millisecond. Typical operation allows for output transitions to occur over the $V_{FAULT(MID)}$ range; as such, it is necessary to ignore fast transients for less than 1 millisecond through this range.

For internal diagnostics that trigger fault conditions (force the output to go to V_{FAULT}), both outputs transition to the $V_{FAULT(HIGH)}$ range. Because there may exist internal or external faults that cause either or both output pins to hold a $V_{FAULT(MID)}$ or $V_{FAULT(LOW)}$ level, these fault ranges should also be monitored. Examples of these fault conditions could be a short circuit of the output to ground, forcing the output to $V_{FAULT(LOW)}$, or a fault in the IC output controller that forces the output to $V_{FAULT(MID)}$.

For examples of the output communicating a fault condition, see Figure 12, Figure 13, and Figure 14.

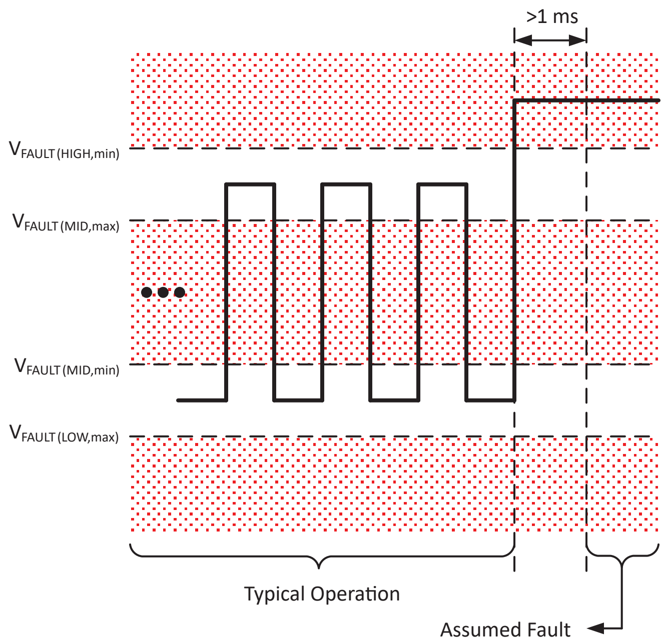

Figure 12: Assumed Fault Example: High Fault

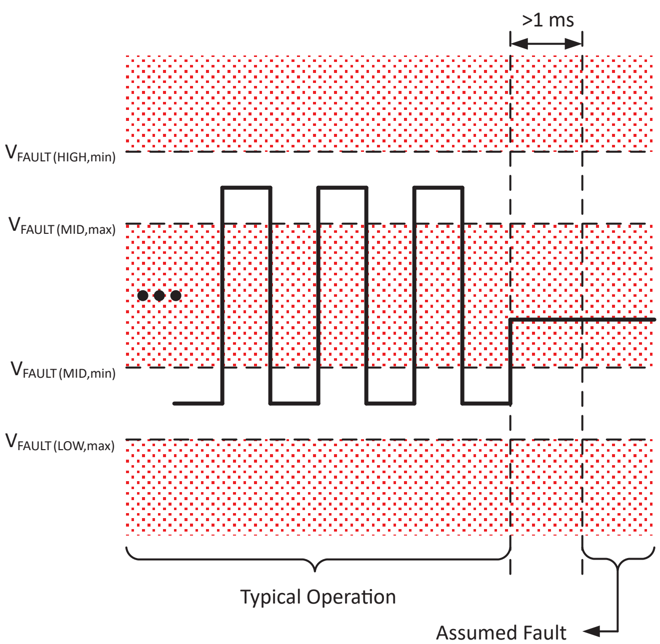

Figure 13: Assumed Fault Example: Mid Fault

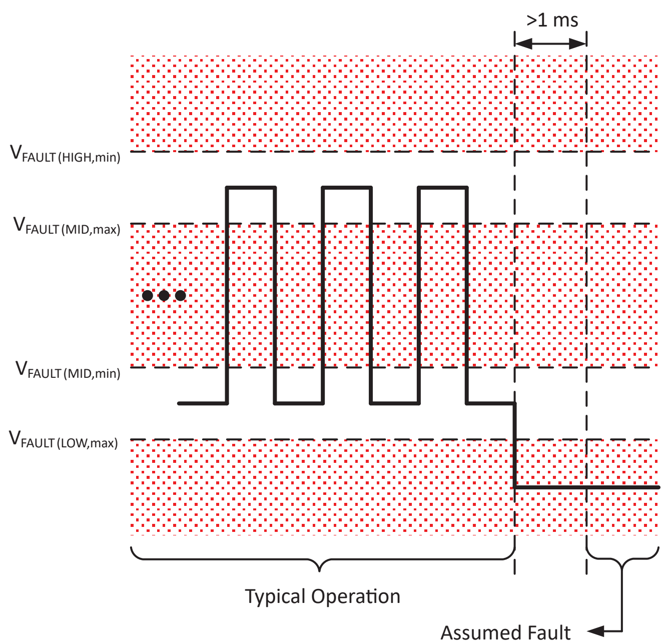

Figure 14: Assumed Fault Example: Low Fault

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DEVICE FEATURES

Undervoltage Lockout

When supply voltage reduces to less than the undervoltage-lockout voltage ($V_{CC(UV)}$), the ATS17501 enters reset, where the output state returns to the power-on state (POS) until sufficient V_{CC} is supplied. This feature prevents false signals, caused by undervoltage conditions, from propagating to the output of the sensor IC.

Power-Supply Protection

The ATS17501 contains an on-chip regulator and can operate over a wide V_{CC} range. For applications that need to operate from an unregulated power supply, transient protection must be added externally. For applications using a regulated line, electromagnetic interference (EMI)/radio-frequency interference (RFI) protection is recommended. For more information about circuitry to address electromagnetic-compatibility (EMC) requirement compliance, contact Allegro. Refer to the Typical Application Circuit section.

Startup Hysteresis

With a power-on and a target held at zero-speed ($f_{OP} \approx 0$ Hz), noise and/or vibration can produce magnetic input signals. Startup hysteresis prevents peak-tracking and switch-point setting at startup immediately following power-on. This occurs until the sensed differential magnetic signal has moved sufficiently to satisfy the hysteresis band for signal tracking. This feature helps to ensure optimal self-calibration of the magnetic signals by rejecting electrical noise and low-amplitude target vibrations during startup and ensures that calibration occurs on actual target features.

Small-Signal Lockout

When $B_{DIFF(pk\text{-}pk)}$ reduces to less than the specification, the internal logic of the sensor IC indicates a reduced signal, as measured in an excessive air gap or a vibration condition. Small-signal lockout holds the output state at the level when $B_{DIFF(pk\text{-}pk)}$ was last in-specification. Once $B_{DIFF(pk\text{-}pk)}$ returns to an in-specification value, the output state is released to transition as expected during typical operation. When direction data is not explicitly defined by the selected output protocol, small-signal lockout is controlled independently for each channel. For example, left-channel speed + right-channel speed output protocol allows for one channel to continue switching while the other is in lockout. When direction data is explicitly communicated, for example XOR + direction output protocol, small-signal lockout occurs when the $B_{DIFF(pk\text{-}pk)}$ of either channel reduces to less than the specification.

Vibration-Robust Signal Tracking

During vibration events, the magnetic input signals can produce oscillations with a sufficient amplitude for the peak-tracking algorithms to bound in and produce a nonideal peak-to-peak. When the ATS17501 detects a direction change, inward bounding of the peak-tracking signals is prevented. This prevents cases of erroneous output transitions from switch points being incorrectly set from vibration signals. Additionally, this allows for immediate acquisition of the magnetic input signals once real target rotation resumes following a vibration event.

Signature-Region-Robust Signal Tracking

Signature teeth (characterized by an extra target tooth and/or valley) can produce significant variations of the magnetic input signals. The bounded updating of the tracking signals prevents overcompensation for these signature variations to provide robust and accurate switch points for the signature region, as well as the features about the signature region.

Temperature-Drift-Robust Signal Tracking

Because temperature changes can impact both the amplitude and offset of the magnetic signal, a full-range ADC, advanced algorithms, temperature compensation, watchdog timers, and an internal temperature sensor ensure robust signal tracking over temperature.

To compensate for amplitude changes over temperature, temperature-compensated gain is first applied to normalize the amplitude over temperature. The full-range ADC and peak-tracking algorithms track and acquire the signal to accurately set the switch points.

To compensate for offset changes over temperature, two algorithms are implemented to ensure the signal tracking accurately follows and updates the switch points to follow the offset. With nominal target rotation, peak-tracking algorithms automatically follow and update the switch points over offset drift. With no target rotation (stopped condition), a watchdog timer is implemented, which adjusts the peaks to track together, allowing for preservation of the correct signal peak-to-peak and switch points once rotation resumes.

With the fixed-threshold algorithm option selected, algorithms are implemented for continuous monitoring and updating of the fixed threshold over temperature to follow the offset drift of the system. This compensation is implemented for each channel independently to provide robust tracking of both signal channels over temperature.

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Diagnostics and Fault Reporting

The ATS17501 contains diagnostics monitors of analog and digital circuits of the IC. These continuously monitor and report if any defect, calculation error, or invalid input stimulus is found. If a diagnostic monitor activates, the outputs of the ATS17501 transition to a V_{FAULT} level. For all faults, the outputs remain at the V_{FAULT} level for enough time to allow the system controller to monitor that a fault has occurred. For some diagnostics, it is possible to clear the fault with a reset of the internal controller of the sensor IC. If any of those diagnostic monitors triggers the fault event, the ATS17501 automatically performs a reset of the internal controller after the output is held at V_{FAULT} for enough time to allow the system controller to monitor the fault event.

For diagnostics and fault reporting to perform correctly, the user must ensure proper programming and must adhere to the specifications and assumptions stated in this datasheet, the ATS17501 Safety Manual, and any other addendum, corrigendum, and application note that applies to the ATS17501. For more information about diagnostics and fault reporting, see the ATS17501 Safety Manual.

Recalibration

Under large amplitude vibration conditions at startup, the peak-to-peak and phase relationship of the magnetic input signals can meet the conditions to calibrate. Once typical rotation resumes, the actual signal amplitudes can be much larger than the peak signals acquired during calibration. Rather than wait several T_{CYCLE} events for the peak signal to be tracked to actual levels, the ATS17501 detects the difference and recalibrates to the new signal. Recalibration allows for fast and robust correction from cases of calibration on vibration events.

Pulse-Collision Prevention

In cases of high-speed vibration, output transitions can occur at very high frequencies. To prevent pulse collision (truncation of the pulse width), the ATS17501 prevents output transitions until the current output-pulse transition is complete. This ensures the system controller can accurately interpret the output signal. This feature is only implemented when a pulse protocol option is selected.

High Configurability

The ATS17501 contains programmable parameters, as shown in the Selection Guide, that can be configured to provide application-level optimization.

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POWER DERATING

The device must be operated at less than the maximum junction temperature of the device ($T_{J(max)}$). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The package thermal resistance ($R_{\theta JA}$) is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity (K) of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case ($R_{\theta JC}$) is a relatively small component of $R_{\theta JA}$. Ambient air temperature (T_A) and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (power dissipation or P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D:

Equation 1: $P_D = V_{IN} \times I_{IN}$

Equation 2: $\Delta T = P_D \times R_{\theta JA}$

Equation 3: $T_J = T_A + \Delta T$

For example, given common conditions, such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC(avg)} = 8.5$ mA, and $R_{\theta JA} = 126°C/W$, then:

$$P_D = V_{CC} \times I_{CC(avg)} = 12\ V \times 8.5\ mA = 102\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 102\ mW \times 126°C/W = 12.9°C$$

$$T_J = T_A + \Delta T = 25°C + 12.9°C = 37.9°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

For example, calculating reliability of V_{CC} given observed worst-case ratings, specifically:

$T_A = 160°C$, $R_{\theta JA} = 126°C/W$, $T_{J(max)} = 175°C$, $V_{CC(max)} = 24$ V, and $I_{CC(max)} = 15$ mA.

The maximum allowable power, $P_{D(max)}$, can be calculated by first inverting Equation 3 and calculating the maximum allowable increase to T_J:

$$\Delta T_{max} = T_{J(max)} - T_A = 175°C - 160°C = 15°C$$

Then, maximum allowable power can be calculated by:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 126°C/W = 119\ mW$$

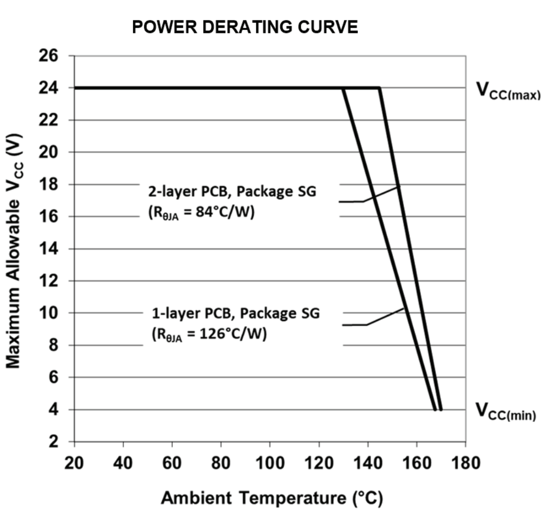
Finally, invert Equation 1 with respect to voltage:

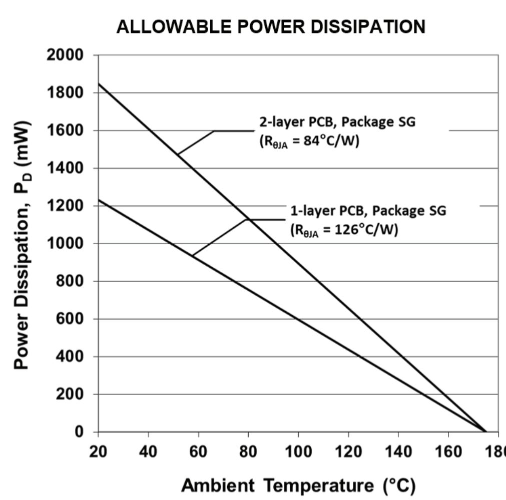
$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 119\ mW \div 15\ mA = 7.9\ V$$

The results indicate that, at T_A, the application and ATS17501 can dissipate adequate amounts of heat at voltages less than or equal to $V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$:

- If $V_{CC(est)} \leq V_{CC(max)}$, reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$.
- If $V_{CC(est)} \geq V_{CC(max)}$, operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.





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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000392)
Dimensions in millimeters. NOT TO SCALE.
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

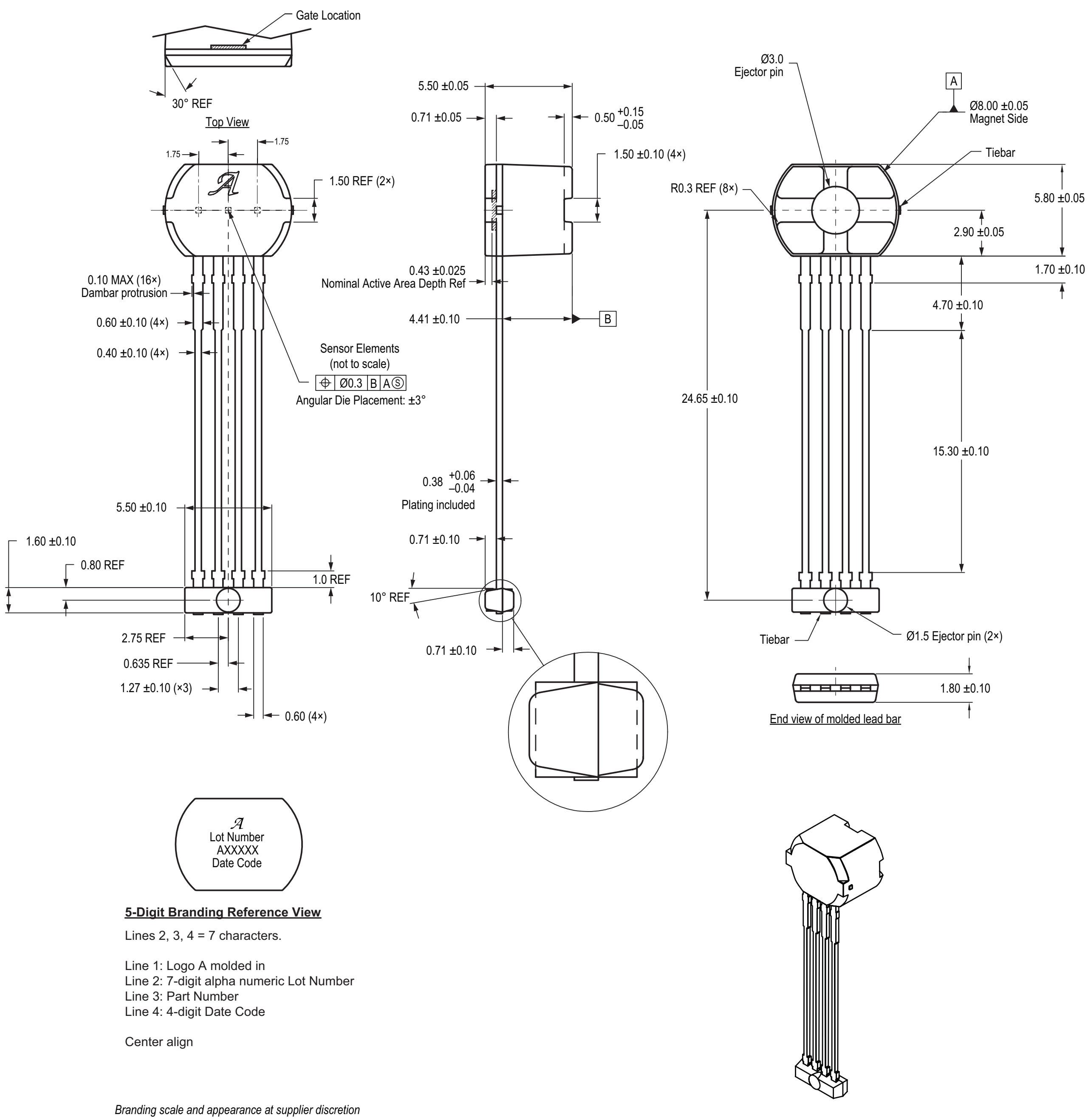

Figure 15: Package SG, 4-Pin SIP

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Revision History

Number	Date	Description
–	November 18, 2019	Initial release
1	February 27, 2020	Updated Selection Guide (page 2), Electrical Protection Characteristics names and symbols (page 5), Operating Air Gap maximum value (page 7)
2	March 19, 2020	Updated Features and Benefits (page 1); removed 50%/50% switch point options (updated Selection Guide (page 2), Output Current Internal Limiter test conditions (page 5), Operate Point, Release Point, and Hysteresis characteristics (page 7); removed 50%/50% Dynamic Threshold Option figure (page 14); updated Output Protocol Options figure (page 16), Startup Hysteresis section (page 19); removed Hidden Hysteresis (page 20))
3	February 22, 2021	Removed Advance Information status and ASIL assessment status; updated Selection Guide; minor editorial updates
4	August 2, 2021	Split Operating Air Gap specification into fault detection mode disabled and enabled (page 7)
5	September 1, 2022	Updated product outline drawing and corrected reference drawing number (page 22)
6	March 8, 2023	Updated Output Characteristics (page 6)
7	April 23, 2025	Changed ASIL logos and ASIL description for clarity (page 1); changed output clamp voltage symbol from V_{OUT} to V_{COUT} and modified test condition descriptions of first output edge, initial calibration, duty cycle, and forward/reverse pulse width (pages 5 and 6); removed jitter characteristic (page 6); removed operating magnetic input and operating magnetic input peak characteristics and modified test conditions and notes for switch point characteristics and input characteristics (page 7); modified description of output protocol (page 16); and made minor editorial changes throughout

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