

A8650 Evaluation Board User Guide

DESCRIPTION

This evaluation board is used to demonstrate the operation and performance of the Allegro A8650 synchronous buck regulator module.

FEATURES

- A8650 synchronous buck converter
- Test points for input and output power and easy access to common signals of interest
- Configured for 1.8 V output voltage at up to 2 A with a 2 MHz switching frequency

EVALUATION BOARD CONTENTS

- APEK8650 evaluation board

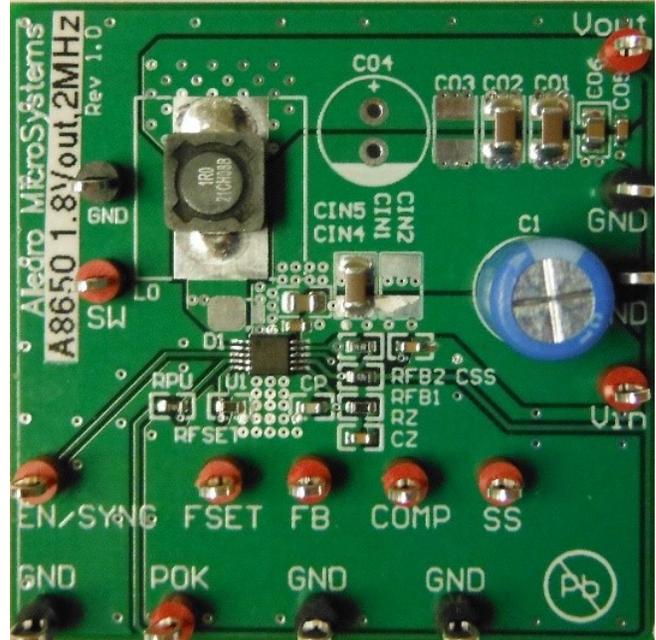


Figure 1: APEK8650 Evaluation Board

Table 1: A8650 Evaluation Board Configurations

Part Number	Package	Output Voltage
APEK8650KLY-01-MH	eMSOP-10	1.8 V

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Table 2: General Specifications

Specification	Min.	Nom.	Max.	Units
Input Operating Voltage	2.5	5	5.5	V
Input Voltage UVLO Rising	2	2.22	2.45	V
Input Voltage UVLO Falling	1.8	2.02	2.25	V
Output Voltage	–	1.8	–	V
Output Current (VIN = 5 V)	–	–	2	A

USING THE EVALUATION BOARD

This section provides an overview of the connections and configuration options of the APEK8650 evaluation board. Each group of connections is highlighted in Figure 2 and detailed in the material that follows. For more detailed information about the use and functionality of each pin, refer to the A8650 datasheet.

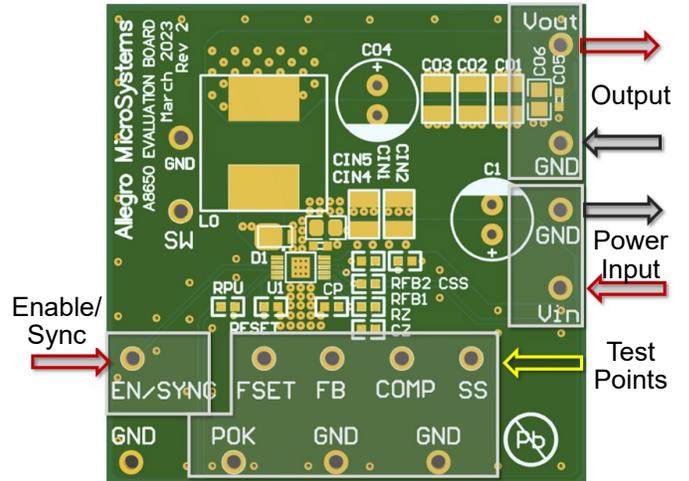


Figure 2: APEK8650 Evaluation Board I/O Connections and Default Jumper Positions

POWER INPUT

Connect a 5 V power supply capable of at least 1.5 A from VIN to GND. Once operational, VIN can fall as low as 2.02 V typical (2.25 V max) before the A8650 is reset.

DEVICE CONFIGURATION

To enable the A8650, connect the power input and connect a signal from EN/SYNC to GND. If the EN/SYNC input voltage exceeds 1.8 V, the A8650 becomes enabled. If the EN/SYNC input voltage is less than 0.8 V, the A8650 becomes disabled. Also, EN/SYNC may be used to simultaneously enable the A8650 and synchronize the PWM switching frequency by applying a square wave with frequency greater than 2.4 MHz.

Do not exceed the absolute maximum rating of 6 V on the VIN or EN/SYNC pin. For maximum ratings of all pins, refer to the datasheet.

Test points on the evaluation board are used to monitor or exercise the A8650. For a description of each test point, see Table 3.

Table 3: Test Point Descriptions

Test Point	Description
VIN	Positive terminal for input-voltage connection or sensing
VOUT	Positive terminal for output-voltage connection or sensing
GND	Negative terminal for voltage input/output or sensing
EN/SYNC	EN/SYNC pin external logic input for chip enable or switching-frequency synchronization
SS	Soft-start pin voltage-monitor test point
FSET	FSET voltage-monitor test point
POK	Power OK signal test point: This pin is pulled up to VOUT and asserts low to indicate the output is out of regulation
FB	Feedback pin test point
COMP	Current mode control-loop compensation test point

EVALUATION BOARD PERFORMANCE DATA

Startup and Shutdown

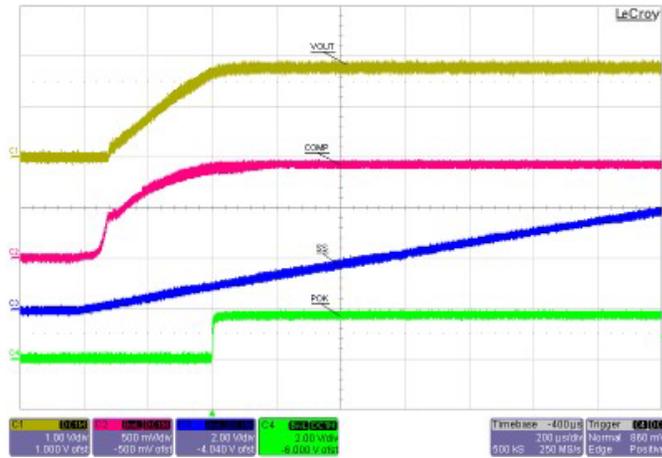


Figure 3: Startup with $V_{IN} = 5\text{ V}$, $I_{OUT} = 1.8\text{ A}$ ($1\ \Omega$ load)

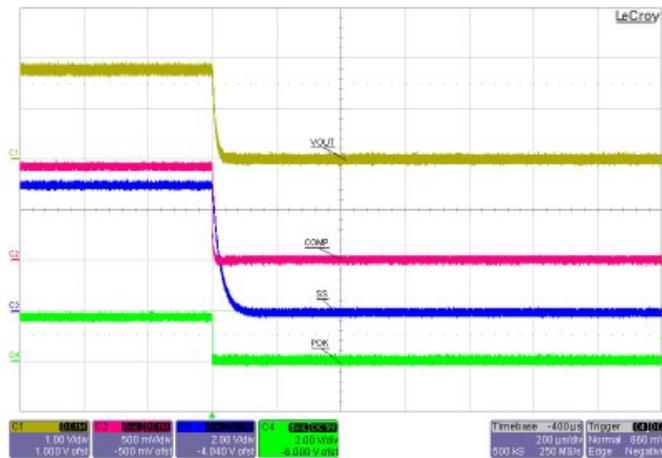


Figure 4: Shutdown with $V_{IN} = 5\text{ V}$, $I_{OUT} = 1.8\text{ A}$ ($1\ \Omega$ load)

Load-Transient Response

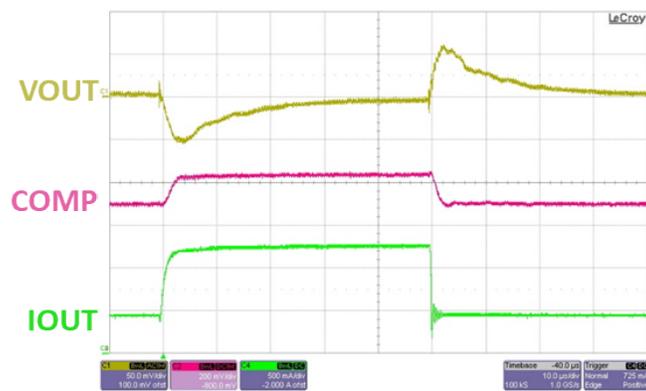


Figure 5: V_{OUT} Response to Load Transient with $V_{IN} = 5\text{ V}$ and Load Step = 500 mA to 1.5 A

Efficiency

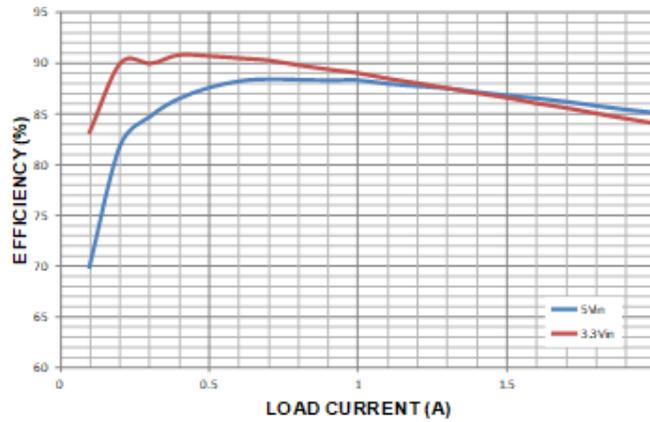


Figure 6: Efficiency with $V_{OUT} = 1.8\text{ V}$

Load Regulation

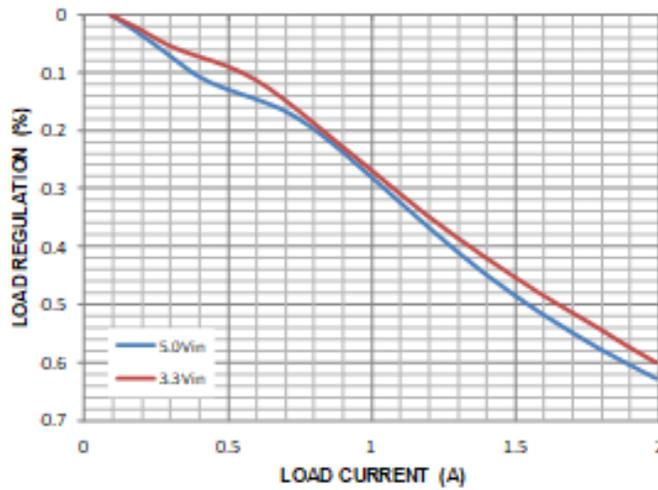


Figure 7: Load Regulation with $V_{OUT} = 1.8\text{ V}$

Line Regulation

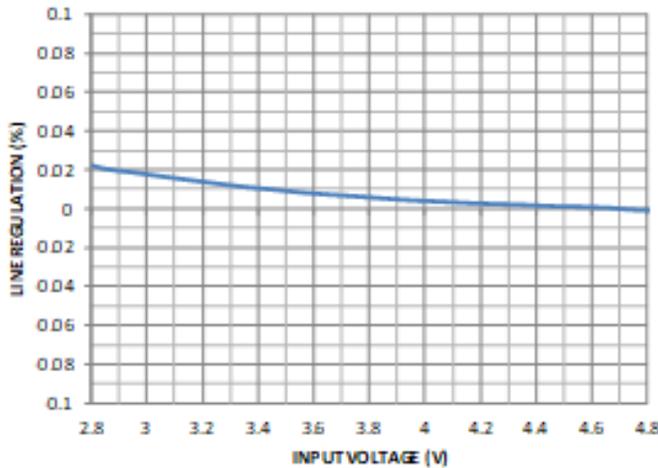


Figure 8: Line Regulation with $V_{OUT} = 1.8\text{ V}$

SCHEMATIC

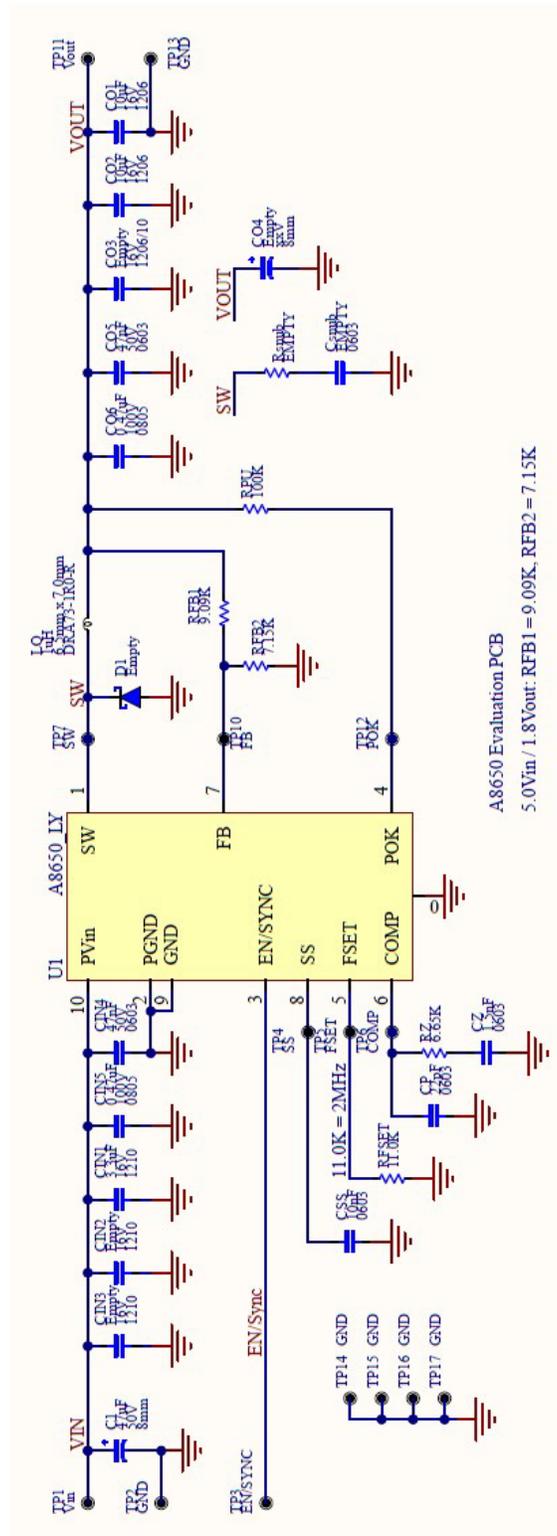


Figure 9: APEK8650KLY Evaluation Board Schematic

LAYOUT

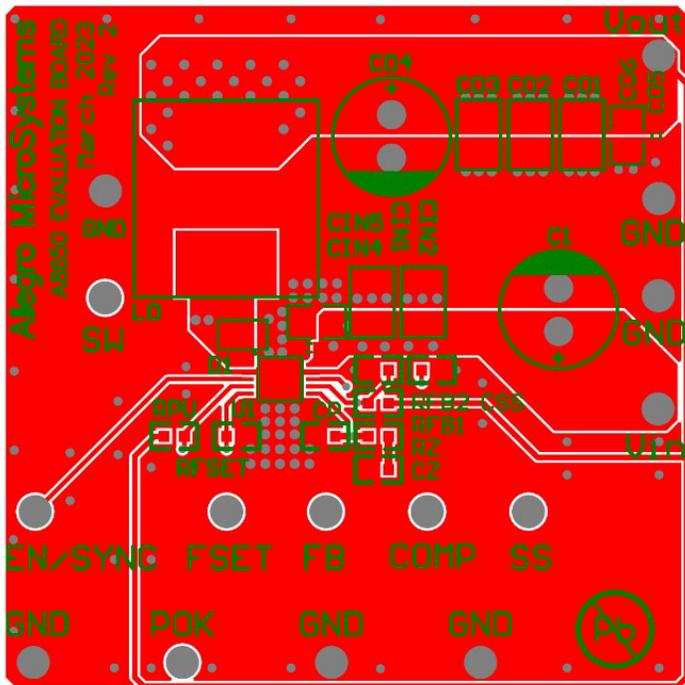


Figure 10: Top Layer with Silk Screen

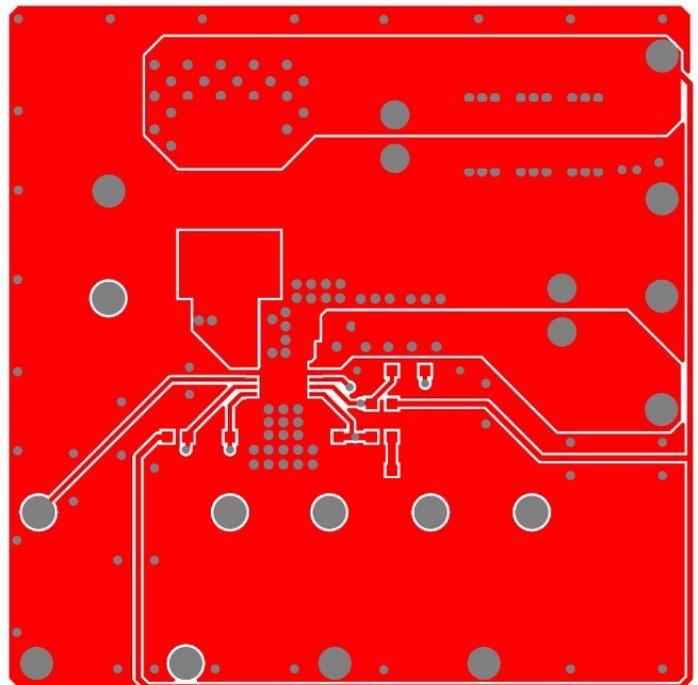


Figure 11: Top Layer

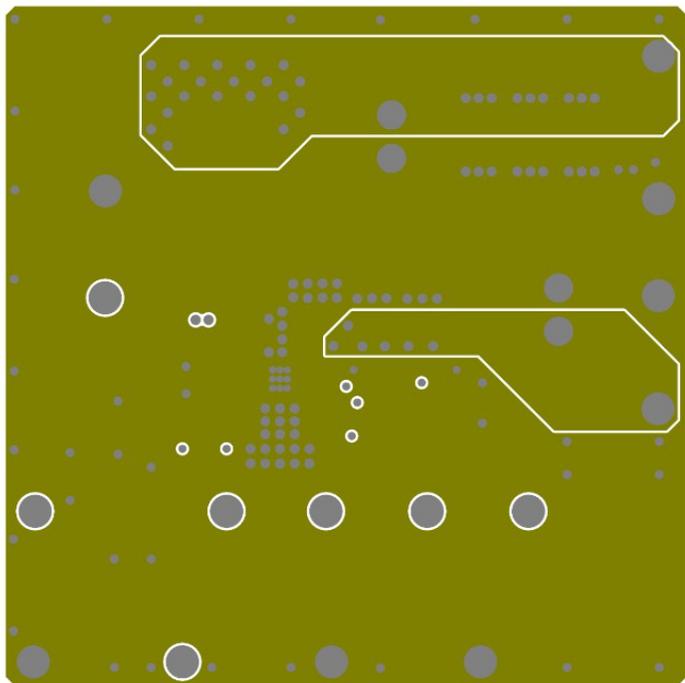


Figure 12: Inner Layer 1

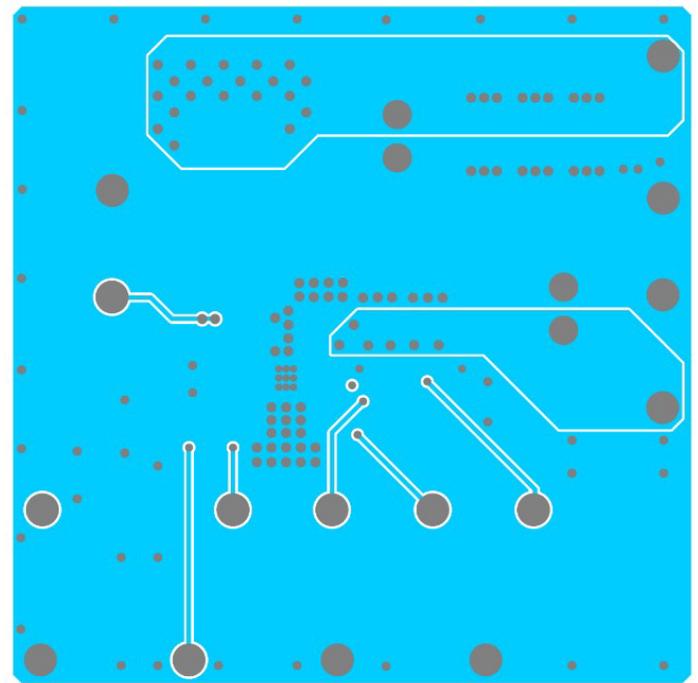


Figure 13: Inner Layer 2

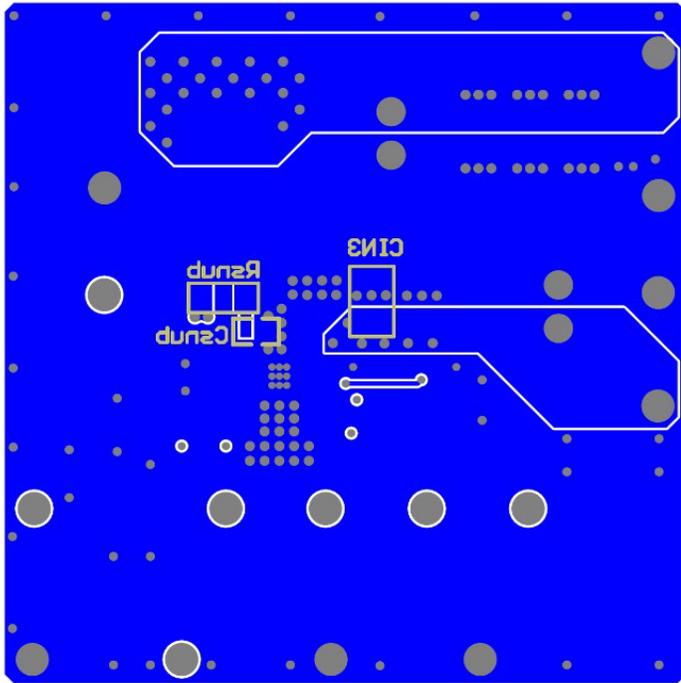


Figure 14: Bottom Layer with Silk Screen

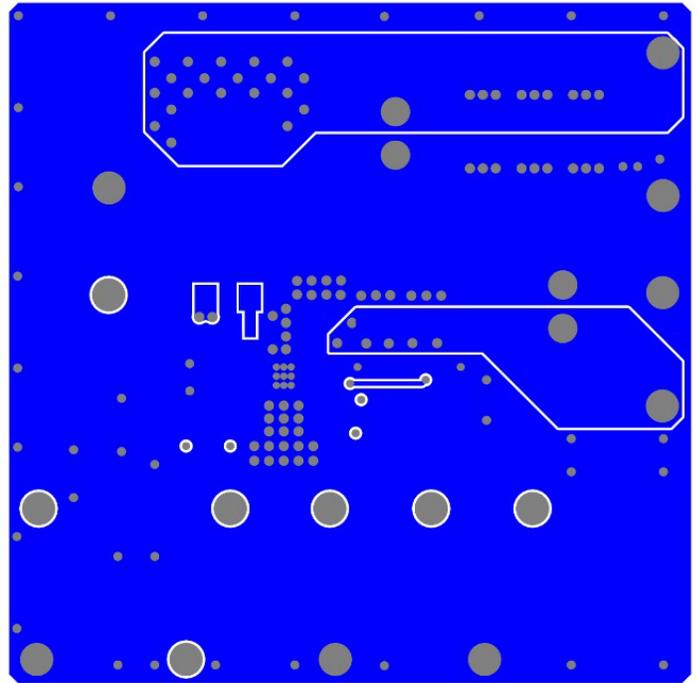


Figure 15: Bottom Layer

BILL OF MATERIALS

Table 2: APEK8650KLY Evaluation Board Bill of Materials

Designator	Description	Footprint	Qty	Manufacturer	Manufacturer Part Number
U1	A8650 2 A Buck Regulator	eMSOP-10	1	Allegro MicroSystems	A8650KLYTR-T
RFB1	Resistor, 9.09 kΩ, 1/10 W, 1%	0603	1	Yageo	RC0603FR-079K09L
RFB2	Resistor, 7.15 kΩ, 1/10 W, 1%	0603	1	Yageo	RC0603FR-077K15L
RFSET	Resistor, 11.0 kΩ, 1/10 W, 1%	0603	1	Yageo	RC0603FR-0711KL
RZ	Resistor, 6.65 kΩ, 1/10 W, 1%	0603	1	Yageo	RC0603FR-076K65L
RPU	Resistor, 100 kΩ, 1/10 W, 1%	0603	1	Yageo	RC0603FR-07100KL
C1	Capacitor, electrolytic, 47 μF, 50 V, <0.5 Ω, -40°C to 125°C	Thru-hole, 8 mm x 11.5 mm	1	Nichicon	UBT1H470MPD
CIN1	Capacitor, ceramic, 3.3 μF, 16 V, 10% or 20%, X7R, -55°C to 125°C	1206 part, 1210 pads	1	Samsung Electro-Mechanics	CL31B335KOHNNNE
CIN4, CO5	Capacitor, ceramic, 47 nF, 50 V, 10%, X7R, -55°C to 125°C	0603	2	Kemet	C0603C473K5RAC7867
CIN5, CO6	Capacitor, ceramic, 0.47 μF, 100 V, 10%, X7R, -55°C to 125°C	0805	2	Murata	GRM21BR72 A474KA73L
CO1, CO2	Capacitor, ceramic, 10 μF, 16 V, 10%, X7R, -55°C to 125°C	1206 part, 1210 pads	2	TDK	C3216X7R1C106K160AC
CSS	Capacitor, ceramic, 10 nF, 25 V, 5%, C0G	0603	1	TDK	CGA3E2C0G1H103J080AA
CZ	Capacitor, ceramic, 1.5 nF, 50 V, 10%, C0G	0603	1	Murata	GRM1885C1H152JA01D
CP	Capacitor, ceramic, 22 pF, 50 V, 5%, C0G	0603	1	Yageo	CC0603JRNPO9BN220
LO	Inductor, SMT, 1 μH, 6.7 mΩ max, 8.22 Asat	7.6 mm x 7.6 mm, 4.35 mm thick	1	Eaton	DRA73-1R0-R
VIN, EN/SYNC, SW, POK, VOUT, SS, FSET, FB, COMP	Test points, red, 0.063-inch diameter	0.063"	9	Keystone	5010
GND	Test points, black, 0.063-inch diameter	0.063"	5	Keystone	5011
Rubber Feet	Self-stick rubber feet	Clear	4	3M	SJ-5303 (CLEAR)
CO3, CO4, CIN2, CIN3, Rsnub, Csnub, D1	Empty	-	0	-	-

RELATED LINKS

A8650 Product Page: <https://www.allegromicro.com/en/products/regulate/regulators/single-output-regulators/a8650>

A8650 Datasheet: <https://www.allegromicro.com/-/media/files/datasheets/a8650-datasheet.pdf>

APPLICATION SUPPORT

For applications support contact, go to <https://www.allegromicro.com/en/about-allegro/contact-us/technical-assistance> and navigate to the appropriate region.

Revision History

Number	Date	Description
–	November 1, 2023	Initial release

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