ACSEVB-MZ6-MY6

MZ and MY Package Bare Evaluation Board User Guide

DESCRIPTION

Bare evaluation boards offer a method for evaluating Allegro current sensors in a lab environment. This document describes the use of the MZ/MY Package Bare Evaluation Board. This evaluation board (ACSEVB-MZ6-MY6, TED-0004281) is intended for use with any MZ or MY package Allegro Hall-based or TMR-based current sensors.

FEATURES OF THE BARE BOARD

- Enhanced thermal performance
  - □ 6-layer PCB with 2 oz copper weight on all layers
  - □ Nonconductive-filled via-in-pad
  - □ High-performance FR4 material with 180°C glass transition temperature
- Flexible layout for user installed connection points
  - □ Standard Keystone test points
  - □ SMA/SMB connector
  - □ 2-pin headers
- Integrated current-loop resistance can be measured directly on the evaluation board after test-point installation; voltage drop can be measured for approximating power loss in the package.

BARE EVALUATION BOARD CONTENTS

- **NOTE:** It is the responsibility of the user to assemble the board with the desired current sensor and supporting circuitry. This board does not come populated with an Allegro current sensor or other components.
- Recommended supporting circuitry for all compatible current sensors is listed in the Supporting Circuitry section below.

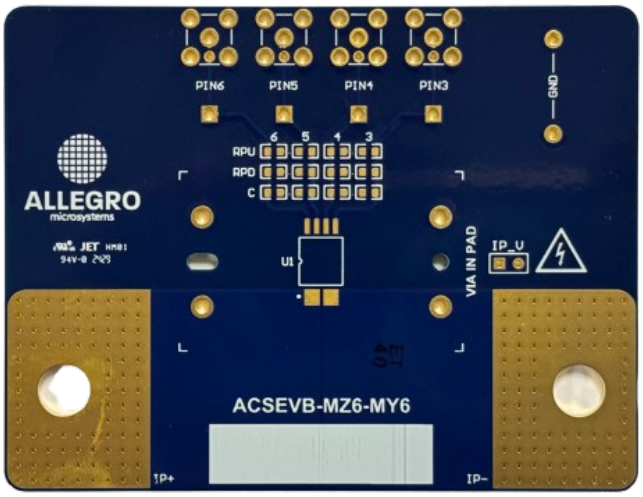
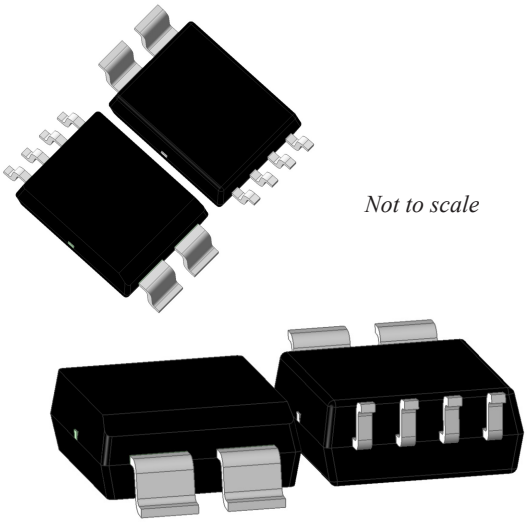


Figure 1: MZ/MY Bare Evaluation Board



Not to scale

Figure 2: Custom SOIC-6 (MZ/MY Package)

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USING THE EVALUATION BOARD

Evaluation Board Procedure

SETTING UP THE EVALUATION BOARD

Upon receiving the evaluation board, it is the responsibility of the user to populate the evaluation board with the desired Allegro current sensor. It is also the responsibility of the user to install test points, SMA/SMB connectors, header connectors, and supporting circuitry, as needed.

CONNECTING TO THE EVALUATION BOARD

The most reliable way to connect measurement instruments to the evaluation board is to use SMB/SMA or 2-pin header connectors along with coaxial cables. This configuration is the most resilient to external coupling, is the most mechanically stable, and is the preferred way to measure a high-speed signal.

Keystone test points provide a convenient way to connect any instrument but are recommended for DC setups only.

Evaluation Board Detailed Description

1. U1 is a combined MZ and MY package footprint (pin 1 is on bottom left side of the package footprint; see the small white dot to the left of the package footprint).
2. U1 pins allow the option to connect:
   - ♦ RPU: pull-up resistor to VCC
   - ♦ RPD: pull-down resistor to GND
   - ♦ C: decoupling or load capacitor to GND

NOTE: Even-numbered pin components are on the top layer of the evaluation board and odd-numbered pin components are on the bottom layer of the board. All passive components are 0603 package size.

3. Optional through-hole test points (Keystone 5005 test points, e.g., Digikey# 36-5005-ND)
4. Optional standard SMB or SMA connection points (e.g., Digikey# 1868-1429-ND)
5. Optional 2-pin 100 mil header connector (note: either SMB or header can be assembled)
6. Primary current cables mounting positions (positive current flow direction is left to right)
7. Optional 2-pin 100 mil header connector for voltage drop measurement across the integrated current loop of the current sensor
8. RB1, RB2, RB3, and RB4: rubber bumper mounting positions (e.g., Digikey# SJ61A6-ND)

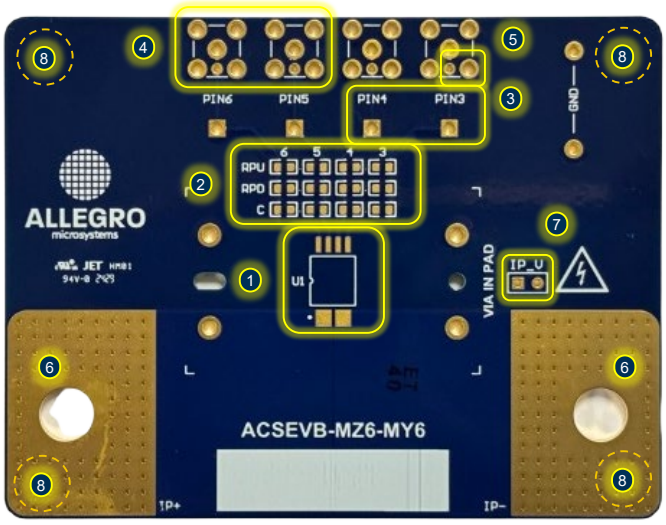

Figure 3: MZ and MY Bare Evaluation Board Reference Image

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

SCHEMATIC

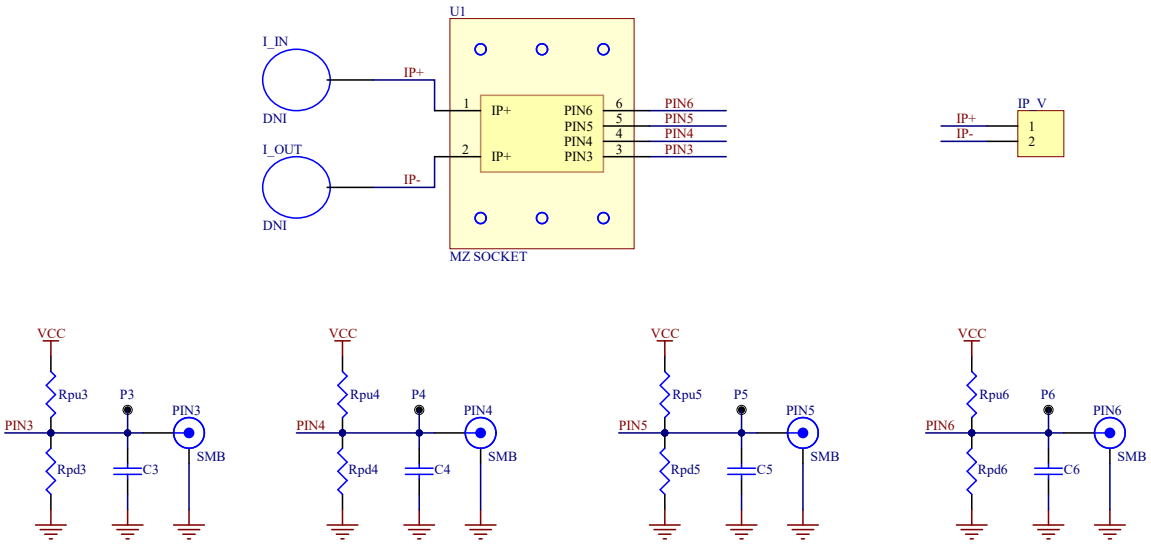

Figure 4: MZ and MY Bare Evaluation Board Schematic

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LAYOUT

The MZ and MY bare evaluation board has the option for a 2-pin 100 mil header connector, which allows the integrated current-loop resistance to be measured directly from the evaluation board. The voltage drop sensing is routed in the first internal layer (as not to reduce the isolation specification of the package). As a consequence, the voltage drop includes the parasitic resistance of the vias between the top layer and the first interior layer.

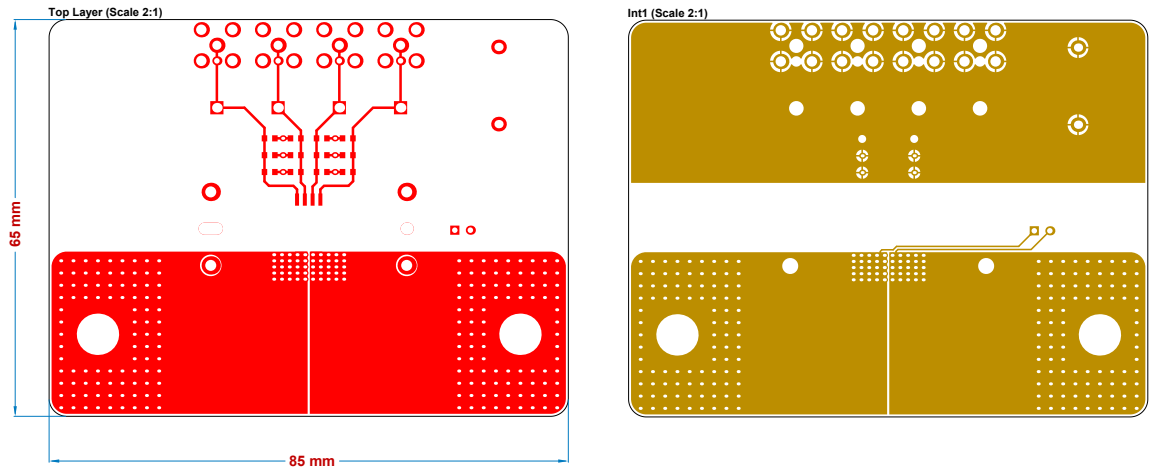

Figure 5: Bare Evaluation Board Top Layer (left) and Interior Layer 1 (right)

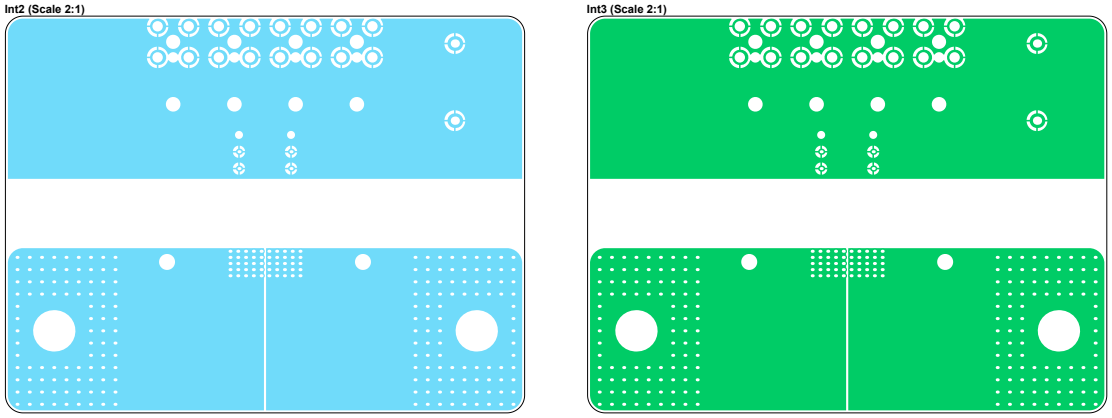

Figure 6: Bare Evaluation Board Interior Layer 2 (left) and Interior Layer 3 (right)

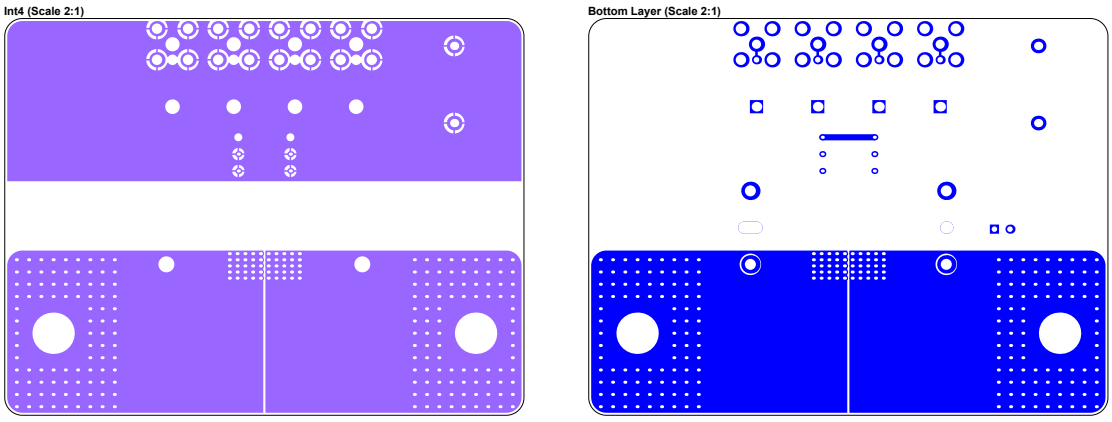

Figure 7: Bare Evaluation Board Interior Layer 4 (left) and Bottom Layer (right)

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SUPPORTING CIRCUITRY

Components listed are based on the typical application circuit given in the respective device datasheet. In the event of a conflict between this document and the main datasheet, the datasheet takes precedence.

Table 1: Evaluation Board Circuitry

ACS37220LMZ ASSEMBLY VARIANT

Pin	Terminal	Components
5	GND	Connect to GND
6	NC	Connect to GND, optional
7	VOUT	C_{L_OUT} = 1 nF, optional
8	VDD	C_{BYPASS} = 100 nF

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Revision History

Number	Date	Description
–	October 29, 2024	Initial release

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