Package Thermal Characteristics

INTRODUCTION

This document provides test information about the standard packages offered by Allegro MicroSystems. The data given is intended as a general reference only and is based on certain simplifications such as constant chip size and standard bonding methods.

To use this document, in the Allegro Package Code column, locate the package designator for the device. To locate package variants, use the JEDEC Package Outline column to locate the corresponding JEDEC designator, or use the Quantity and Type of Terminals column to locate the variant by the configuration of terminals.

Three columns of results are presented:

- $R_{\theta JA}$ High K. This test is performed using a high thermal conductivity, multilayer printed circuit board that closely approximates those specified in the JEDEC standards JESD51-7 (for surface-mount devices except area array devices), JESD51-9 (for area array devices), or JESD51-10 (for through-hole devices). For devices with exposed thermal pads, thermal vias are included per JESD51-5. These standards are available for download on the JEDEC website, www.jedec.org.
- $R_{\theta JA}$ Usual. This test is performed using a common printed circuit board. Where only one value is shown in this column, a single-layer printed circuit board with minimal exposed copper area is tested. Where two values are shown in this column, it indicates that the printed circuit board has multiple test locations, each having a different amount of exposed copper foil (2 oz. thickness). Both one- and two-layer boards are tested. The ground leads (power tabs) or exposed pad of the devices are connected to these areas of copper foil. The two results shown indicate the highest and the lowest test results.
- $R_{\theta JP}$ and $R_{\theta JT}$. This column provides results on other thermal dissipation paths:
  - $R_{\theta JP}$ [p] Through the exposed thermal pad (for related topic, see Application Note 26020, Procedure for Measuring Pad-to-Ambient Thermal Resistance ($R_{\theta PA}$) for Exposed Pad Packages).
  - $R_{\theta JT}$ [t] Certain devices have some leads joined together (fused) internally, and in some instances externally, to provide more efficient heat dissipation (referred to as a power tab or batwing configuration).

PACKAGE DESIGNATORS

Allegro Package Code	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity and Type of Terminals	$R_{\theta JA}$		$R_{\theta JP}$ $R_{\theta JT}$ (°C/W)
				High K (°C/W)	Usual (°C/W)	
A	Plastic Dual In-Line (DIP, PDIP, DIL, or PDIL)	MS-001 AA	14-Pin	40	73	–
		MS-001 BB	16-Pin	38	68	–
		MS-001 AC	18-Pin	36	65	–
		MS-001 AD	20-Pin	32	60	–
		MS-010 AA	22-Pin	30	56	–
		MS-001 AF	24-Pin	26	50	–
		MS-011 AB	28-Pin	–	45	–
B	Semi-Tab Plastic Dual In-Line (DIP, PDIP, DIL, or PDIL)	MS-001 BB	16-Pin	28	41-63	6 [t]
		MS-001 AF	24-Pin	26	36-54	6 [t]
CA/CB	Current Sensor: Refer to device datasheet	–	–	–	–	–
CG	Wafer-level Chip Scale Package (WLCSP): refer to device datasheet	–	–	–	–	–
EC	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WGGE	4 × 4 mm 26-Contact	35	–	2 [p]
ED	Semi-Tab (four) Plastic Leaded Chip Carrier (PLCC/PQCC)	MS-018 AC	44-J Lead	22	30-50	6 [t]
EE	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 UCCD	2 × 2 mm 8-Contact	49	92-219	–
		MO-229 UEED	2 × 2 mm 10-Contact	–	55	–
EG	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WGHD	4 × 5 mm 28-Contact	33	–	2 [p]
EH	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WCED	3 × 2 mm 6-Contact	50	70-221	2 [p]
EJ	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WEED	3 × 3 mm 10-Contact	45	65-190	2 [p]
EK	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WEEA	3 × 3 mm 5-Contact	50	72-182	2 [p]
EL	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 WCCD	2 × 2 mm 6-Contact	56	95-250	2 [p]
ES	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WEED	3 × 3 mm 16-Contact	47	96-133	–
		MO-220 WGGD	4 × 4 mm 20-Contact	37	75-136	2 [p]
		MO-220 WGGD	4 × 4 mm 24-Contact	37	–	–
ET	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 VHHD	5 × 5 mm 28-Contact	32	64-115	2 [p]
			5 × 5 mm 32-Contact	30	–	–
EU	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WGGC	4 × 4 mm 16-Contact	36	–	2 [p]
EV	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 VJJD	6 × 6 mm 36-Contact	27	64-103	2 [p]
		MO-220 VJJD	6 × 6 mm 40-Contact	27	–	2 [p]
		MO-220 VKKD	7 × 7 mm 48-Contact	24	–	2 [p]
EW	Plastic Leadless Package with Exposed Thermal Pad (MLPD/DFN/SON)	MO-229 X2BCD	1.5 × 2 mm 6-Contact	64	125-235	–

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Allegro Package Code	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity and Type of Terminals	$R_{\theta JA}$		$R_{\theta JP}$ $R_{\theta JT}$ (°C/W)
				High K (°C/W)	Usual (°C/W)	
EX	Plastic Leadless Package with Exposed Thermal Pad (MLPQ/QFN)	MO-220 WEED	3 × 3 mm 10-Contact	–	24	–
		MO-220 WEED	3 × 3 mm 12-Contact	–	24	–
		MO-220 WGGD	4 × 4 mm 26-Contact	–	55	–
JP	Plastic Low-Profile Quad Flatpack with Exposed Thermal Pad (eLQFP)	MS-026 BBA-HD	32-Gull Wing	23	44	2 [p]
		MS-026 BBC-HD	48-Gull Wing	23	44-86	2 [p]
JS	Plastic Thin-Profile Quad Flatpack with Exposed Thermal Pad (TQFP)	MS-026 ADD-HD	80-Gull Wing	21	–	2 [p]
K	Plastic Single In-Line (SIP)	–	4-Lead	–	177	–
KA	Plastic Single In-Line (SIP)	–	5-Lead	–	164	–
KB	Plastic Single In-Line (SIP)	–	3-Lead	–	177	–
KC	Plastic Single In-Line (SIP)	–	3-Lead	–	177	–
KE	Plastic Single In-Line (SIP)	–	4-Lead	–	156	–
KH	Plastic Single In-Line (SIP)	–	3-Lead	–	165	–
KN	Plastic Single In-Line (SIP)	–	4-Lead	–	170	–
KT	Plastic Single In-Line (SIP)	–	4-Lead	–	174	–
L	Plastic Small-Outline IC (SOIC)	MS-012 AA	8-Gull Wing	80	140	–
		MS-012 AB	14-Gull Wing	65	120	–
		MS-012 AC	16-Gull Wing	64	118	–
LA	Plastic Small-Outline IC (SOIC) with internally fused conductor	MS-013AA	16-Gull Wing	–	17	–
LB	Semi-Tab Plastic Small-Outline IC (SOIC)	MS-013 AA	16-Gull Wing	38	48-90	6 [t]
		MS-013 AC	20-Gull Wing	38	48-87	6 [t]
		MS-013 AD	24-Gull Wing	35	45-77	6 [t]
LC	Plastic Small-Outline IC (SOIC)	MS-012AA	8-Gull Wing	–	23 [1]	–
LD	Plastic Thin Shrink Small-Outline IC (TSSOP)	MO-153 BD-1	38-Gull Wing	51	127	–
LE	Plastic Thin Shrink Small-Outline IC (TSSOP)	MO-153 AA	8-Gull Wing	145	–	–
		MO-153 AB-1	14-Gull Wing	–	82	–
		MO-153 AC	20-Gull Wing	–	127	–
		MO-153 AD	24-Gull Wing	–	117	–
LF	Plastic Small-Outline IC (SOIC) with internally fused conductor	MO-137AE	24-Gull Wing	–	27	–
LG	Plastic Thin Shrink Small-Outline IC (TSSOP) with 6 internally-fused leads	MO-153 BD-1	38-Gull Wing	47	121	–
LH	Plastic Small-Outline Transistor (SOT23W)	–	3-Lead	154	–	–
		–	5-Lead	124	–	–
LJ	Plastic Small-Outline IC (SOIC) with Exposed Thermal Pad	MS-012 BA	8-Gull Wing	35	62-147	2 [p]
LK	Plastic Small-Outline IC (SOIC) with Exposed Thermal Pad	–	10-Gull Wing	35	–	–
LN	Plastic Small-Outline IC (SOIC)	–	10-Gull Wing	–	130	–
LP	Plastic Thin Shrink Small-Outline IC with Exposed Thermal Pad (eTSSOP)	MO-153 ABT	16-Gull Wing	34	43-129	2 [p]
		MO-153 ACT	20-Gull Wing	23	44	2 [p]
		MO-153 ADT	24-Gull Wing	28	32-100	2 [p]
		MO-153 AET	28-Gull Wing	28	32-100	2 [p]
LQ	Plastic Small-Outline IC (SOIC)	–	36-Gull Wing	44	85	–
		–	44-Gull Wing	35	–	–
LR	Plastic Small-Outline Flip-Chip IC (PSOF)	–	7-Lead	–	18 [2]	–
LS	Plastic Small-Outline Flip-Chip IC (PSOF)	–	10-Lead	–	18 [2]	–

PUB296102, Rev. 4
MCO-0000229

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Allegro Package Code	Package Type (Common Package Designator)	JEDEC Package Outline	Quantity and Type of Terminals	$R_{\theta JA}$		$R_{\theta JP}$ $R_{\theta JT}$ (°C/W)
				High K (°C/W)	Usual (°C/W)	
LT	Plastic Small-Outline Transistor (SOT89)	TO-243 AA	3-Lead	–	78-180	–
LU	Plastic Thin Shrink Small-Outline IC (TSSOP)	–	8-Gull Wing	145	–	–
		–	14-Gull Wing	174	–	–
LV	Plastic Thin Shrink Small-Outline IC with Exposed Thermal Pad (eTSSOP)	–	38-Gull Wing	–	30	–
LW	Wide-Body Plastic Small-Outline IC (SOIC)	MS-013 AA	16-Gull Wing	48	94	–
		MS-013 AB	18-Gull Wing	48	94	–
		MS-013 AC	20-Gull Wing	48	90	–
		MS-013 AD	24-Gull Wing	44	85	–
		MS-013 AE	28-Gull Wing	44	80	–
LY	Mini Small Outline (MSOP) with Exposed Thermal Pad	MO-187BA-T	10-Gull Wing	44	48-177	–
MA	Plastic Small-Outline IC (SOIC-W)	MS-013AA	16-Gull Wing	–	23	–
OL	Plastic Small-Outline IC (SOIC)	MS-012AA	8-Gull Wing	–	125	–
SA	Plastic (9 mm Ø × 9 mm long) SIP Module	–	4-Lead	–	147	–
SB	Plastic (8.9 mm Ø × 7 mm long) SIP Module	–	4-Lead	–	150	–
SE	Plastic (10 mm Ø × 7 mm long) SIP Module	–	4-Lead	–	77-101	–
SG	Plastic (8 mm Ø × 5.5 mm long) SIP Module	–	4-Lead	–	84-126	–
SH	Plastic (8 mm Ø × 5.5 mm long) SIP Module	–	4-Lead	–	54-126	–
SJ	Plastic (8 mm Ø × 5.5 mm long) SIP Module	–	4-Lead	–	54-126	–
SL	Plastic (9.65 or 10.0 mm Ø × 6.0 mm long) SIP Module	–	3-Lead	–	134	–
SM	Plastic (8 mm Ø × 5 mm long) SIP Module	–	3-Lead	–	147	–
SN	Plastic (8 mm Ø × 5 mm long) SIP Module	–	2-Lead	–	150	–
SP	Plastic (8 mm Ø × 5 mm long) SIP Module	–	3-Lead	–	146	–
		–	2-Lead (center pin removed)	–	159	–
UA	Plastic Ultra-Mini Single In-Line (SIP)	–	3-Lead	–	165	–
UB	Plastic Mini Single In-Line (SIP)	–	2-Lead	–	213	–
UC	Plastic Mini Single In-Line (SIP)	–	3-Lead	–	270	–

[1] Mounted on the Allegro 85-xxxx evaluation board with 1500 mm^2 of 2 oz. copper on each side, connected to pins 1 and 2, and to pins 3 and 4, with thermal vias connecting the layers. Performance values include the power consumed by the PCB.

[2] Mounted on the Allegro evaluation board ASEK781 85-0807-001 with FR4 substrate and 8 layers of 2 oz. copper (with an area of 1530 mm^2 per layer) connected to the primary leadframe and with thermal vias connecting the copper layers. Performance is based on current flowing through the primary leadframe and includes the power consumed by the PCB.

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com

Revision History

Number	Date	Description
1	February 15, 2018	Added EE-10, EG-28, ES-24, EX-12, JP-32, KE-4, LA-16, LE-14, LE-20, LE-24, LF-24, LK-10, LN-10, LP-20, LQ-44, LR-7, LS-10, LU-8, LV-38, MA-16, SL-3, SM-3, SN-2, and UC-3 packages; removed U package (obsolete)
2	February 28, 2019	Minor editorial updates
3	May 1, 2020	Corrected LU package description; added LU-14; minor editorial updates
4	April 23, 2024	Added EX-10, EX-26, KH-3, LC-8, OL-8, and SP-3 packages

For the latest version of this document, visit our website:

www.allegromicro.com

PUB296102, Rev. 4
MCO-0000229

Allegro MicroSystems
955 Perimeter Road
Manchester, NH 03103-3353 U.S.A.
www.allegromicro.com